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# Systematic development for fast and high-accuracy wavefront corrector based on liquid crystal on silicon device

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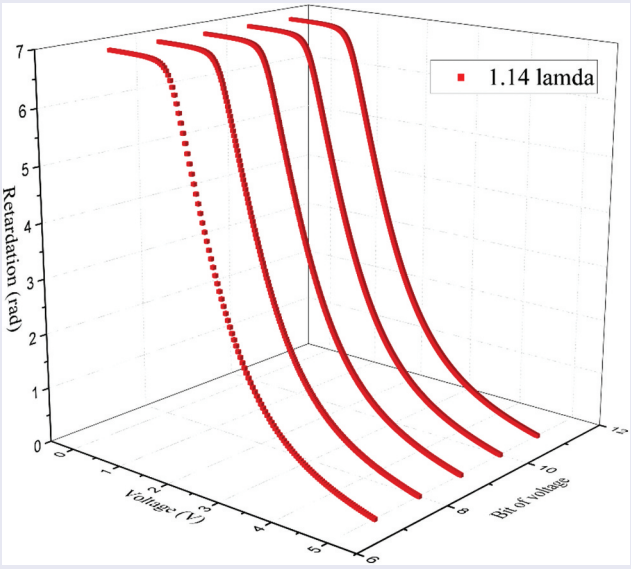
**ABSTRACT**

For wavefront corrector (WFC) based on liquid crystal on silicon (LCoS), existing good phase change linearity and fast response are the key requirements to achieve fast and high-accuracy performance. Aiming at this, refreshing manner and period is optimised firstly to minimise the temporal phase fluctuation derived from pixels phase updating. Grey bit of applied voltage used for LCoS-WFC is also optimised to form better phase linearity and phase modulating accuracy, whether the LCoS is under over-driving method or not. After optimisation, both the phase error derived from poor phase linearity and the temporal phase fluctuation derived from improper refreshing process could be reduced by nearly one time, and the phase modulated step can be reduced to 80% of that before optimisation. This result can not only save significant LCoS design costs, but also provide full design guidance for future improvement of LCoS WFC.

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Liquid crystal on silicon; wavefront corrector; systematic optimisation; fast response; high accuracy

## 1. Introduction

Liquid crystal spatial light modulator (LC-SLM), especially as wavefront corrector (WFC) device, have been used in adaptive optics system (AOS) for many years [1–3]. WFC based on liquid crystal on silicon (LCoS) can achieve real-time pixel-by-pixel control of the amplitude or phase modulation of incident light. Compared with transmission type LC-SLM [4], such as thin film transistor liquid crystal display (TFT-LCD), the reflective structure of LCoS chip could significantly improve light utilisation [5]. Furthermore, compared with conventional deformable mirror device (DMD) WFC, LCoS-WFC does not need any dynamic mechanical components, but offers higher reliability, accuracy, and resolution as well as lower power consumption and cost [6–8]. Meanwhile, LCoS-WFC could easily provide millions of active pixels based on nano-level complementary metal oxide semiconductor (CMOS) technology of silicon chip. It is much easier to expand its phase modulation depth from 1 λ to over ten times larger [6,9,10] by using

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phase wrapping technique [11–13]. Therefore, LCoS-WFC could be widely used in phase modulation system, such as the beam deflection in light detection and raging (LIDAR) system [14,15].

Usually, the phase change of LCD with applied voltage is nonlinear; this nonlinear phase response would degrade modulating accuracy of LCSLM [16,17]. Especially when used as wavefront corrector, relation between phase modulation and applied voltage of LCoS should be linear to achieve high-accuracy waveform correction [18]. Better phase linearity will not only decrease phase modulated error but also enhance data handling efficiency. People have explored linear lookup table (LUT) to solve this disadvantage of nonlinear phase response of LCSLM [19]. The function of the LUT is to provide linear relationship between phase modulation and the voltage grey level. In industrial displays, similar as the LUT in phase modulation field, gamma correction based on complex peripheral circuit design is used to correct the nonlinearity between brightness of LCD and its applied voltage [20]. It can be seen that whether it is used for phase modulation or brightness display, the core to solving nonlinear problem is to ensure the precise subdivision of applied voltage. But for CMOS LCoS-WFC, precise subdivision of voltage needs complex circuit design which means more complicate fabrication procedure and higher power consumption [9]. Besides, overly complex driving circuit of LCoS-WFC would cause slow transmitting of pixels data which would lead to the happen of poor synchronisation during frame refreshing. Therefore, it can be seen that the degree of precise subdivision of applied voltage by LCSLM driver should be appropriately optimised. Driving mechanism of LCoS-WFC is another key parameter for improving correction speed and accuracy [7], although most work is focused on device structure optimisation, fast LC material design and temperature optimisation [21–24] reported previously. For this, digital voltage technique such as pulse width modulation (PWM) [25–27] has been explored to drive LCoS-SLMs. PWM adopts the method of changing the pulse width or duty cycle to adjust the voltage and control the brightness of LCoS. It can be seen that the output voltage of PMW is not exactly equal to a specific value but changes over time [28,29]. But when used as LCoS-WFC, the PWM would cause phase flicker effect;, which the phase value would inevitably fluctuate with PWM waveform due to its time dependent voltage value, even if the phase flicker has already been optimised by many researchers [30,31]. It means digital PWM voltage driving method is not suitable for LCoS-WFC, in contrast, analogue voltage method would be a better choice.

Hence based on analogue voltage framework, this work focuses on systematic design for LCoS-WFC. The goal is to achieve linear phase change of LCoS with voltage change but without excessive subdivision of voltage grey level and data transmission slowing. The frame refreshing mode, refreshing period and voltage grey level of LCoS WFC are specifically optimised here, and the final improvement of the LCoS-WFC device is quantitatively regulated based on research results and experimental data.

## 2. Method

For theoretical simulation, LC molecules kinetic process is depicted by Erickson-Leslie equation, and the backflow and inertial effects are ignored to simplify the model [32]. In this work, the LCoS device is designed in anti-parallel mode with 2° pretilt angle on both substrates and the cell gap $d$ is divided into 100 layers. Differential iteration method is utilised to process theoretical calculation for LC director distribution as reference [3]. As shown in Figure 1, $\theta$ is the rotation angle between LC molecules director and substrate in Z-axis plane, $U$ is the applied voltage of LC cell. Based on the above methods, the phase changes and response curve of LCoS-WFC between every two applied voltage grey could be simulated then.

## 3. Experiment and results

One 2.8 μm LCoS device with 256 × 256 resolution and 8 kHz refreshing rate and with 7 grey bit bought from BNS corporation has been used as WFC for AOS in our previous experiments [33,34], and the correction performance of this 2.8 μm LCoS-WFC is used as prototype before optimisation in this work. This device is filled with high birefringence LC material UCF-B [2,35], which could provide whole1.1λ retardation modulation depth within 5 ms at λ = 633 nm; it is referred to as 2.8 μm device in this work.

When correcting wavefront, the phase matrix of LCoS-WFC needs to be refreshed to new phase values frequently to real-time compensate the wavefront residual. This means that in each frame refreshing period, all pixels would fufill importing new phase data process. Taking a normal 1920 × 1080 resolution LCoS as an example, it needs hundreds of microseconds for all pixels to fulfill frame refreshing process. Hundreds of microseconds are already long enough to cause significant asynchronous response between the last refreshed pixel and the first refreshed pixel. Hence, firstly, in this work, the refreshing manner of optimised LCoS is designed with frame buffering technique based on ping-pang operation. 'Ping-pang operation' is a processing

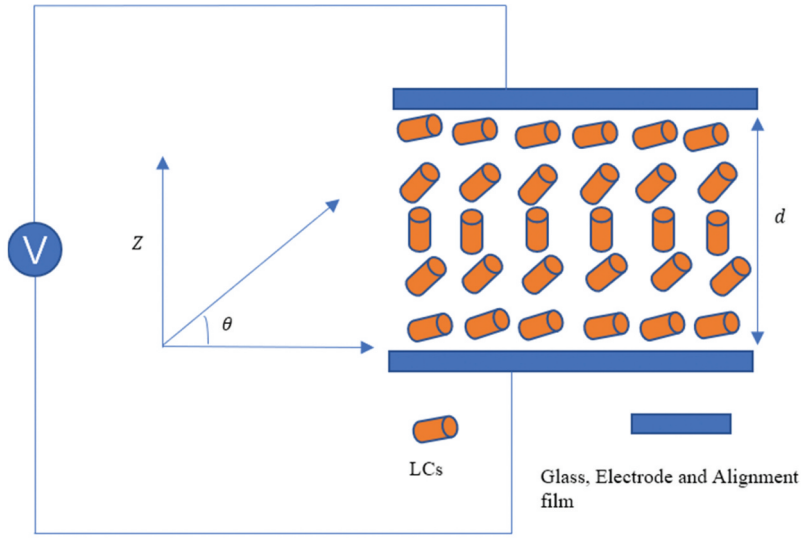


**Figure 1.** (Colour online) Schematic illustration for dynamics response of LC molecule under applied voltage.

technique often adopt for data flow control. Its distinguished feature is that the buffered data stream is calculated and processed without pauses by switching between 'input data unit' and 'output data unit' in a rhythmic and coordinated manner [36]. Through a buffered unit, serial to parallel conversion of data streams is achieved; so, ping-pang operations can enable low-speed modules to process high-speed data. In this work, it is used to pre-charge pixels capacitance required for reconstructing new phase matrix of next frame into buffer capacitor during current frame displaying period. And immediately at the end of current frame, buffer capacitor could accomplish charging all pixel capacitors within very short time due to its large buffer capacitance/pixel capacitance ratio. This means that frame buffer ping-pang operation can greatly reduce the unsynchronised refreshing time of LCoS-WFC. The schematic diagram for refreshing three frames from initial data A to B and then to C is shown in Figure 2. Used 2.8 μm LCoS-WFC device is fabricated

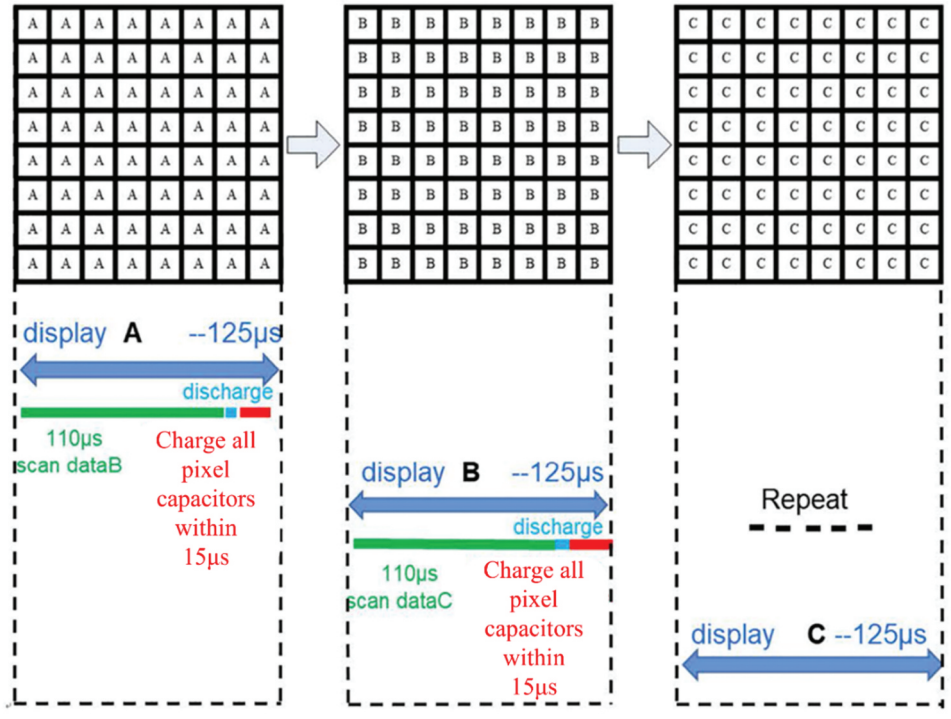


**Figure 2.** (Colour online) Refreshing process for three frames from initial frame a to B and then to C.

with 8 kHz refreshing rate, which its one frame period is 125 μs; hence, here we take 125 μs as one frame period to illustrate frame refreshing process based on ping-pang method. As shown in Figure 2. within 125 μs displaying data A period, buffer could use the first 110 μs of 125 μs to in advance pre-charge pixels capacitance required for new B data into buffer capacitor; then the last 15 μs of 125 μs is used for buffer capacitor to accomplish charging all pixel capacitors for new B data. It shows that with Ping-pang buffering technique of one frame period can be doubly used in parallel; on one hand is 100% for displaying A, on the other hand is 88% of frame period to store data B in advance and the rest 12% to fulfill whole B refreshing just at the end of A display process. It means with the ping-pang method, the pixels asynchronous refreshing time only occupy 12% of whole 125 μs frame period. This new LCoS-WFC refreshing design based on buffered ping-pang technology can significantly shorten pixels asynchronous refreshing time, to be almost 20% of original refreshing time of used 2.8 μm devices. In practical applications, the 2.8 μm LCoS-WFC dose not adopt buffering ping-pang technique, so it needs 55 μs to fulfill all pixels refreshing. Compared with the rising response, the falling response of LC devices is relatively slow, so here we only consider the temporal phase fluctuations during falling response process of LCoS-WFC. The temporal phase fluctuation change caused by refreshing process happened starting from different initial phase values is simulated in Figure 3, especially for different refreshing period of 10 μs/15 μs (our designed LCoS device) and 55 μs (used 2.8 μm LCoS device). The inset graph of Figure 3 is the test falling phase response curve of real 2.8 μm LCoS-WFC after removal of 5 V applied voltage. It shows that the falling response for one wavelength phase modulation depth can be completed within 5 milliseconds due to the application of fast and high birefringence LC material UCF-B. Based on the inset falling response curve, we could calculate temporal phase fluctuation value caused by refreshing happened starting from different phase point of 2.8 μm LCoS during its falling response for different 10 μs, 15 μs and 55 μs refreshing periods. As shown in Figure 3, it shows that shorter refreshing period can achieve smaller phase fluctuation value, which among the three curves, the 55 μs refreshing period produces the largest phase fluctuation value. It also states that the maximum phase fluctuation occurs at the starting point of falling response. With the refreshing starting point goes far away from initial starting point, the phase fluctuation value becomes smaller and smaller; the fluctuation phase value occurred at the end of falling response for three different refreshing periods is all near zero. From the inset graph, we can see that about first 70% part responds much faster than the last 30%, besides the first 70% of the phase falling curve is nearly linearly responsive over time. So, when refreshing occurs at first 70% part of the falling response, 55 μs is sufficient

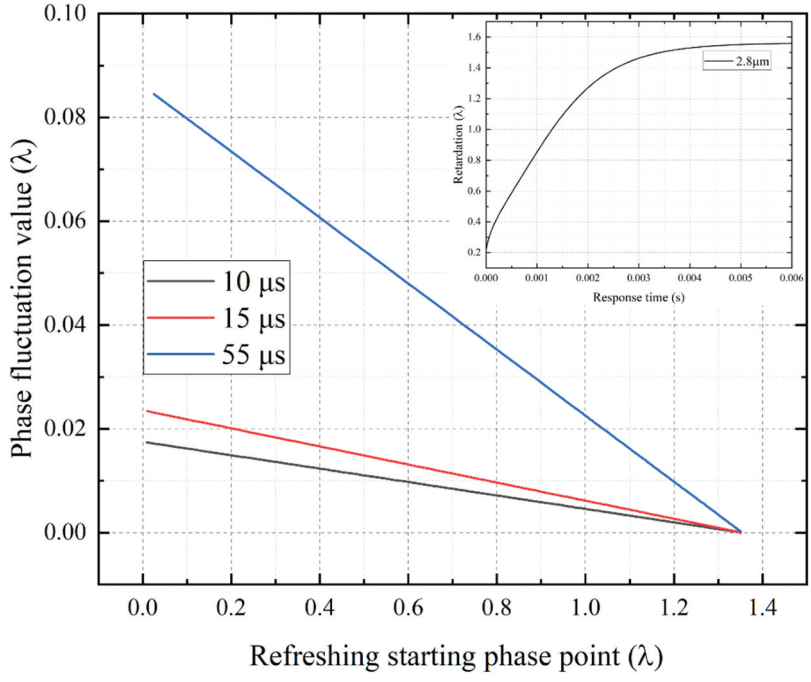


**Figure 3.** (Colour online) Phase fluctuation value curve with refreshing starting from different starting phase values for different refreshing period of 10 μs, 15 μs and 55 μs.

long for fast UCF-B LC molecule to happen tilt to some extent, resulting in certain amount of phase value fluctuation within the refresh period. So, it is reasonable to see that the phase fluctuation value is relatively larger when refreshing happens at the linearly responsive region of LCoS response. And when refreshing happens close to the end regions of LCoS exponential response process, the phase fluctuation value is relatively smaller. The reason for these results is just due to the exponential response nature of LC device. And this result is also consistent with LC response test work reported previously [37].

Table 1 summarises the maximum phase fluctuation value for three different refreshing periods. It states that short refreshing period could greatly reduce the phase fluctuation. With design of frame buffering technique, our optimised LCoS in this work could reduce its refreshing time to be around 20% of its original with 10 kHz refreshing rate. Correspondingly, the phase fluctuation value could be reduced from original 0.07 λ to be 0.015 λ. Compared with 55 μs in practical 2.8 μm LCoS WFC, 10 μs and 15 μs refreshing period could reduce its temporal phase fluctuation value by 78% and 71%, respectively. These results indicate that shortening refresh time is beneficial for LCoS-WFC to achieve weak refreshed phase fluctuations.

Beside the refreshing manner and period, maximum applied voltage and available phase modulation depth are another two key parameters to affect correction performance; and these two factors are correlated to each other. It is known to all that LCoS-WFC needs to provide at least 1 λ (@633 nm in this work) modulation depth to accomplish phase wrapping when used as WFC. Inside LC device, due to strong anchoring of alignment layer [38], the surface layer LC molecules is hard to be tilt to the same inclination degree as the intermediate layer LC molecules even if they are both under same applied voltage. Surface anchoring of LC molecules closest to the alignment layer is usually considered infinite, and an infinite external field is required in order to tilt the LC molecules. Therefore, under a finite external field, there is always a portion of strongly anchored LC molecules which cannot be driven by the finite electric field in the cell, and the phase quantity that can not be changed caused by these molecules is called the unable driving phase value here. This unable driving phase value can not be counted into the available modulation depth under its maximum applied voltage. In other words, under specific applied voltage, effective phase depth of the LCoS-WFC will be somewhat reduced compared to its theoretical phase depth. Hence, when designing LCoS-WFC, it is necessary to make sure its effective phase depthunder specific applied voltage. Here, taking the used 2.8 μm LCoS device (manufactured with CMOS chip of maximum 5 V voltage) as reference, we simulate the phase response curve under different maximum voltage with 10 bit voltage grey level, still filled with UCF-B LC material as shown in Figure 4. The unable driving phase values of the 2.8 μm cell under different maximum voltages are summarised in Table 2. It can be seen that as the maximum voltage increases, the unable driving phase value gradually decreases. When maximum voltage is 5.0 V, the unable driving phase value is about 13.6% of its total phase, and this value could be down to be 8.0% when maximum voltage is 8.0 V. It shows that the increased 3 V voltage could release 5.6% of the effective phase modulation quantity for LCoS-WFC. This means that the starting position of phase falling response shown in Figure 3 inset graph could been lowered, from the original 13.6% point to the 8% point of the total phase value. And this lower phase starting position means more of the fast response portion of LCoS response is released to be as effective modulation phase, which means that the response time required for 1 λ effective phase modulation will be shortened. All these results says that less unable driving phase could promote fast phase modulating performance; meaning higher maximum voltage could form faster response for LCoS-WFC compared to that with lower applied voltage. And this result is also consistent with the published results in Ref [39].

Based on the above results, it is found that the driving voltage of the LCoS should be as high as possible. For CMOS chip for LCoS, 5.0 V is the most commonly used voltage, so 5.0 V is chosen as maximum voltage in following work. Given that the unable driving phase value is about 13.6% of its total phase under 5.0 V maximum voltage; hence, for further design of LCoS-WFC in this work, the total phase depth is set to be about 1.14 λ at λ = 633 nm.

After the maximum voltage and modulation depth is determined, the next is to confirm the grey level of voltage, thereby to determine the degree of linearity for the effective phase depth under corresponding voltage grey level. The 2.8 μm LCoS WFC device is used as reference again, with maximum 5.0 V voltage, 7 grey bit and total phase depth of 1.14 λ at 633 nm. First, in this work, effective phase modulation quantity of 1.0 λ at 633 nm is linearly divided into 256 parts, and these 256

**Table 1.** Maximum phase fluctuation value caused by 10 μs, 15 μs and 55 μs refreshing period.

| Time (μs) | 10 | 15 | 55 |
|---|---|---|---|
| Phase fluctuation (λ) | 0.015 | 0.02 | 0.07 |
| Improved ratio (%) | 78.6 | 71.4 | 0 |

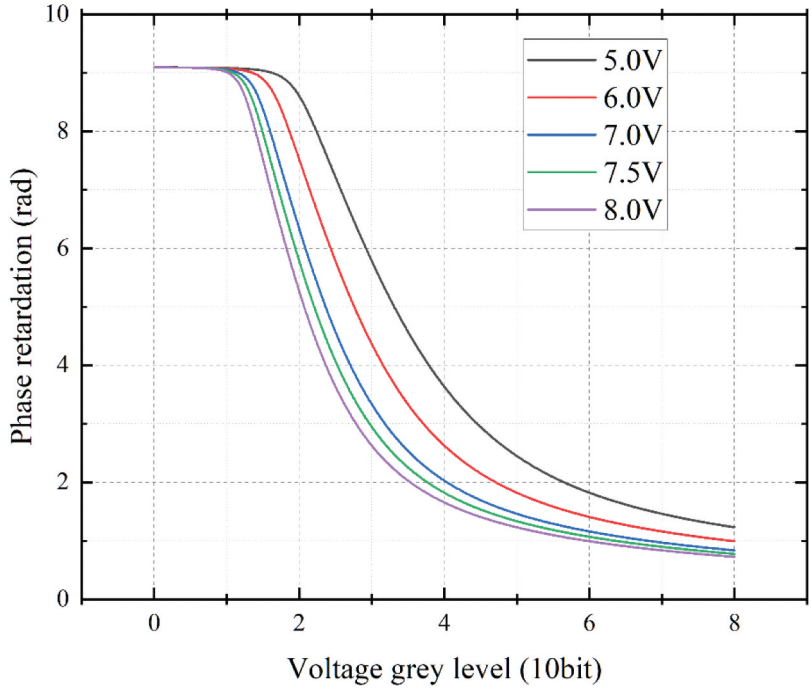


**Figure 4.** (Colour online) Phase response curve with 10 bit voltage grey level of LCoS cell for different maximum voltage.

**Table 2.** Unable driving phase value of 2.8 μm cell under different Max. voltage of 5.0 V, 6.0 V,7.0 V, 7.5 V, 8.0 V.

| Voltage (V) | 5.0 | 6.0 | 7.0 | 7.5 | 8.0 |
|---|---|---|---|---|---|
| The total phase (rad) | 9.09385 | 9.09385 | 9.09385 | 9.09385 | 9.09385 |
| Unable driving phase (rad) | 1.23239 | 0.99398 | 0.83796 | 0.77815 | 0.72693 |
| Ratio of unable to total (%) | 13.6 | 10.9 | 9.2 | 8.6 | 8.0 |

**Table 3.** The phase effective number, error, and step height for 8, 9, 10, 11-bits respectively.

| Bit of voltage | Effective phase number | Phase error(λ) | Error reduced ratio (%) | Phase step (λ) | Step raised ratio (%) |
|---|---|---|---|---|---|
| BNS device (7) | 83 | 0.0128 | 0 | 0.0266 | 0 |
| 8 | 136 | 0.0065 | 49.2 | 0.0132 | 50.4 |
| 9 | 207 | 0.0032 | 75.0 | 0.0071 | 73.3 |
| 10 | 256 | 0.0016 | 87.5 | 0.0066 | 75.2 |
| 11 | 256 | 0.00081 | 93.7 | 0.0049 | 81.6 |

linear values are used as standard values to measure the phase linearity of designed LCoS-WFC under different voltage grey bit. Phase change of full 1.14 λ modulation depth under voltage grey bits of 7, 8, 9, 10 and 11 are simulated in Figure 5. Then, based on 256 standard phase values, find the closest phase value in the phase response curve as its effective phase value under corresponding grey level. Figure 5 shows that as the grey level increases, the spacing between phase changing points becomes more dense, which means selectivity of providing 256 linear effective phase values are increased. The effective linear phase value of LCoS-WFC under 5 V with 7, 8, 9, 10 and 11-bits relative to the standard phase values is shown in Figure 6. It shows that 7, 8, 9, 10 and 11-bits all can provide certain linear phase change value, with difference in number and changed step and accuracy. And the effective phase value number, the phase step (difference between effective linear phase values), and phase error (error value between the searched value and the standard phase value) are all summarised in Table 3. These data show that 10-bits grey level is enough to provide 256 effective linear phase values (100% coverage of standard values), and the phase error is reduced by 87.5% and the step height reduced by 75.2% compared with used 2.8 μm LCoS device. And 11-bits also could provide 256 standard phase values, the phase error and the step height is reduced by 6.6% and 6.2% compared with 10-bits, respectively. Based on the above results, the accuracy of the effective linear phase value could be obviously improved when the grey bit of voltage exceeded 10. And considering data transmitting quantity, 11-bits is 1.1 times more than 10-bits, hence 10-bits is the best choice for our designed LCoS-WFC. Till now, the design results of LCoS-WFC are in situation that without overdriving technique.

Besides, overdriving technique is usually adopted to improve response speed for LCoS-WFC [40]. Then the modulated phase depth needs to be expanded to be about 1.2 λ [3, 11]. For LCoS-WFC working with overdriving technique, the effective value number and phase error and phase step are calculated and summarized in Tables 4 and 5.

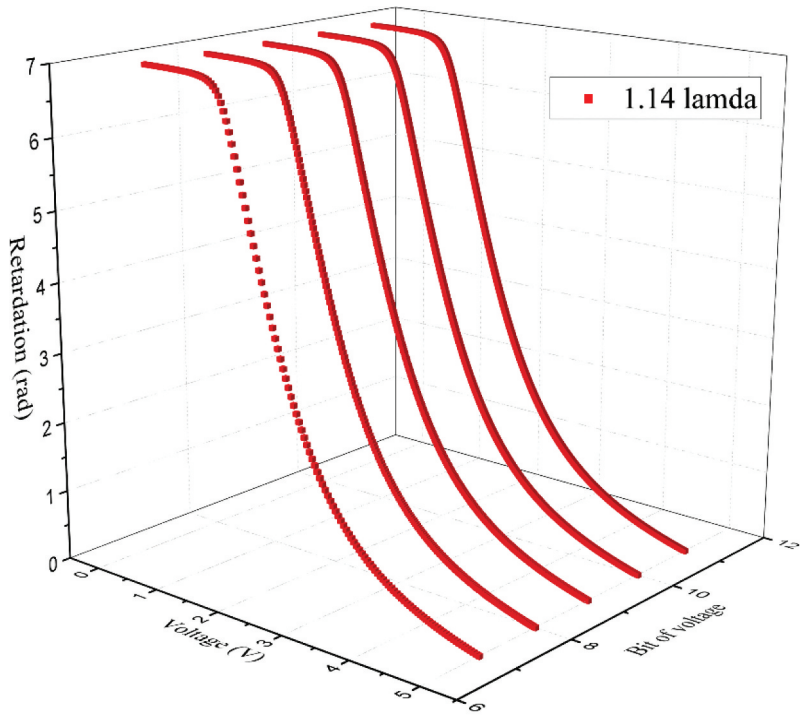


**Figure 5.** (Colour online) The phase changes under 5.0 V voltage of LCoS but with 7, 8, 9, 10 and 11-bits without overdriving.

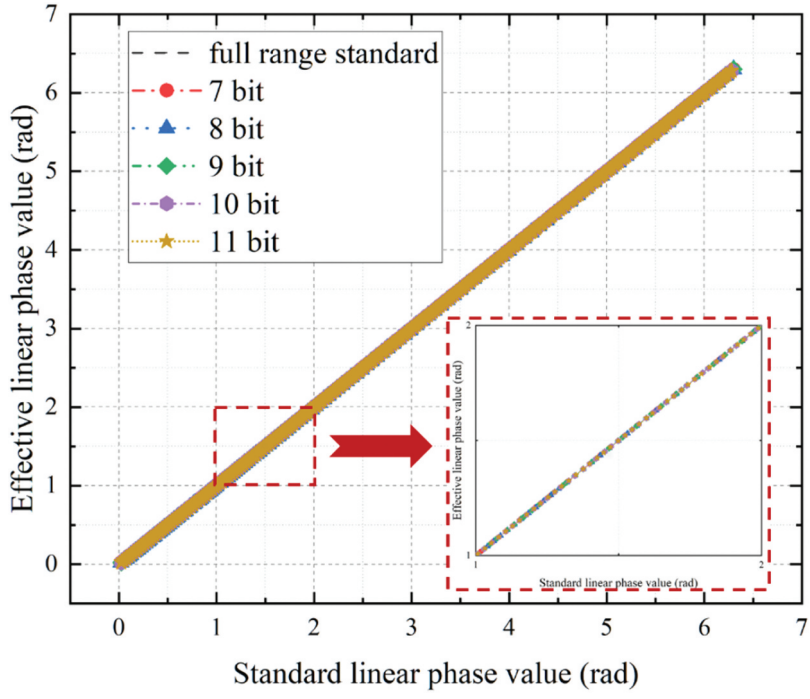


**Figure 6.** (Colour online) The effective linear phase value of LCoS relative to standard phase values under 5 V with 8, 9, 10 and 11-bits without overdriving.

The result shows that the 11-bits can provide full 256 linear values even in overdriving situation. The 10-bits voltage could provide 251 effective linear phase values (98% coverage of standard phase value) and its phase error reduced by 87.4% and phase step improved by 77.5% compared with practical 2.8 μm LCoS device. Compared to 10-bits, 11-bits further improves the effective number, the phase error, and the phase step height 1.9%, 6.8% and 7.8%, respectively, as shown in Table 5. The total phase depth of LCoS-WFC under overdriving

**Table 4.** The phase effective number, error, and step height for 8, 9, 10, 11-bits with overdriving technique.

| Bit of voltage | Effective phase number | Phase error(λ) | Error reduced ratio (%) | Phase step (λ) | Step raised ratio (%) |
|---|---|---|---|---|---|
| BNS device (7) | 78 | 0.0167 | 0 | 0.0342 | 0 |
| 8 | 122 | 0.0085 | 49.1 | 0.0171 | 50.0 |
| 9 | 184 | 0.0043 | 74.3 | 0.0085 | 75.1 |
| 10 | 251 | 0.0021 | 87.4 | 0.0077 | 77.5 |
| 11 | 256 | 0.0011 | 93.4 | 0.0056 | 83.6 |

**Table 5.** Phase improvement for 10, 11-bits with and without overdriving technique.

| Bit of voltage | Effective phase number | Error improved ratio (%) | Step improved ratio (%) |
|---|---|---|---|
| 10 | 256 | 87.5 | 75.2 |
| 11 | 256 | 93.7 | 81.6 |
| Improved ratio of 11-bit to 10-bit (%) | 0 | 7.0 | 8.5 |
| 10 (overdriving) | 251 | 87.4 | 77.5 |
| 11 (overdriving) | 256 | 93.4 | 83.6 |
| Improved ratio of 11bit to10-bit (%) | 1.9 | 6.8 | 7.8 |

is increased almost 10% compared with that without overdriving; there must be a little deviation from the standard value even with same grey bit. But the change range of improved ratio for 11-bits to 10-bits is within 2% as shown in Table 5. The results still show that 10-bits is also the best choice even under overdriving technique.

## 4. Conclusions

Systematic development of fast and high accuracy LCoS-WFC device was studied here. To minimise temporal phase fluctuation caused by refreshing process, frame buffering method based on ping-pang process is explored in our designed LCoS WFC. The asynchronous refreshing time could be reduced from 55 μs to 15 μs using ping-pang frame buffering technique, and the corresponding phase fluctuation value could be reduced from 0.07 λ to 0.02 λ at λ = 633 nm. For voltage grey bit optimisation, 10-bits could provide almost full 256 linear standard values. For the LCoS device working with or without overdriving method, the phase error could be reduced by about 87%, and the phase step height is improved 75–77% compared with bought 2.8 μm LCoS device.

After systematic optimisation, the phase correcting error and the refreshing phase fluctuation are reduced by nearly one time, and the phase step accuracy is improved nearly one time compared to the 2.8 μm LCoS device. This work could obtain high accurate optimisation model for LCoS-WFC with reducing design cost and providing guidance for future improvement of LCoS-WFC.

## Disclosure statement

No potential conflict of interest was reported by the author(s).

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