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Abstract

The demand for faster and more efficient integrated photonic circuits has prompted the rise of silicon-on-insulator technology. In this paper, silicon-on-silica waveguides have been employed for the all-optical realization of a complete family of logic gates, including XOR, AND, OR, NOT, NOR, NAND and XNOR operated at 1.55 μm. This waveguide consists of three identical slots and six microring resonators, all made of silicon patterned on silica. The principle of operation of these logic gates is based on the constructive and destructive interference induced by the phase difference between the input signals. The gates' performance is evaluated against the contrast ratio (CR) metric. Compared to existing waveguides, the proposed waveguides achieve higher CRs with a speed as high as 120 Gb s^{-1}.

1. Introduction

All-optical logic gates (AOLGs) are essential elements for the optical processing of information, since they overcome the fundamental difficulties of their electronic counterparts, in particular the limited data transfer speed and bandwidth. These logic operations may serve as the basis for, or at least a component of, digital communication systems at THz frequencies as well as other complex photonic circuitry [1, 2]. Recently, silicon has been used as a basic element in making passive and active photonic devices owing to its high thermal and mechanical properties, stability, high quality, low loss and large bandwidth extending from 1.55 μm to nearly 7 μm [3]. On the other hand, owing to the high transparency of silicon in the infrared spectrum and the wide refractive index difference between silicon (~ 3.45) and silica (~ 1.46), silicon-on-insulator (SOI) waveguides exhibit unique optical features. With advancements in silicon electronic device fabrication, silicon photonic devices can now be made available by utilizing the same complementary metal-oxide-semiconductor (CMOS) platform [4], especially with the help of mature SOI technology. The development of the 6G and 7G communication era, which will enable real-time terabits per second wireless connectivity for network sensing, holographic communication, and the cognitive internet of everything, will be accelerated by the addition of silicon photonics to CMOS compatible terahertz technologies. In fact, silicon periodic waveguides [5], metal slot waveguides [6], metal-insulator-metal structures [7], gold nanowire waveguides [8], plasmonic nanoparticles [9], silicon hybrid waveguides [10], dielectric-metal-dielectric design [11], dielectric-loaded waveguides [12], photonic crystal waveguides [13], optical amplifiers [14], graphene plasmonic structures [15, 16] have all been reported to realize the AOLGs. Most of these designs have employed photonic crystals to implement one or at most two logic gates [5, 9, 10, 17–20], unlike our simple design, which implemented seven logic gates at once. And the other reported works have used noble metals such as gold and silver [6–9, 12], which are more expensive compared with the materials (i.e. silicon and silica) used in our design. Moreover, these reported schemes require complicated and extremely precise microfabrication technology. It is therefore still a significant challenge to realize multifunctional logic gates with high contrast ratios (CRs) between the output logic states '1'

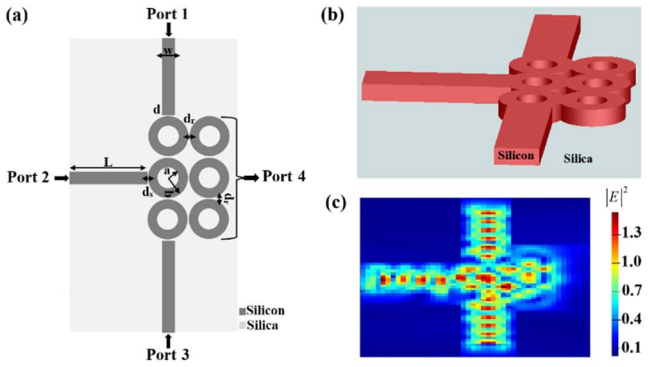

Figure 1. (a) Schematic diagram, (b) FDTD 3D view and (c) electric field intensity distributions of silicon-on-silica waveguide.

and '0' based on simple and less expensive waveguides. Additionally, the proposed design operates at a higher rate of 120 Gb s^{-1} and achieves higher CRs than reported in previous designs [6, 7, 11–13]. This helps meet the growing demands and future needs for optical logic and processing at faster speeds and with better performance. Following these steps, in this research, we design seven basic logic operations, i.e. XOR, AND, OR, NOT, NOR, NAND and XNOR, using silicon-on-silica waveguides operated at 1.55 μm. It is well known that silicon and silica exhibit negligible loss at shorter wavelengths, but at longer wavelengths, there are several multiphonon absorption peaks [21]. The proposed waveguide consists of three identical slots and six microring resonators. These logic operations are realized based on the constructive and destructive interferences between the input optical signals. With the convolutional perfectly matched layer (PML) as an absorbing boundary condition, a Lumerical finite-difference-time-domain (FDTD) simulation is run to simulate and demonstrate the operation of the proposed logic operations. The incident light will be absorbed with a minimum amount of reflections under the PML absorbing boundary conditions. However, spurious numerical reflections occur in a discretized FDTD space even when the PML is perfectly capable of absorbing incident beams. The coordinate stretching variables inside the PML might be graded to lessen these reflections [22]. The performance of these logic operations is evaluated against the contrast ratio (CR). According to the simulation results, the suggested compact waveguide can be used to realize AOLGs with higher CRs compared to previously reported structures [6, 7, 11–13].

2. Silicon-on-silica waveguide

The suggested waveguide has a silicon core patterned on a silica substrate as cladding, which is beneficial for both linear and nonlinear applications as well as optical device size control [3]. There are three input ports, which are exposed to the transverse electric mode polarized wave, and one output port on this waveguide. When the incident light is passed through the inner microrings from the strips waveguide, the light builds up in intensity over multiple round-trips owing to constructive interference and is output to the three outer microrings which serve as the output port (i.e. port 4). The light traveling through the waveguides in the microrings remains within the waveguides due to the total internal reflection phenomena. Consequently, assuming there are no losses in the system such as those due to absorption, evanescence, or imperfect coupling, the intensity of the light emitted from the outer microrings will be equal to the intensity of the light fed into the waveguide.

High spectral transmission (T) is obtained if the microring resonators and the waveguide are brought close together, as in our case. Figure 1 shows the schematic diagram, FDTD 3D view and electric field intensity distributions of a silicon on-silica waveguide.

The intensity and wavelength of the input signals are identical. The FDTD tool's intensity monitors are adjusted to record the simulation results. To determine the appropriate logic function, the threshold transmission (T_{th}) is first set to 0.26. $T = I_{out}/I_{in}$[12] is the spectral transmission, where $I_{out} = |E_{out}|^2$ is the intensity at port 4 and $I_{in} = I_1 + I_2 + I_3$ is the sum of the intensities at three input ports. When $T > T_{th}$, the logic output '1' is obtained; otherwise, the logic output is '0'. To optimize transmission, the incident beam must meet phase-matching conditions. When the incidence beams' phases are misaligned with the structure, destructive interference scatters the incident beams, resulting in a '0' output (i.e. $T < T_{th}$). To assess the logic operations' performance, the CR is employed as the metric. It is defined as $CR(dB) = 10\ ln[P^1_{mean}/P^0_{mean}]$[14], where P^1_{mean} and P^0_{mean} are the mean peak powers of logical '1' and '0', respectively. The CR is commonly defined as in our case, i.e. by taking into account the power of all output logic bits, whereas other metrics such as the extinction ratio takes into account only the peak power of the minimum and the maximum output '1' and '0', respectively.

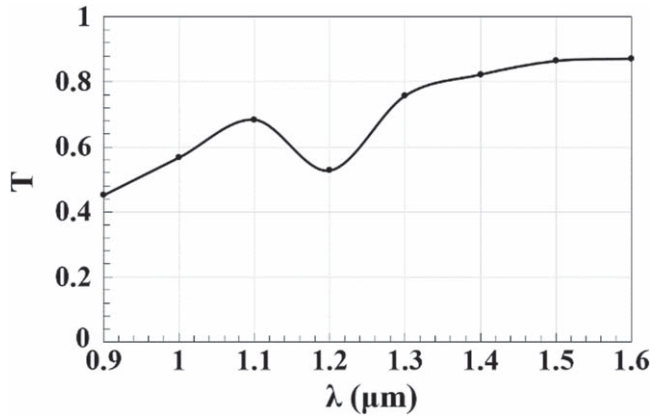

Figure 2. Spectral transmission (T) versus operating wavelength (λ) using silicon-on-silica waveguide.

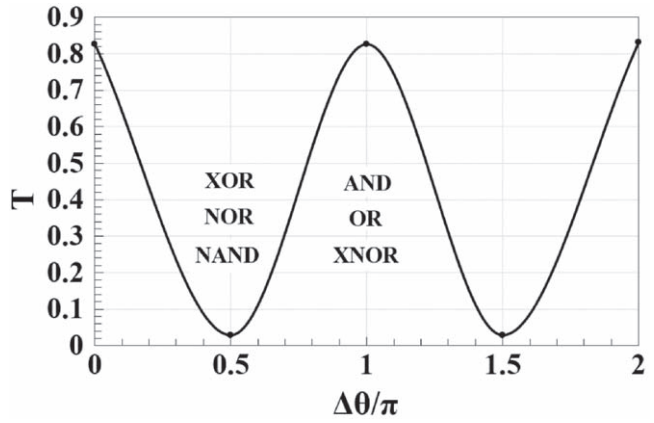

Figure 3. Spectral transmission (T) versus phase difference between two input signals ($\Delta\theta$) using silicon-on-silica waveguide.

Thus, the CR provides a better and more accurate assessment of the performance of the all-optical logic gate scheme [23]. The wavelength of the microrings resonator (λ_s) is defined as $\lambda_s = 4\pi n_{eff}\, b$, where n_{eff} is the effective refractive index and b is the radius of the outer microring [11]. All simulations were prepared and ran using FDTD with the default parameters listed in table 1.

Figure 2 shows the spectral transmission (T) as a function of the operating wavelength (λ) when the incident beams, as well as the Clk (all '1's), are launched at the three input ports with the same phase of 180°. This figure shows that the suggested waveguide achieves high T throughout a wide range of telecommunications wavelengths, from 1.3 to 1.6 μm.

Figure 3 shows the variation in T of the proposed waveguide with the phase difference between the two input signals $\Delta\theta = \theta_1$—θ_2 at 1.55 μm operating wavelength. The minimum T = 0.029 and the maximum T = 0.831 correspond to $\Delta\theta = (2n + 0.5)\pi$ and $\Delta\theta = 2n\pi$ [12], where n = 0, 1, 2,….. Thus, this figure indicates that different optical logic functions can be realized at different values of $\Delta\theta$.

For more realistic results, we have tested the design performance using different rings number of different sizes. Therefore, we optimized the size and number of rings to avoid unintended crosstalk and hence realize the considered gates with higher CRs. Figure 4 shows the dependence of the T on the ring's inner radius and rings number. It is clear from these figures that in order to achieve the proposed gates with high CRs, each slot must be assigned an inner and an outer microring with an inner radius of 0.1 μm. Accordingly, by decreasing the number of rings to less than six or increasing them to more than six, high optical losses are incurred as a direct by-product of the light scattering and absorption within the materials, which in turn reduces the CR.

The distance between the strip and inner microring (d_s) plays an important role in the proposed design in order to implement the considered logic gates with high CRs. Thus, the simulated spectral transmission (T) as a function of d_s at 1.55 μm is shown in figure 5. This figure shows that the silicon-on-silica waveguide achieves high T = 0.552 up to d_s = 40 nm. This outcome demonstrates that the suggested design could be implemented in

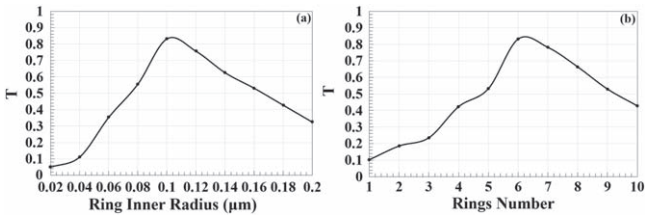

Figure 4. Spectral transmission (T) versus (a) ring inner radius and (b) rings number using silicon-on-silica waveguide at 1.55 μm.

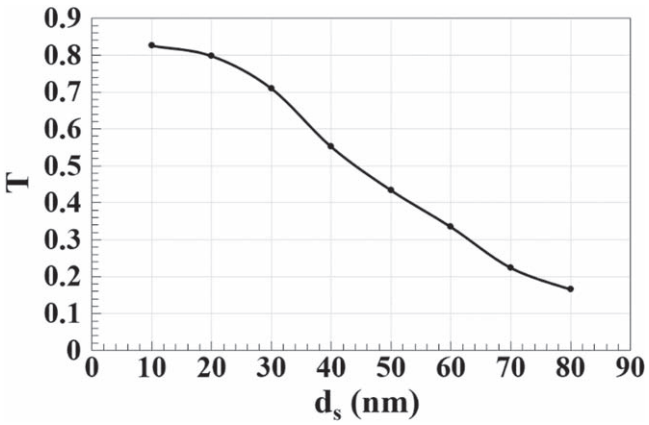

Figure 5. Spectral transmission (T) versus distance between strip and inner microring (d_s) using silicon-on-silica waveguide at 1.55 μm.

Table 1. Simulation parameters.

Symbol	Definition	Value	Unit
L	Length of stripe	1.0	μm
w	Width of stripe	0.3	μm
d	Thickness of stripe	0.3	μm
a	Inner radius of microring	0.1	μm
b	Outer radius of microring	0.22	μm
d_s	Distance between strip and inner microring	0.01	μm
Dr	Distance between microrings	0.01	μm
λ	Operating wavelength	1.55	μm
T_{th}	Threshold transmission	0.26	—

practice and transformed into a working prototype based on the specified design with the development of nanofabrication techniques in recent years, such as lithographic fabrication methods [8] and femtosecond laser direct writing technology [24–28].

3. Logic gates

3.1. XOR

A reference beam (REF) must be injected into port 2 of figure 1, and the other two beams must be launched from ports 1 and 3 in order to construct the XOR, AND, and OR logic gates. The REF, which is a series of consecutive '1', i.e. all '1's, is used here to create a reference phase difference between input signals, thereby causing constructive or destructive interference. When two input signals are '0' and '1', or vice versa (i.e. 01 or 10) and REF (all '1's) are all adjusted with the same phase of 0°, port 4 generates logical '1' due to the constructive interference between the input beams. When both ports 1 and 3 are '1' at $\theta_1 = 180°$ & $\theta_3 = 90°$ launched with

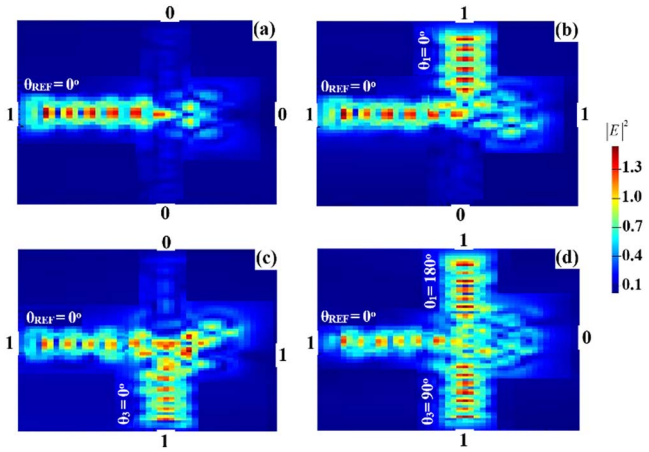

Figure 6. XOR field intensity distributions using silicon-on-silica waveguide at 1.55 μm. (a) '00' input, (b) '01' input, (c) '10' input and (d) '11' input.

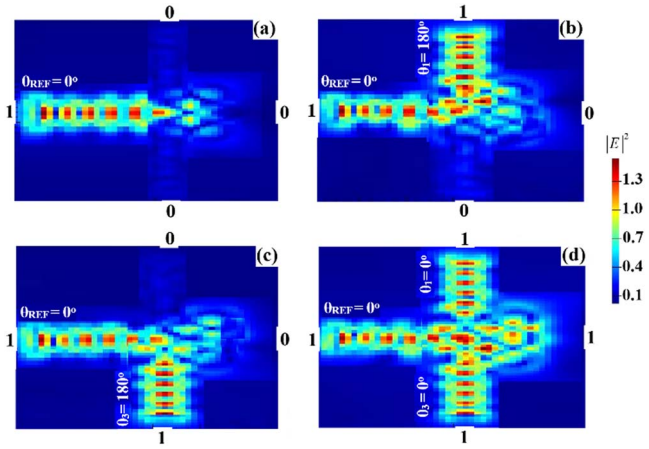

Figure 7. AND field intensity distributions using silicon-on-silica waveguide at 1.55 μm. (a) '00' input, (b) '01' input, (c) '10' input and (d) '11' input.

Table 2. XOR simulation results ($T_{th} = 0.26$).

Port 1	Port 3	Port 2 (REF)	T	Port 4	CR (dB)
0	0	1	0.029	0	23.62
0	1	1	0.524	1	
1	0	1	0.452	1	
1	1	1	0.063	0	

REF at $\theta_{REF} = 0°$, the output of port 4 produces '0' because of destructive interference between the input signals. The XOR gate is then achieved between the two input beams. Figure 6 illustrates the field intensity distributions for the logic XOR gate at 1.55 μm.

Due to the relatively slight difference between the mean peak powers of '1' and '0', a CR = 23.62 dB is obtained. The XOR simulation results are listed in table 2.

3.2. AND

The AND operation is performed by inserting two signals into ports 1 and 3, as well as the REF (all '1's) into port 2 (see figure 1). The phase angle of REF is adjusted at $\theta_{REF} = 0°$. When two signals '1' and '0', or vice versa (i.e. 01 or 10), are injected at a different phase than the REF phase, destructive interference occurs due to the phase difference between the input beams, resulting in '0' output. When both input signals are '1', port 4 provides '1'

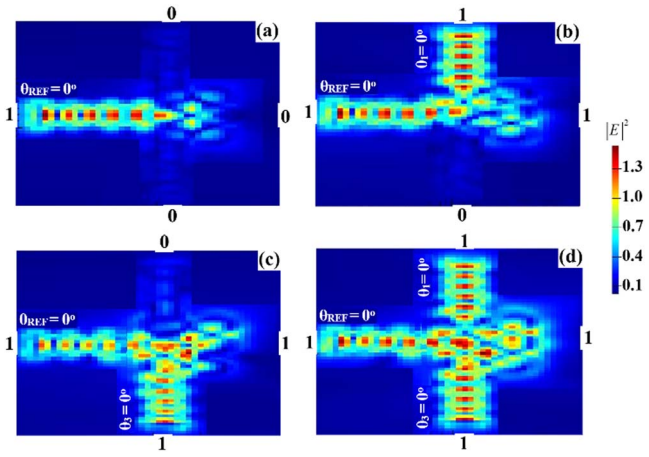

Figure 8. OR field intensity distributions using silicon-on-silica waveguide at 1.55 μm. (a) '00' input, (b) '01' input, (c) '10' input and (d) '11' input.

Table 3. AND simulation results ($T_{th} = 0.26$).

Port 1	Port 3	Port 2 (REF)	T	Port 4	CR (dB)
0	0	1	0.029	0	26.40
0	1	1	0.075	0	
1	0	1	0.073	0	
1	1	1	0.826	1	

Table 4. OR simulation results ($T_{th} = 0.26$).

Port 1	Port 3	Port 2 (REF)	T	Port 4	CR (dB)
0	0	1	0.029	0	30.33
0	1	1	0.524	1	
1	0	1	0.452	1	
1	1	1	0.831	1	

output owing to constructive interference, which occurs because the input signals and Clk have the same phase, i.e. $\theta_1 = \theta_3 = \theta_{REF} = 0°$. As a result, the AND logic operation is functionally achieved. The field intensity distributions for the logic AND gate at 1.55 μm can be seen in figure 7.

The AND simulation results with CR = 26.40 dB are summarized in table 3.

3.3. OR

In this case, two beams are supplied into the waveguide from ports 1 and 3, respectively, while the REF is supplied from port 2 (see figure 1). When only one of the OR gate's inputs is '1', the outcome is '1'. Therefore, this gate can be straightforwardly realized when all input beams propagate at the same phase, i.e. $\theta_1 = \theta_3 = \theta_{REF} = 0°$, resulting in '1' output due to constructive interference between the input beams. Figure 8 depicts the field intensity distributions for the logic OR gate using the proposed waveguide at 1.55 μm.

Table 4 displays the simulation results for the OR gate at 1.55 μm with respect to T and CR. The huge difference between the mean peak powers of logical '1' and '0' allows for a high CR = 30.33 dB.

3.4. NOT

The proposed waveguide must receive a clock light (Clk) with an angle of 180° degrees from port 1 in order to operate all inverted logic gates, including NOT, NOR, NAND, and XNOR. The Clk introduces an additional phase shift on the traveling beams, which changes the waveguide balance and results in an output. The Clk input is a series of consecutive'1', i.e. all '1's. To implement the NOT logic gate, one beam is fed into port 3 at an angle of 90°. When port 3 is set to '1', the input beams experience different phases, causing destructive interference, resulting in a logical '0' output (i.e. $T < T_{th}$). When port 3 is '0', the Clk does not experience any differencing

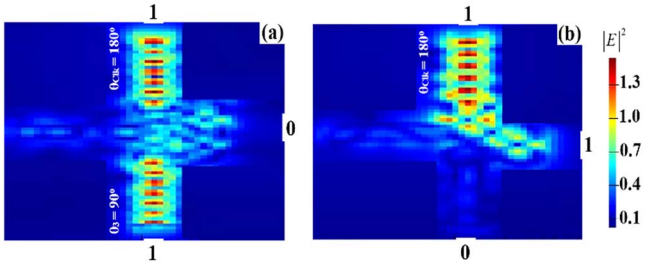

Figure 9. NOT field intensity distributions using silicon-on-silica waveguide at 1.55 μm. (a) '1' input and (b) '0' input.

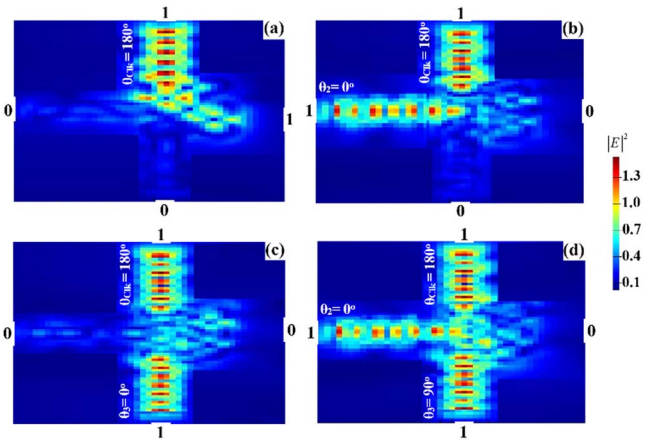

Figure 10. NOR field intensity distributions using silicon-on-silica waveguide at 1.55 μm. (a) '00' input, (b) '01' input, (c) '10' input and (d) '11' input.

Table 5. NOT simulation results ($T_{th} = 0.26$).

Port 1 (Clk)	Port 3	T	Port 4	CR (dB)
1	1	0.062	0	20.51
1	0	0.482	1	

phase, resulting in logical '1' output (i.e. $T > T_{th}$) at port 4. In this way, the NOT gate is implemented. Figure 9 shows the field intensity distributions for the NOT gate at 1.55 μm.

Table 5 summarizes the simulation results of the NOT function. These results show that the proposed waveguide can be used to form a NOT logic gate at 1.55 μm with CR = 20.51 dB.

3.5. NOR

The NOR gate produces an output '1' if and only if all inputs are '1'. In order to realize the NOR gate, the Clk is injected into port 1, while the two other beams are injected into ports 2 and 3, respectively (see figure 1). The phase angle of Clk is first set at $\theta_{Clk} = 180°$. The input beams' combination (01, 10, or 11) is injected at different angles, resulting in logical '0' at port 4 due to destructive interference. If the beams' combination (00) is launched, the Clk beam having $\theta_{Clk} = 180°$ will cancel the phase balance of the three ports, resulting in a logical '1' at port 4. The Boolean NOR logic gate is thus realized, as illustrated in figure 10.

The simulation results for the NOR gate with CR = 23.50 dB are summarized in table 6.

3.6. NAND

NAND gate (NOT-AND) produces '0' output if and only if all its inputs are '1'. The NAND gate can be realized by injecting the Clk into port 1 and the two other beams into ports 2 and 3, respectively. When ports 2 and 3 are 'OFF' (i.e. 00), the output is '1' due to the Clk having $\theta_{Clk} = 180°$. In this case, the T value is slightly above the T_{th}. When (01, 10) are launched with Clk at the same angle of 180°, constructive interference is simply happening,

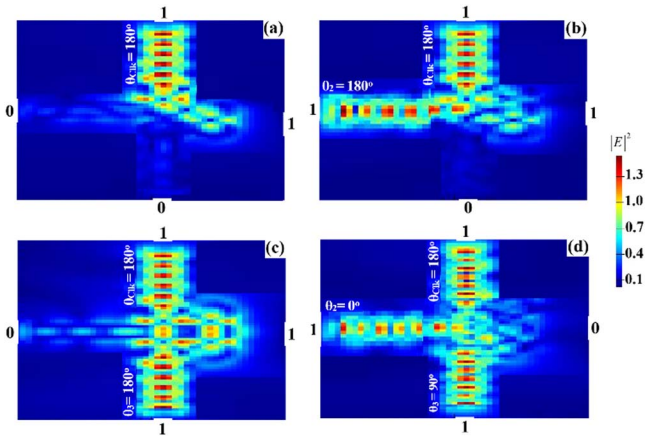

Figure 11. NAND field intensity distributions using silicon-on-silica waveguide at 1.55 μm. (a) '00' input, (b) '01' input, (c) '10' input and (d) '11' input.

Table 6. NOR simulation results ($T_{th} = 0.26$).

Port 1 (Clk)	Port 2	Port 3	T	Port 4	CR (dB)
1	0	0	0.482	1	23.50
1	0	1	0.061	0	
1	1	0	0.042	0	
1	1	1	0.035	0	

Table 7. NAND simulation results ($T_{th} = 0.26$).

Port 1 (Clk)	Port 2	Port 3	T	Port 4	CR (dB)
1	0	0	0.482	1	29.14
1	0	1	0.832	1	
1	1	0	0.452	1	
1	1	1	0.032	0	

resulting in '1' output. Whereas a destructive interference results in '0' output when (11) is launched with Clk at different phases, i.e. $\theta_2 = 0°$, $\theta_3 = 90°$ and $\theta_{Clk} = 180°$, as shown in figure 11.

Table 7 summarizes the simulation results for the NAND gate. When employing the proposed waveguide at 1.55 μm, the mean peak power of '1' is larger than that of '0', resulting in a high CR = 29.14 dB for the NAND function.

3.7. XNOR

Similar to the NOR and NAND gates, the Clk enters port 1, while the two other beams are injected from ports 2 and 3, respectively. The output port 4 generates a '1' due to constructive interference when the input beams' combination (11) is inserted along with the Clk at the same phase. For (00) combination, the Clk at 180° results in '1' output. By contrast, port 4 produces a '0' when the signals' combination (01) or (10) is launched with a different phase, as shown in figure 12.

The XNOR gate has a high CR = 25.46 dB due to the large difference in the mean peak powers of the '1' and '0' bits. Table 8 summarizes the XNOR simulation results.

The Nyquist formula, which uses the terms B for the optical bandwidth and M for the total number of signal levels, calculates the speed of a transmission system as $B\ log_2[M]$ [29]. B is defined as $B = (c/\lambda^2)\Delta\lambda$, where c is the speed of light in a vacuum, $\lambda = 1.55$ μm is the wavelength of the optical carrier and $\Delta\lambda$ is the spectral width of the signal. This indicates that the projected speed in our scenario, where B = 30 GHz and for four signal levels (00, 01, 10, 11), is 120 Gb s^{-1}.

Silicon and silica are common in the Earth's crust and are important components of the Earth's mantle. Therefore, the experimental verification of the proposed waveguide can be done based on the main outcomes of this simulation, given that the required technology is accessible. This is a technology issue that can be addressed

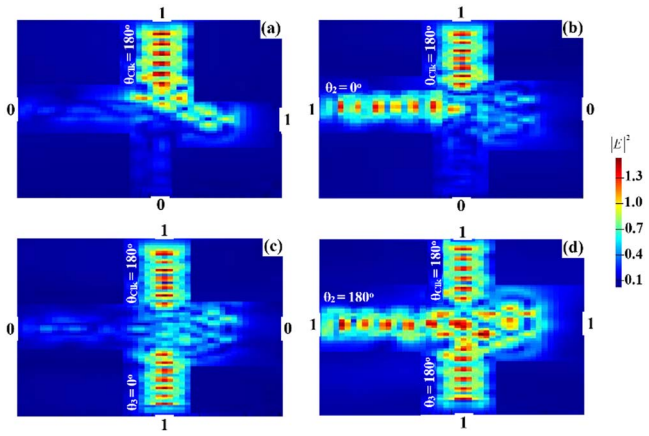

Figure 12. XNOR field intensity distributions using silicon-on-silica waveguide at 1.55 μm. (a) '00' input, (b) '01' input, (c) '10' input and (d) '11' input.

Table 8. XNOR simulation results ($T_{th} = 0.26$).

Port 1 (Clk)	Port 2	Port 3	T	Port 4	CR (dB)
1	0	0	0.482	1	25.46
1	0	1	0.061	0	
1	1	0	0.042	0	
1	1	1	0.832	1	

Table 9. Comparison of our and various reported waveguide-based designs of AOLGs at different wavelengths.

Operations	Design	wavelength (nm)	CR (dB)	References
NOT, XOR, AND, OR, NOR, NAND, XNOR	Metal slot waveguide	632.8	6–16	[6]
NOT, XOR, AND, OR, NOR, NAND, XNOR	Metal-insulator-metal structures	632.8	15	[7]
NOT, XOR, AND, OR, NOR, NAND, XNOR	Dielectric-metal-dielectric design	900 and 1330	5.37–22	[11]
XOR, AND, OR, NOR, NAND, XNOR	Dielectric-loaded waveguides	471	24.41–33.39	[12]
AND, XOR, OR, NOT, NAND, NOR XNOR	Photonic crystal waveguides	1550	5.42–9.59	[13]
XOR, AND, OR, NOT, NOR, NAND, XNOR	Silicon-on-silica waveguides	1550	20.51–30.33	This work

in practice, rather than a fundamental impediment. Design and fabrication of SOI microring resonators and slots waveguides have been experimentally reported for AOLGs [6, 8, 30–32].

Table 9 compares the proposed waveguide to various reported designs for the realization of AOLGs at different wavelengths. The suggested waveguides have higher CRs, while they are made of less expensive materials compared to other reported designs.

The proposed waveguide is more scalable, as it is simple to use to implement more combinational logic circuits such as adders and latches. Besides, the operating wavelengths can be turned on or off on demand, which allows for the easy provisioning of services and quick scaling for a growing network. The proposed waveguide is also small and light. It can typically be placed in optical computers for growth needs up to 15 to 20 years in the future. Furthermore, additional optical components can be installed later to make way for network expansion. However, the optical losses limit the scalability [33]. Thus, the losses must be minimized at the coupling interfaces between the strips and microrings by optimizing the waveguide operational parameters as in our case. The overall loss is very low (i.e. ~1.8 dB) thanks to the high spectral T that our compact waveguide emits.

4. Conclusion

Using a compact silicon-on-silica waveguide, we realized a complete family of basic Boolean operations operated at 1.55 μm. These operations were simulated using the FDTD method. The micro-waveguide consists of three identical slots and six ring resonators. The constructive and destructive interferences induced by the

phase difference of the input signals form the basis for the proper operation of these logic gates. The suggested waveguide produces higher contrast ratio values than previously reported.

Acknowledgments

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Data availability statement

The data cannot be made publicly available upon publication because they are not available in a format that is sufficiently accessible or reusable by other researchers. The data that support the findings of this study are available upon reasonable request from the authors.

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