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ABSTRACT

Owing to the advanced fabrication technology of silicon, silicon waveguides are particularly attractive for implementing all-optical signal processing devices and switches. Therefore, in this paper, a silicon-on-silica waveguide that consists of four slots arranged in the shape of letter E is proposed to be employed as the building block for simulating fundamental all-optical logic gates (AOLGs), including XOR, AND, OR, NOT, NOR, NAND, and XNOR, at 1.55 μm telecommunications wavelength. The operation concept of these logic gates relies on the constructive and destructive interference that results from the phase difference induced by optical beams that are incident on the E-shaped waveguide. The performance of the target logic gates is assessed against the contrast ratio (CR) metric. Moreover, the dependence of the spectral transmission on the device's key operating parameters is investigated and assessed. Compared to other reported designs, the results obtained by conducting simulations using the finite-difference-time-domain in lumerical commercial software show that the proposed waveguide can operate at a higher speed of 80 Gb/s and attain higher CRs of 36, 39, 35.5, 28.8, 30, 38, and 36.7 dB for logic XOR, AND, OR, NOT, NOR, NAND, and XNOR, respectively. This suggests that by using the proposed scheme, AOLGs could be realized more feasibly with greater performance and faster operation toward satisfying the present and future needs of light wave circuits and systems.

I. INTRODUCTION

The high field confinement in silicon core combined with superior miniaturization and low loss are some of the key features of using silicon waveguides for realizing integrated optical components.[1] In addition, silicon has the best crystal quality and is the least expensive of all semiconductor materials. On the other hand, all-optical logic gates (AOLGs), which overcome the fundamental barriers of their electronic counterparts, especially the limited speed of data handling and manipulation, are essential for the processing of information exclusively in the optical domain. Various schemes have been proposed to demonstrate AOLGs based on linear interference mechanisms or third order nonlinear optical effects in photonic microstructures and plasmonic nanostructures, but each has its own unique design and different features; otherwise, they would not have all been published.[2–22] However, the majority of these described devices only utilized photonic crystals to realize one or at most two logic gates,[2–12] while the proposed waveguide here realizes seven AOLGs concurrently. Furthermore, some of these reported efforts have utilized more expensive noble metals, such as gold and silver,[14–18] as opposed to silicon and silica materials. Additionally, these reported schemes demand sophisticated and precise microfabrication technology. Compared with the K-shape silicon waveguide,[22] the E-shaped silicon waveguide achieves higher contrast ratios (CRs) measured in dBs for logic XOR (i.e., 36 vs 34), AND (i.e., 39 vs 31), OR (i.e., 35.3 vs 33.73), NAND (i.e., 38 vs 34), and XNOR (i.e., 36.7 vs 31). Because of these issues, realizing multifunctional logic gates with high performance based on simple and low-cost waveguides continues to be challenging. Given this fact, in

this paper, we simulate seven AOLGs, exclusive-OR (XOR), AND, OR, NOT, NOT–OR (NOR), NOT–AND (NAND), and exclusive-NOR (XNOR), using an E-shaped silicon-on-silica optical waveguide operating at 1.55 μm telecommunications wavelength. It is generally known that silicon has a relatively low optical loss for wavelengths up to 8 μm, but silica's optical loss is increased rapidly beyond 3.6 μm.[23] Recently, silicon has been considered the preferable material of choice for systems operating in the middle infrared region, i.e., from 1.2 to 1000 μm or even higher.[24] This waveguide is made up of four slots that are arranged to form letter E. The working principle of these logic gates is based on the constructive and destructive interference incurred by the phase difference of the incident optical beams. The results obtained by conducting simulations using the finite-difference-time-domain (FDTD) method in Lumerical commercially available software show that the proposed waveguide outperforms the previously published schemes, as it can attain higher CRs of tens of dB at a higher speed of 80 Gb/s. This suggests that by exploiting the proposed scheme, AOLGs could be realized more feasibly with better performance and faster operation toward the satisfaction of present and future demands in light wave circuits and systems.

II. E-SHAPED SILICON WAVEGUIDE

The proposed waveguide consists of four identical slots arranged in the shape of letter E. An electromagnetic pulse with a transverse magnetic mode polarization at 1.55 μm excites the three input ports at an input power of 0.3 μW. Figure 1 depicts the schematic illustration, the FDTD 3D view, and the corresponding field intensity distributions of the E-shaped silicon-on-silica waveguide.

The CR, defined as $CR(dB) = 10\ln[P^1_{mean}/P^0_{mean}]$,[22] where P^1_{mean} and P^0_{mean} are the mean peak powers of the binary logic outcomes, can be used to evaluate the performance of the considered logic gates more precisely and effectively than other metrics.[25] FDTD monitors were employed to measure the electric field intensities at the input and output ports of the proposed waveguide. The output spectral transmission (T) is calculated as $T = I_{out}/I_{in} = |E_{out}|^2/|E_{in}|^2$,[18] where I_{out} is the intensity at the output port (i.e., P_{out}) and $I_{in} = I_1 + I_2 + I_3$ is the sum of the intensities at the three input ports. The initial setting of the threshold transmission (T_{th}) value is 0.15. P_{out} only produces a logical output of "1" when $T > T_{th}$ and "0" in all other circumstances. To optimize T, the incident beams must meet the phase-matching conditions.[26] On the other hand, when the phases of the incident beams and waveguides are out of phase, destructive interference scatters the incident beams and results in a "0" output. Table I lists the default parameters for the simulation of the E-shaped waveguide-based logic functions. The FDTD simulations have been run many times in order to optimize these operating parameters and obtain a higher T.

Figure 2 shows the spectral transmission (T) as a function of the operating wavelength (λ) using the proposed waveguide when the incident beams are injected at the three input ports with the same phase of 180°. This figure shows that the suggested waveguide achieves high T throughout a wide range of telecommunications wavelengths, from 1.3 to 1.6 μm.

In order to implement the considered logic gates with high CRs, the proposed design heavily relies on the angle between the short slots and long slot, which is assumed to be θ = 90° in this simulation. Thus, Fig. 3 simulates the impact of θ on the normalized spectral transmission (T) at a 1.55 μm operating wavelength. The exact value of θ is not so critical, according to this figure, and it is likely to fall between 45° and 90° with a high CR. This outcome demonstrates that the suggested design could be implemented in practice and transformed into a working prototype based on the specified design, given the 3D capabilities of the existing femtosecond laser direct writing (FLDW) technology.[27–30]

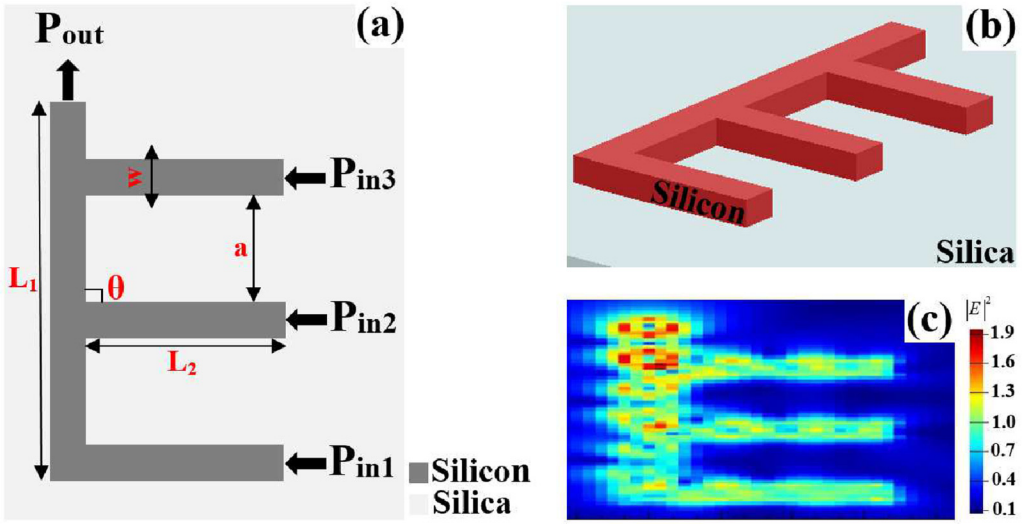

FIG. 1. (a) Schematic illustration, (b) FDTD 3D view, and (c) field intensity distributions of the E-shaped silicon waveguide.

TABLE I. Simulation parameters.

Symbol	Definition	Value	Unit
L_1	Length of long slot	2.5	μm
L_2	Length of short slot	1.0	μm
w	Width of slot	0.22	μm
d	Thickness of slot	0.3	μm
a	Distance between short slots	0.67	μm
θ	Angle between short slots and long slot	90	degree
λ	Operating wavelength	1.55	μm
T_{th}	Threshold transmission	0.15	…

Figure 4 shows the dependence of the normalized spectral transmission (T) on the distance between short slots (a). It is clear from this figure that the exact value of this parameter is not so critical and it is likely to fall between 0.5 and 0.9 μm with high CRs that lie within 0.573 and 0.575, respectively. This result confirms the feasibility of realizing the suggested waveguide in practice with the available FLDW technology.

The input power plays a central role in the waveguide performance. Therefore, Fig. 5 shows the output power as a function of the input power utilizing the proposed waveguide at 1.55 μm. It can be seen that the output power is increased as the input power gets higher and the operating input power of 0.3 μW produces an output power of 0.2 μW. This behavior will allow these silicon-based devices to carry greater optical powers than devices fabricated from polymers.[31]

III. OPERATION REALIZATION

A. XOR

For the realization of the XOR logic gate, a clock signal (Clk) is injected into input P_{in1}, while two input beams are injected into inputs P_{in2} and P_{in3} of Fig. 1. A Clk (all "1"s) introduces an additional phase shift to the propagating beams, altering the waveguide balance and producing the desired output function. When all input beams are injected at the same phase, constructive interference occurs, but destructive interference happens when they are launched at a different phase. As a result, P_{out} produces a "1" output due to the constructive interference between the two input beams when their combination (01 or 10) is launched along with the Clk beam at the same phase (i.e., $\Phi_2 = \Phi_3 = \Phi\text{Clk} = 180°$). The injection beams interact destructively, generating T < Tth (meaning "0" output) when the combination (11) is injected into the proposed waveguide together with Clk at various phases (i.e., $\Phi_2 = 90°$, $\Phi_3 = 0°$, and $\Phi\text{Clk} = 180°$). The XOR field intensity distributions employing an E-shaped silicon-on-silica waveguide at 1.55 μm are shown in Fig. 6.

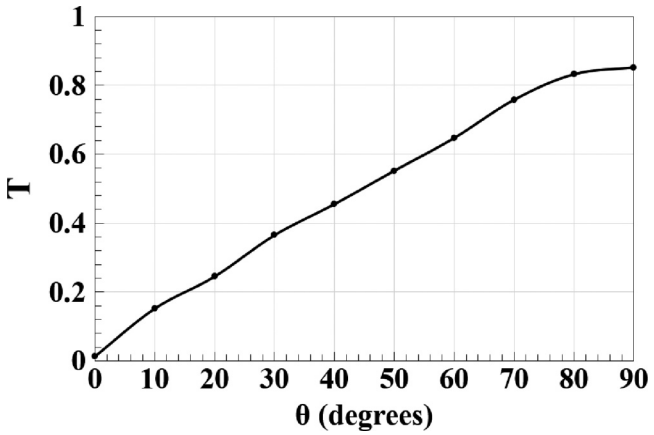

FIG. 3. Normalized spectral transmission (T) vs angle between short slots and long slot (θ) using the E-shaped silicon waveguide at 1.55 μm.

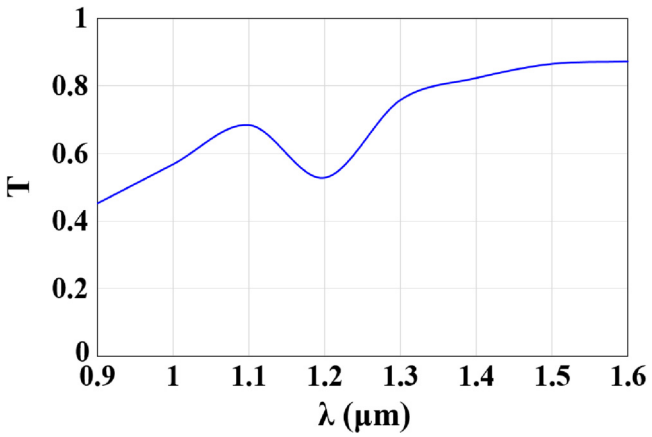

FIG. 2. Spectral transmission (T) vs operating wavelength (λ) using the E-shaped silicon waveguide.

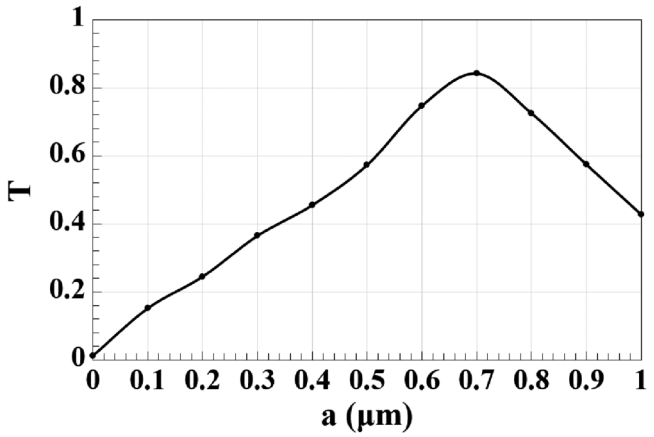

FIG. 4. Normalized spectral transmission (T) vs distance between short slots (a) using the E-shaped silicon waveguide at 1.55 μm.

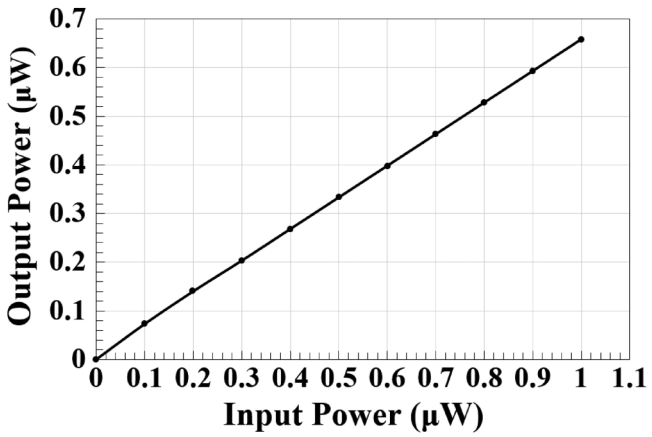

FIG. 5. Output power vs input power using the E-shaped silicon waveguide at 1.55 μm.

The proposed waveguide achieves a high CR = 36 dB due to a significant difference between the mean peak powers of "1" and "0." Table II lists the XOR simulation results using an E-shaped silicon-on-silica waveguide at 1.55 μm.

B. AND

Similar to the XOR gate, both input beams are, respectively, inserted into P_{in2} and P_{in3}, together with a Clk beam (all "1"s) into P_{in1} (see Fig. 1). When all incident beams are released into the proposed waveguide at the same phase (i.e., $\Phi_2 = \Phi_3 = \Phi_{Clk} = 180°$), P_{out} generates "1" output due to constructive interference. In contrast, due to destructive interference, P_{out} outputs a "0" when these incident beams are injected at a different phase. In this manner, the AND gate is realized. Using an E-shaped silicon-on-silica waveguide at 1.55 μm, the AND field intensity distributions are displayed in Fig. 7.

The suggested waveguide at 1.55 μm results in a high CR = 39 dB. Table III presents the results of the AND simulation.

C. OR

The outcome of the P_{out} is "1" when the combination of input beams (01, 10, or 11) is inserted with Clk at the same phase of 180°. This results in the realization of the OR logic gate between the two input beams. The OR field intensity distributions utilizing the suggested waveguide at 1.55 μm are shown in Fig. 8.

Because of the significant difference in the mean peak powers between "1" and "0," the suggested waveguide achieves a high CR of 35.3 dB. In terms of T and CR, Table IV summarizes the results of the OR simulation at 1.55 μm.

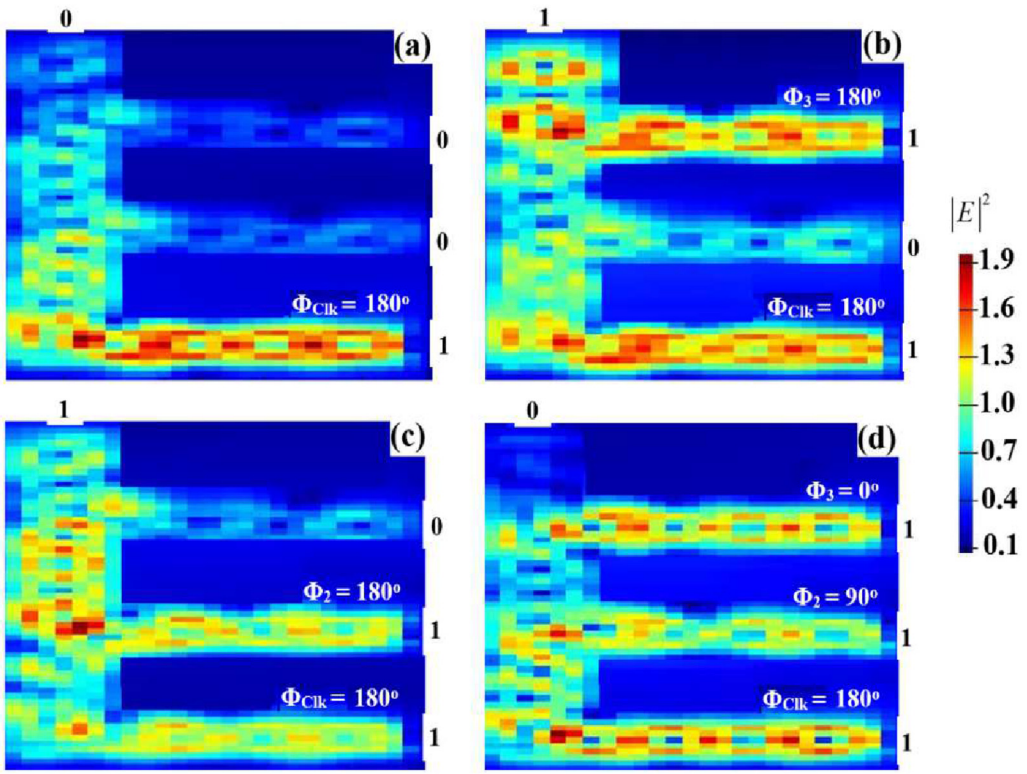

FIG. 6. XOR field intensity distributions using the E-shaped silicon-on-silica waveguide at 1.55 μm. (a) "00" input, (b) "01" input, (c) "10" input, and (d) "11" input.

TABLE II. XOR simulation results (T_{th} = 0.15).

P_{in1} (Clk)	P_{in2}	P_{in3}	I_{out}	T	P_{out}	CR (dB)
1	0	0	0.007	0.023	0	36
1	0	1	0.256	0.852	1	
1	1	0	0.203	0.675	1	
1	1	1	0.005	0.018	0	

The XOR, AND, and OR logic gates cannot be implemented without the Clk. Using the recommended waveguide at 1.55 μm, we evaluate the performance of these three gates in terms of CR in the presence of the Clk (i.e., Clk = "1") and absence of it, meaning that there is no input light injected into P_{in1}. Table V demonstrates the need for the Clk in order to get higher CRs.

D. NOT

All inverted logic gates, such as NOT, NOR, NAND, and XNOR, are executed by sending a clock light (Clk) with an angle of 0° into the suggested waveguide from P_{in3}, as shown in Fig. 1. To implement the NOT gate, one beam is injected into P_{in1} at an angle of 180°. When P_{in1} is set to "1," P_{out} generates a logical "0" (i.e., $T < T_{th}$) due to the destructive interference that happens as a result of the different phase conditions of the input beams. The Clk (all "1"s) outputs a logical "1" (i.e., $T > T_{th}$) at P_{out} when P_{in1} is set to "OFF." The NOT gate is performed in this way. Figure 9 depicts the NOT field intensity distributions at 1.55 μm employing an E-shaped silicon-on-silica waveguide.

For NOT gate, the proposed waveguide yields a high CR = 28.8 dB. The results of the NOT simulation utilizing the suggested waveguide at 1.55 μm are listed in Table VI.

E. NOR

The NOR (NOT–OR) operation is carried out by two beams launched into P_{in1} and P_{in2}, while P_{in3} is launched with Clk (all 1's) (see Fig. 1). Destructive interference causes a logical "0" at P_{out} when the input beams (01, 10, or 11) are combined and injected at

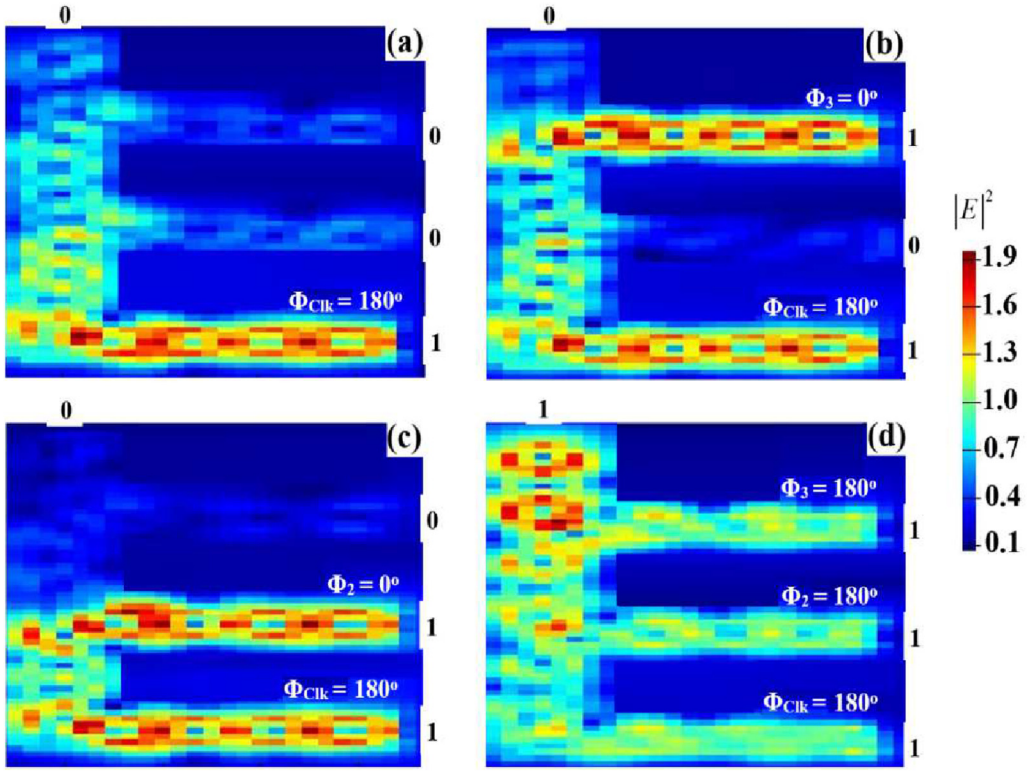

FIG. 7. AND field intensity distributions using the E-shaped silicon-on-silica waveguide at 1.55 μm. (a) "00" input, (b) "01" input, (c) "10" input, and (d) "11" input.

TABLE III. AND simulation results (T_{th} = 0.15).

P_{in1} (Clk)	P_{in2}	P_{in3}	I_{out}	T	P_{out}	CR (dB)
1	0	0	0.007	0.023	0	39
1	0	1	0.005	0.016	0	
1	1	0	0.004	0.012	0	
1	1	1	0.256	0.852	1	

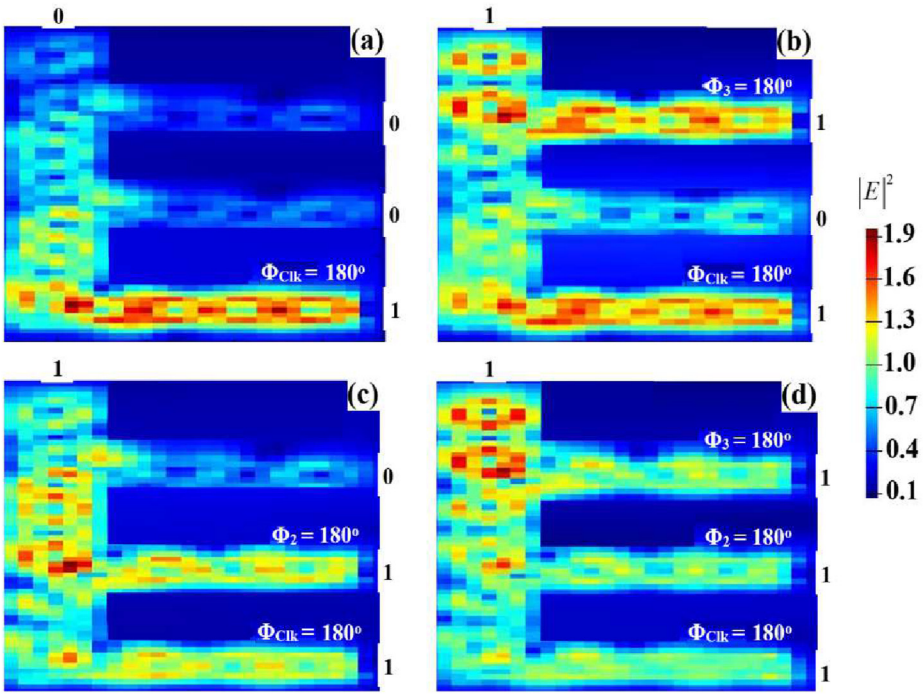

FIG. 8. OR field intensity distributions using the E-shaped silicon-on-silica waveguide at 1.55 μm. (a) "00" input, (b) "01" input, (c) "10" input, and (d) "11" input.

TABLE IV. OR simulation results (T_{th} = 0.15).

P_{in1} (Clk)	P_{in2}	P_{in3}	I_{out}	T	P_{out}	CR (dB)
1	0	0	0.007	0.023	0	35.3
1	0	1	0.248	0.826	1	
1	1	0	0.203	0.675	1	
1	1	1	0.256	0.852	1	

TABLE V. CR with and without REF.

Gate	CR (dB) with Clk	CR (dB) without Clk
XOR	36	7.4
AND	39	8.2
OR	35.3	7.3

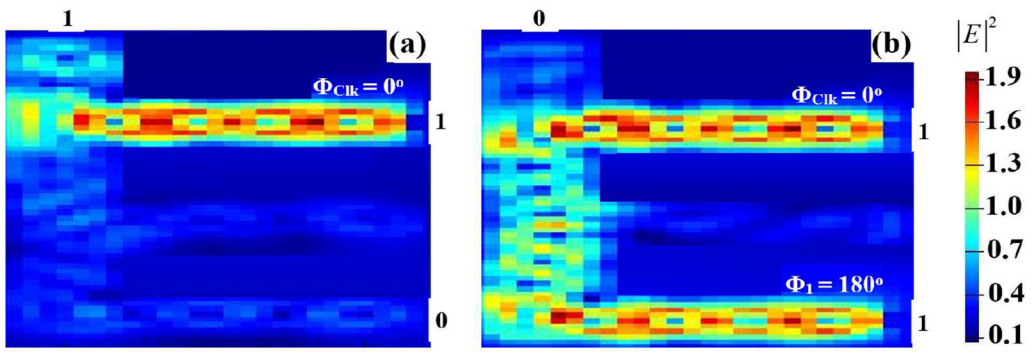

FIG. 9. NOT field intensity distributions using the E-shaped silicon-on-silica waveguide at 1.55 μm. (a) "0" input and (b) "1" input.

TABLE VI. NOT simulation results (T_{th} = 0.15).

P_{in1}	P_{in3} (Clk)	I_{out}	T	P_{out}	CR (dB)
0	1	0.086	0.285	1	28.8
1	1	0.005	0.016	0	

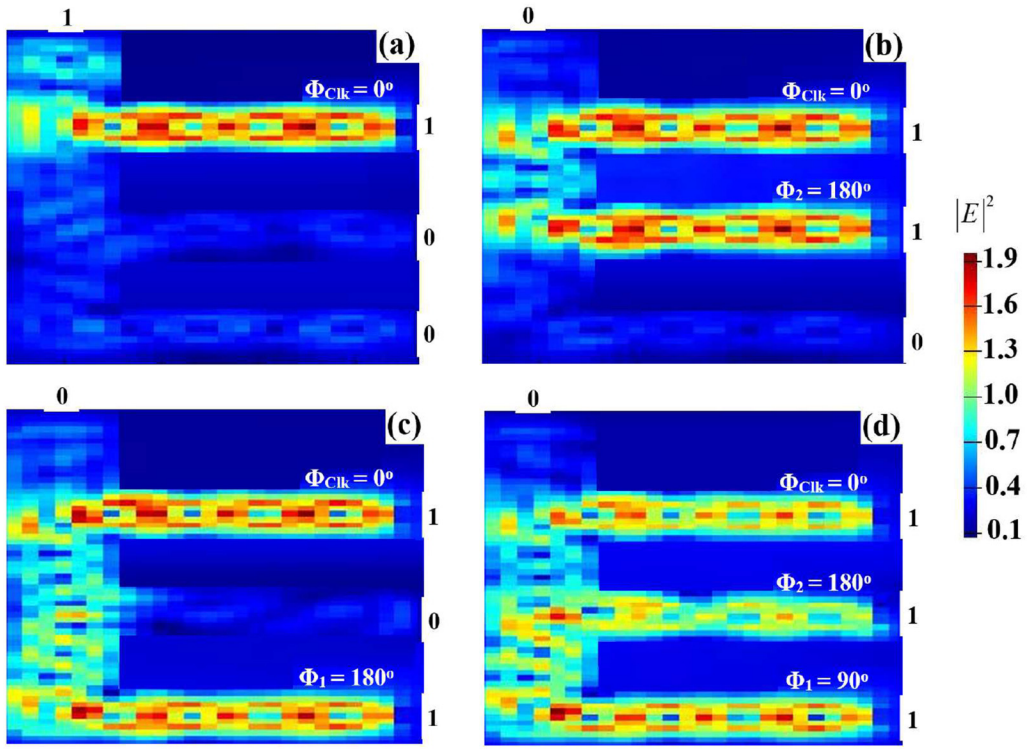

FIG. 10. NOR field intensity distributions using the E-shaped silicon-on-silica waveguide at 1.55 μm. (a) "00" input, (b) "01" input, (c) "10" input, and (d) "11" input.

TABLE VII. NOR simulation results (T_{th} = 0.15).

P_{in1}	P_{in2}	P_{in3} (Clk)	I_{out}	T	P_{out}	CR (dB)
0	0	1	0.086	0.285	1	30
0	1	1	0.004	0.013	0	
1	0	1	0.005	0.016	0	
1	1	1	0.004	0.014	0	

different angles. The phase balance of the inputs will be canceled by the Clk having $\Phi_{Clk} = 0°$ if the beams' combination (00) is launched, resulting in a logical "1" at P_{out}. As a result, the NOR gate is realized, as shown in Fig. 10.

Due to the significant difference between P^1_{mean} and P^0_{mean}, the suggested waveguide achieves a high CR = 30 dB for the NOR gate. Table VII contains an overview of the simulation results for this gate.

F. NAND

By injecting the Clk into P_{in3} and the other two beams into P_{in1} and P_{in2}, respectively, the NAND (NOT–AND) gate can be created. The phase balance of the three inputs is canceled by the Clk with $\Phi_{Clk} = 0°$, making P_{out} become "1" when P_{in1} and P_{in2} are both "OFF" (i.e., 00). When Clk and (01, 10) are launched at the same angle of 0°, constructive interference simply happens, producing an output of "1." As shown in Fig. 11, when (11) is launched with Clk at different phases, such as $\Phi_1 = 90°$, $\Phi_2 = 180°$, and $\Phi_{Clk} = 0°$, a "0" output is generated.

Table VIII provides a summary of the NAND simulation results using the recommended waveguide, which produces a high CR of 38 dB at 1.55 μm.

G. XNOR

The XNOR (exclusive-XOR) gate is created by the Clk entering P_{in3} in a manner similar to the NOR and NAND gates, with the other two beams coming from P_{in1} and P_{in2}, respectively. When the combination of the incident beams (11) is introduced

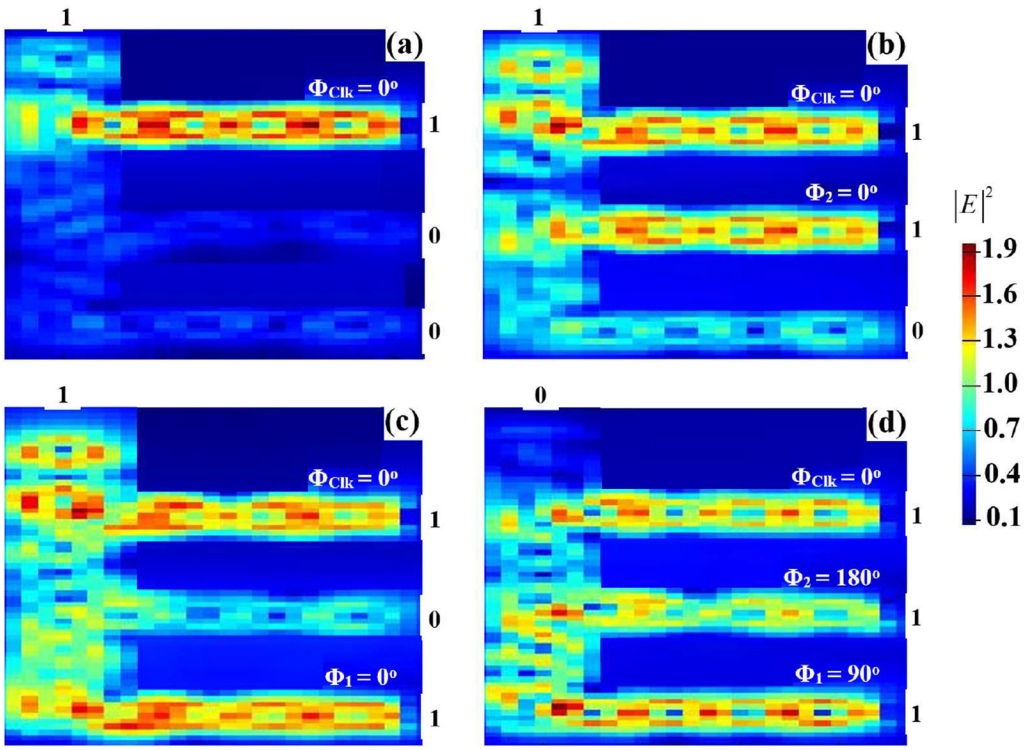

FIG. 11. NAND field intensity distributions using the E-shaped silicon-on-silica waveguide at 1.55 μm. (a) "00" input, (b) "01" input, (c) "10" input, and (d) "11" input.

TABLE VIII. NAND simulation results (T_{th} = 0.15).

P_{in1}	P_{in2}	P_{in3} (Clk)	I_{out}	T	P_{out}	CR (dB)
0	0	1	0.086	0.285	1	38
0	1	1	0.227	0.755	1	
1	0	1	0.248	0.826	1	
1	1	1	0.004	0.014	0	

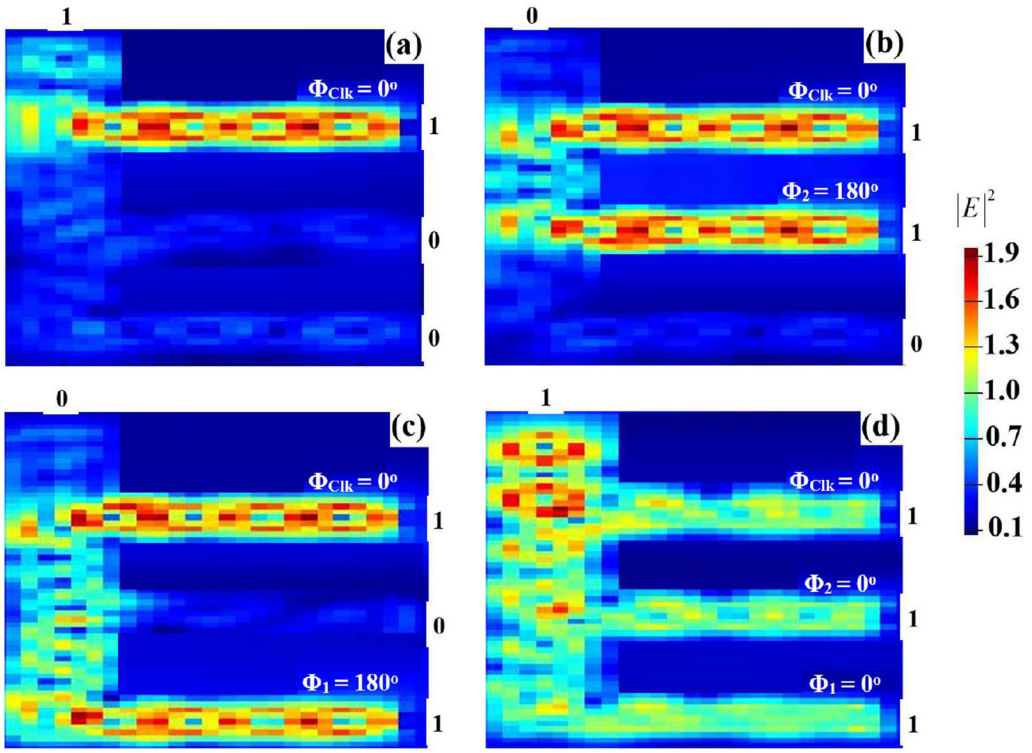

FIG. 12. XNOR field intensity distributions using the E-shaped silicon-on-silica waveguide at 1.55 μm. (a) "00" input, (b) "01" input, (c) "10" input, and (d) "11" input.

TABLE IX. XNOR simulation results (T_{th} = 0.15).

P_{in1}	P_{in2}	P_{in3} (Clk)	I_{out}	T	P_{out}	CR (dB)
0	0	1	0.086	0.285	1	36.7
0	1	1	0.004	0.013	0	
1	0	1	0.005	0.016	0	
1	1	1	0.256	0.852	1	

TABLE X. Concise comparison of proposed and other waveguide-based designs of AOLGs.

Operations	Design	Wavelength (nm)	CR (dB)	Reference
AND, XOR, OR	T-shaped photonic crystal waveguides	1550	8.29–33.05	5–7
AND, NOR, XNOR	Si photonic platform	1550	>10 dB	11
AND, XOR, OR, NOT, NAND, NOR XNOR	Photonic crystal waveguides	1550	5.42–9.59	13
NOT, XOR, AND, OR, NOR, NAND, XNOR	Metal slot waveguide	632.8	6–16	15
NOT, XOR, AND, OR, NOR, NAND, XNOR	Metal–insulator–metal structures	632.8	15	16
NOT, XOR, AND, OR, NOR, NAND, XNOR	Dielectric–metal–dielectric design	900 and 1330	5.37–22	17
XOR, AND, OR, NOR, NAND, XNOR	Dielectric-loaded waveguides	471	24.41–33.39	18
XOR, AND, OR, NOT, NOR, XNOR, NAND	K-shaped silicon waveguides	1550	30.5–34	22
XOR, AND, OR, NOT, NOR, XNOR, NAND	E-shaped silicon waveguides	1550	28.8–39	This work

with the Clk at the same phase of 0°, constructive interference causes P_{out} to emit a "1." In contrast, as shown in Fig. 12, P_{out} generates a "0" when the combination of the input beams (01) or (10) is launched with a different phase.

Table IX lists the results of the XNOR simulation with a high CR = 36.7 dB using the suggested waveguide.

The demand for data centers and high-performance computing is growing as big data and the Internet of Things are being rapidly developed. For high-speed datacom interconnects between multi-cores or local/distant caches, a very large link capacity is required. Conventional electrical interconnects, on the other hand, suffer from constrained bandwidth and high power consumption, making it increasingly challenging for them to meet the always expanding capacity demands. In order to increase power efficiency, reduce latency, and boost capacity, photonic integrated circuits have been developed in response to the demand for high-capacity, dependable, and affordable optical data networks. It will be impossible to afford the considerably increased complexity of next-generation high-capacity data communication systems by merely increasing the number of discrete optical channels. Optoelectronic technology based on silicon has enormous potential for the future since it can considerably enhance integration density while lowering cost and energy usage. The ability to use complementary metal–oxide–semiconductor-compatible fabrication, which allows for high-volume production at low cost, is the main driving force behind silicon photonics.[32,33] To this aim, the amount of information that can be transmitted through silicon is important and was estimated here through $B \log_2[1 + SNR]$.[34] B is the optical bandwidth, $B = (c/\lambda^2)\Delta\lambda$, where c is the speed of light in vacuum, $\lambda = 1.55\,\mu m$ is the optical carrier wavelength and $\Delta\lambda$ is the spectral width of the signal. SNR is the signal-to-noise ratio, $SNR = P_{out}/kTB$,[34] where P_{out} is the total output power, k is Boltzmann's constant, and T is the absolute temperature. Thus, for B = 6.24 GHz, $P_{out} = 0.2\,\mu W$, and T = 295 K in our case, the calculated speed is more than 80 Gb/s. To further increase the device's operating speed, a reverse bias p–i–n junction can be built across the waveguide.[35]

The suggested waveguide can be made more easily and more affordably, thanks to the availability of silicon and silica components. As a result, provided the required technology is available and the main conclusions of this simulation are accurate, the suggested waveguide may be experimentally verified. FLDW technology is currently used as a key implementation technique for photonic integrated circuit fabrication strategies because of its mask-free, efficient, and three-dimensional capabilities.[27–30] On the other hand, several logic operations have been experimentally accomplished using a variety of waveguides.[6,8,9,36,37] For the whole experimental setup for building logical operations, additional components such as laser sources, couplers, fibers, phase shifters, amplifiers, and filters should certainly be required.[38–40]

Table X compares the proposed waveguide's ability to perform logic operations at various wavelengths to that of other waveguide designs that have been reported for the same purpose. From the information provided in this table, it can be deduced that the proposed scheme can achieve the target logic operations with comparatively better performance and faster speed in a practically feasible manner.

IV. CONCLUSION

In conclusion, a suite of fundamental logic gates, including XOR, AND, OR, NOT, NOR, NAND, and XNOR, was theoretically demonstrated at 1.55 μm telecommunications wavelength using properly driven E-shaped silicon-on-silica waveguides. Lumerical FDTD solutions obtained in commercially available software were used to simulate these logic functions. The constructive and destructive interference produced by the phase difference of the input beams is the key for the proper realization of these logic gates. The suggested E-shaped waveguide operates at a higher speed of 80 Gb/s and achieves higher CRs compared to the other reported waveguides. Moreover, the simulated outcomes demonstrate that the suggested scheme could be implemented in practice and transformed into a working prototype based on the specified design, given the 3D capabilities of the existing relevant technologies. Therefore, the proposed scheme can constitute a viable technological option for the implementation of these gates, with subsequent operational and practical benefits in applications where these gates are employed as the core building blocks.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Amer Kotb: Conceptualization (equal); Data curation (equal); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Methodology (equal); Resources (equal); Software (equal); Validation (equal); Visualization (equal); Writing – original draft (equal). **Kyriakos E. Zoiros:** Data curation (equal); Formal analysis (equal); Investigation (equal); Validation (equal); Writing – review & editing (equal). **Chunlei Guo:** Project administration (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available within the article.

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