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2 × 2 Compact Silicon Waveguide-Based Optical Logic Functions at 1.55 µm

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Abstract: Compact waveguide crossing is a fundamental component of optoelectronic fusion chip solutions due to its orders-of-magnitude smaller footprint than that of conventional photonic integrated circuits. In this paper, we suggest 2 × 2 compact silicon-on-silica waveguides that can implement all of the fundamental Boolean logic functions, including XOR, AND, OR, NOT, NOR, XNOR, and NAND, operated at 1.55 µm. Three input waveguides, one output waveguide, and a design area compose the proposed waveguide. The execution of the specified logic gates relies on the constructive and destructive interferences produced by the phase variations between the input beams. The contrast ratio (CR) is employed as a performance metric to assess how well these logic functions operate. In comparison to other reported designs, the proposed waveguide achieves higher CRs at a high speed of 120 Gb/s.

Keywords: logic functions; waveguide crossing; contrast ratio

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1. Introduction

The need for computational resources has grown significantly in today's information society, and the density of conventional integrated circuit transistors is reaching its physical limit. In the past decade, there has been considerable growth in the field of integrated photonics, particularly in the area of silicon photonics, due to the high transmission efficiency, low power consumption, affordable and dense integration, and compatibility with complementary metal–oxide–semiconductor (CMOS) manufacturing processes [1]. Since the inception of silicon photonics in the telecommunications industry, many applications that are based on this platform have grown to include sensing, optomechanics, nonlinear optics, quantum optics, and even neuroscience. On the other hand, optoelectronic and photonic devices and circuits based on silicon-on-insulator (SOI) are appealing because they can be fabricated using the CMOS process and have the potential for monolithic integration on CMOS chips. SOI is produced by depositing a thin layer of crystalline silicon on a silica (silicon dioxide) insulating layer. Moreover, the SOI waveguide crossing is a crucial device unit to create a variety of implementation schemes, such as shaped taper waveguide crossing [2–5], multimode interferometers [6–8], and photonic crystal waveguide crossing [9,10]. However, low insertion loss was reported using these structures, especially in 2 × 2 [2], but large crossings are unattractive for large-scale photonic interconnects. All-optical Boolean functions, on the other hand, are essential elements for information optical processing because they efficiently overcome the fundamental restrictions of their electronic equivalents, particularly the constrained data transfer speed and bandwidth. Recently, a variety of optical waveguides have been employed to implement all-optical Boolean functions [11–22]. However, the majority of these described devices have used photonic crystal structures or are constructed from noble costly metals to implement only

one, or at most two, logic operations. Furthermore, these reported schemes necessitate highly accurate and advanced microfabrication technologies. Due to these impediments, it is still difficult to implement multifunctional logic functions with high performance using simple and inexpensive waveguides. Therefore, in this paper, we propose compact 2 × 2 silicon-on-silica waveguides to realize seven basic Boolean logic functions, i.e., XOR, AND, OR, NOT, NOR, XNOR, and NAND, operated at the 1.55 µm telecommunications wavelength. The proposed waveguide consists of three input waveguides, one output waveguide, and a design area. Based on the constructive and destructive interference produced by the phase differences between the input beams, the considered logic functions operate. By employing Lumerical finite-difference-time-domain (FDTD) simulation tools, the contrast ratio (CR) is calculated to evaluate how effectively the logic functions work. Through comparison of the outcomes with other reported designs [11–22], it is shown that the proposed design exhibits higher CRs at a high speed of 120 Gb/s.

2. 2 × 2 Silicon Waveguide

The proposed waveguide comprises a silicon core that is printed on a silica substrate as cladding, which is advantageous for controlling the size of optical devices as well as for linear and nonlinear applications [1]. This waveguide has three input ports that are open to transverse electric mode polarized waves, one output port, and a design area. The design area measures 2 µm by 0.6 µm, the top and lower arms are separated by 4 µm, and the width of the input and output arms are both set to 0.4 µm. The coupling gap between the top and lower arms is 0.1 µm, and the bend radius is 2 µm. The total waveguide cross-section area is 6 × 4.8 µm^2. The input beams have the same wavelength and intensity. A schematic diagram of the 2 × 2 silicon waveguide and the light field distributions are displayed in Figure 1.

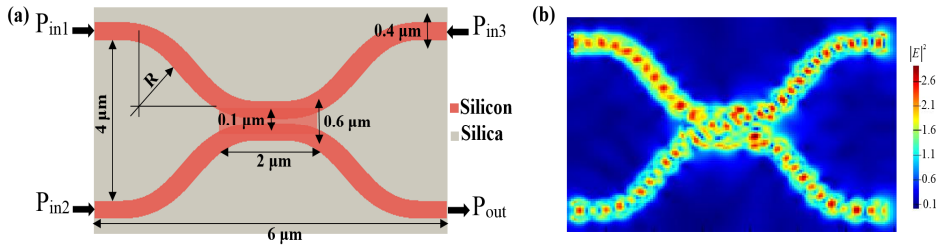

Figure 1. (**a**) Schematic diagram and (**b**) light field distributions of 2 × 2 silicon waveguide.

The threshold transmission (T_{th}) value is initially set to 0.14, which is the minimum normalized power required to generate the spectral transmission (T). $T = I_{out}/I_{in}$, where $I_{out} = |E_{out}|^2$ is the intensity at P_{out} and $I_{in} = |E_{in}|^2 = I_1 + I_2 + I_3$ is the sum of the intensities at three input ports [15]. The intensity monitors of the FDTD are set to record the simulation findings. The logic output is '1' when $T > T_{th}$; otherwise, the output is '0' (i.e., $T < T_{th}$). The incident beams must match in phase to maximize T. The destructive interference scatters the incident beams when the phases of the incident beams are out of phase with the waveguide, producing a '0' output. The CR described by $CR(dB) = 10\,ln\left[P^1_{mean}/P^0_{mean}\right]$ [19,20], where P^1_{mean} and P^0_{mean} are the mean peak powers of outputs '1' and '0', respectively, is employed to evaluate the performance of the considered logic functions better and more accurately than other metrics [23].

Figure 2 depicts the spectral transmission (T) and the loss versus the operating wavelength (λ) when the input beams are injected at the three input ports with the same phase of 0°. Due to the constructive interference between the input beams utilizing the suggested waveguide, a high T of 0.865 and a low loss of 0.63 dB/µm are achieved. The scattering at the interfaces between the slots and the design area and the material absorption are responsible for these negligible propagation losses. Moreover, this graph demonstrates that our waveguide generates a high T and a low loss across the entire range of exploitable telecommunication wavelengths, i.e., 1.3–1.6 µm.

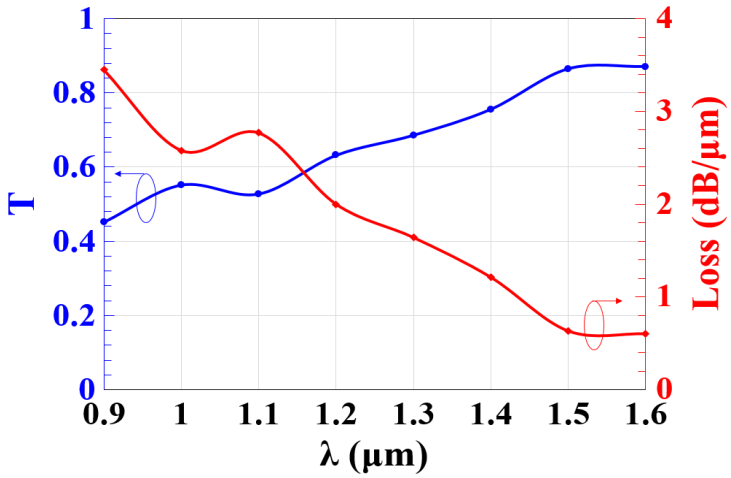

Figure 2. Spectral transmission (T) and loss versus operating wavelength (λ) utilizing 2 × 2 silicon waveguide.

The design area, which controls the coupling gap between the upper and the lower waveguide's arms, is essential for the suggested design to achieve the considered logic functions with high CRs. Therefore, Figure 3 illustrates the simulation of the effect of the design area's volume on the normalized spectral transmission (T) at 1.55 μm. This figure shows that the maximum T occurs between 0.40 and 0.60 μm^3, which gives flexibility in the practical implementation of the suggested design. A closer look at this figure reveals that by varying the design area's volume, the light scattering and absorption within the materials increase, which, in turn, causes higher losses.

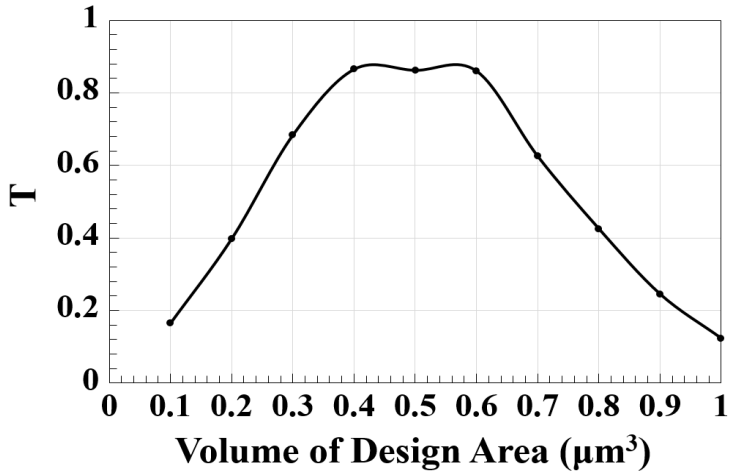

Figure 3. Spectral transmission (T) versus volume of design area utilizing 2 × 2 silicon waveguide at 1.55 μm.

The process variations, such as those in waveguide thickness, etching depth, waveguide width, and material refractive indices, result in phase errors that introduce uncertainty in the responses of photonic devices [24–26]. Therefore, it is necessary to study the effect of the phase error on the performance of the logic operations. Figure 4 shows the dependence of the normalized spectral transmission (T) on the phase error utilizing the 2 × 2 silicon waveguide at 1.55 μm. This figure shows that by increasing the amount of phase error, T is decreased, which, in turn, reduces the CR.

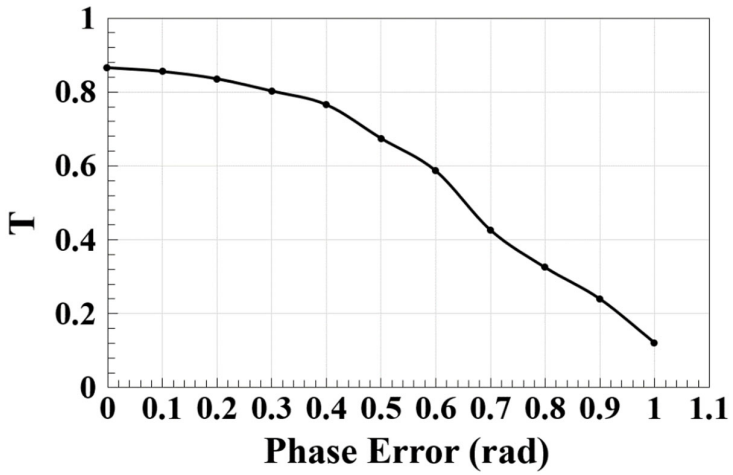

Figure 4. Spectral transmission (T) versus phase error utilizing 2 × 2 silicon waveguide at 1.55 μm.

The top and lower waveguide arms are separated by a gap of 4 μm. This gap plays a central role in the waveguide performance. Therefore, Figure 5 shows the relation between the spectral loss and the gap between the waveguide arms utilizing the proposed 2 × 2 waveguide crossing at 1.55 μm. It can be seen that the loss deteriorates with the widening of the separated gap. This happens because if the separated gap is increased, the upper and lower waveguide arms move away from their convergence point at the design area, which induces no interferences between the incoming beams, and thus naturally results in a loss increase.

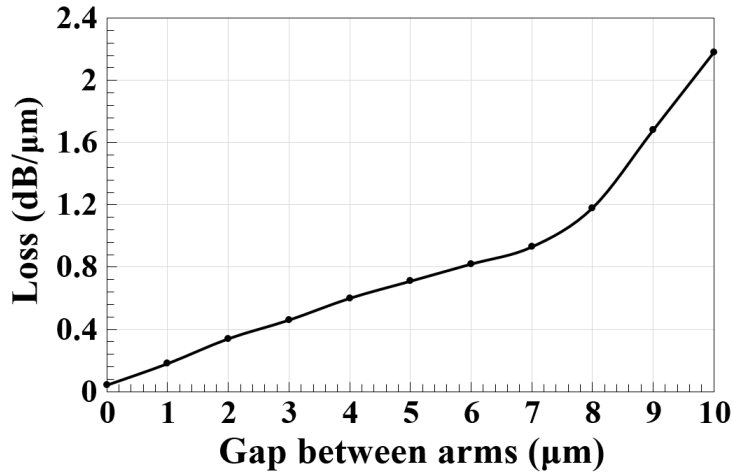

Figure 5. Spectral loss versus gap between waveguide arms utilizing 2 × 2 silicon waveguide at 1.55 μm.

The bending radiation losses are caused by the coupling of light from core modes to cladding modes when the optical waveguides/fibers are bent. These losses must be simulated correctly as they critically affect the device's performance. Therefore, Figure 6 shows the bending loss as a function of the bend radius (R) using the proposed waveguide at 1.55 μm. The form of the obtained curve agrees well with the trend that bending losses increase for smaller R. Accurate measurements of bending losses in silicon waveguides with submicron dimensions fabricated on SOI wafers that experimentally verify this fact are reported in [27,28].

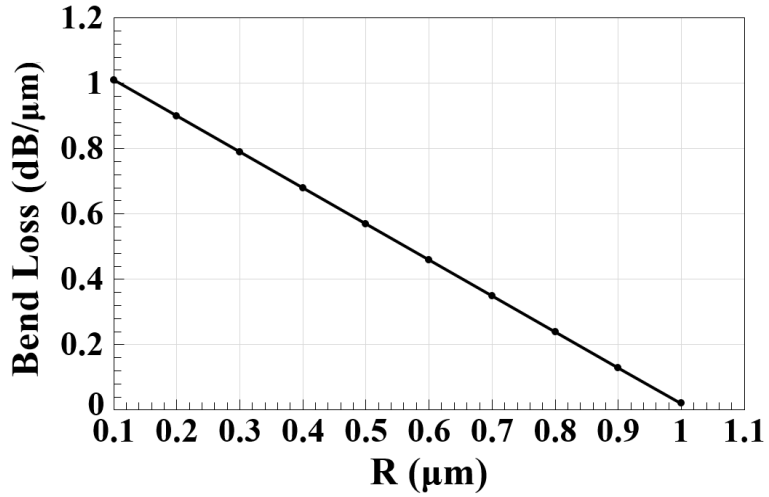

Figure 6. Bending radiation loss versus bend radius (R) utilizing 2 × 2 silicon waveguide at 1.55 μm.

Realizing a highly flat and low dispersion over a broad wavelength range is a key challenge for integrated waveguides. Dispersion flattening has proven to be a challenge for silicon waveguides due to the tight light confinement and severe waveguide dispersion in the highly nonlinear integrated waveguides. Additionally, it may be advantageous to reduce phase mismatching and eliminate the need for high pump power in nonlinear processes by optimizing the dispersion profile in silicon waveguides [29]. The transverse size of silicon strip and rib waveguides would need to be quite large to produce one zero-dispersion wavelength in the desired wavelength range, which is typically around 1.55 μm [30,31]. The waveguide dispersion [32] is decreased with the increase in the operating wavelength (λ), as shown in Figure 7. The proposed 2 × 2 silicon waveguide achieves a low dispersion of 0.54 ps^2/m at 1.55 μm and also exhibits flattened dispersion from the 1.45 to 1.6 μm wavelength, which is potentially useful for both telecom and mid-infrared applications. The device's performance can be optimized through the control of the waveguide dispersion by varying the waveguide's geometry [32].

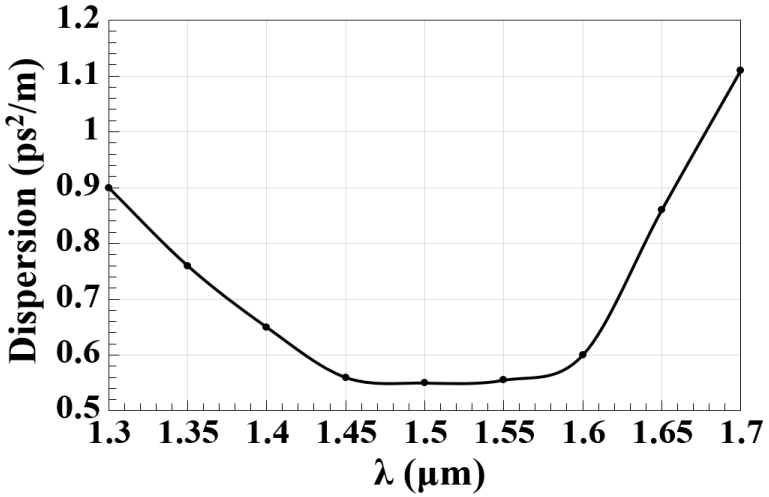

Figure 7. Waveguide dispersion versus operating wavelength (λ) utilizing 2 × 2 silicon waveguide.

3. Logic Functions

3.1. XOR

For the XOR, AND, and OR operations to be implemented, a reference beam (REF) needs to be inserted into P_{in3} of Figure 1. A reference phase difference between the input beams is introduced using the REF (all '1's), which can produce either constructive or destructive interference. Two additional beams are supplied to P_{in1} and P_{in2}, respectively.

P_{out} generates a logical '1' as a result of the constructive interference between the input beams when P_{in1} and P_{in2} are '0' and '1', or vice versa (i.e., 01 or 10), with REF adjusted at the same phase of 0°. Due to destructive interference between the input beams, P_{out} results in a '0' when both P_{in1} and P_{in2} are '1' launched at θ_1 = 180° and θ_2 = 90° with REF at θ_{REF} = 0°. The XOR gate is then implemented between the two input beams. The distributions of the light fields for the logic XOR gate at 1.55 µm are shown in Figure 8.

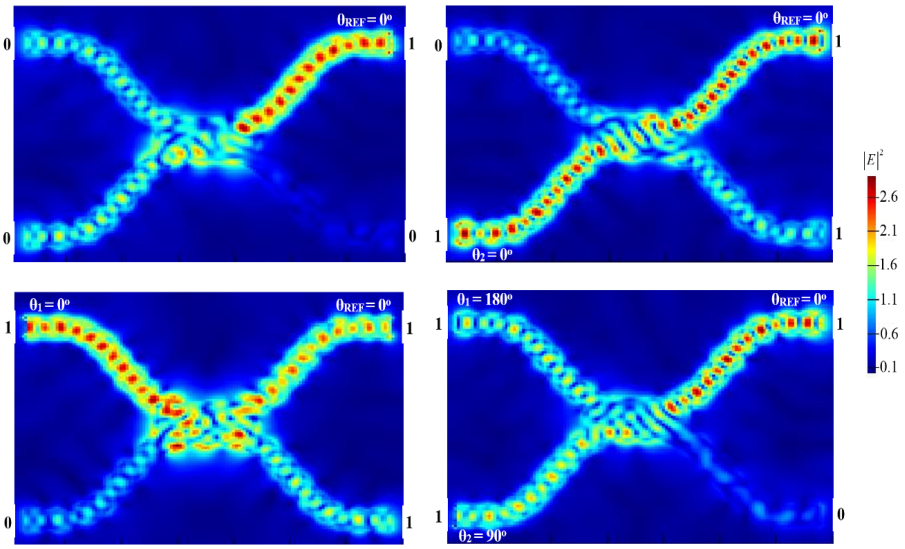

Figure 8. Light field distributions for XOR function utilizing 2 × 2 silicon waveguide at 1.55 µm.

The considerable disparity between P^1_{mean} and P^0_{mean} allows the proposed waveguide to have a high CR = 39.64 dB. The simulation findings for the XOR function are provided in Table 1.

Table 1. Simulation findings for XOR (T_{th} = 0.14).

P_{in1}	P_{in2}	P_{in3} (REF)	T	P_{out}	CR (dB)
0	0	1	0.009	0	39.64
0	1	1	0.524	1	
1	0	1	0.552	1	
1	1	1	0.012	0	

3.2. AND

By connecting two beams to P_{in1} and P_{in2}, as well as the REF (all '1's) to P_{in3}, the AND function is performed (see Figure 1). The phase angle of REF is adjusted to θ_{REF} = 0°. Destructive interference manifests because of the phase difference between the input beams when the two beams '1' and '0', or vice versa (i.e., 01 or 10), are injected at a different phase than the REF phase, leading to an output of '0'. Because the input beams and REF have the same phase, i.e., $\theta_1 = \theta_2 = \theta_{REF}$ = 0°, constructive interference produces '1'' at P_{out} when both input beams are '1'. The AND logic operation is therefore functionally accomplished. Figure 9 displays the light field distributions for the logic AND gate at 1.55 µm.

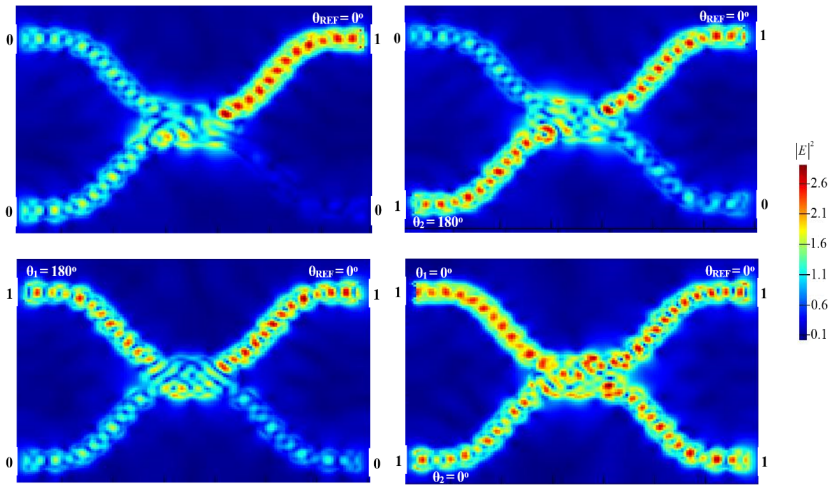

Figure 9. Light field distributions for AND function utilizing 2 × 2 silicon waveguide at 1.55 µm.

The simulation findings for the AND function with CR = 31 dB are summarized in Table 2.

Table 2. Simulation findings for AND (T_{th} = 0.14).

P_{in1}	P_{in2}	P_{in3} (REF)	T	P_{out}	CR (dB)
0	0	1	0.009	0	31
0	1	1	0.055	0	
1	0	1	0.053	0	
1	1	1	0.865	1	

3.3. OR

Two beams are sent into the waveguide from P_{in1} and P_{in2}, respectively, while the REF is supplied from P_{in3}, similar to the XOR and AND operations. When all input beams propagate at the same phase, i.e., $\theta_1 = \theta_2 = \theta_{REF} = 0°$, the OR function can be straightforwardly achieved, yielding a '1' output as a result of constructive interference between the input beams. Utilizing a 2 × 2 silicon waveguide at 1.55 µm, Figure 10 displays the light field distributions for the logic OR function.

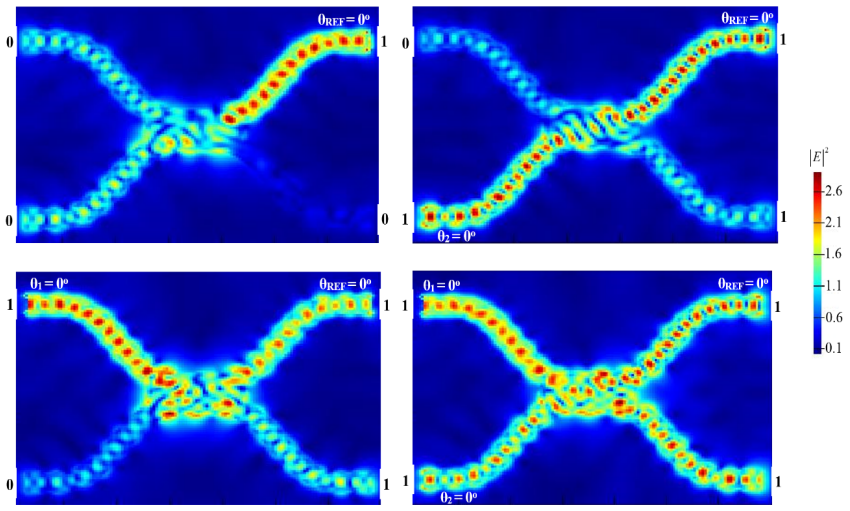

Figure 10. Light field distributions for OR function utilizing 2 × 2 silicon waveguide at 1.55 µm.

The simulation findings for the OR function at 1.55 µm concerning T and CR are summarized in Table 3. A high CR = 42.75 dB is achieved by utilizing the proposed waveguide due to the wide gap between P^1_{mean} and P^0_{mean}.

Table 3. Simulation findings for OR (T_{th} = 0.14).

P_{in1}	P_{in2}	P_{in3} (REF)	T	P_{out}	CR (dB)
0	0	1	0.009	0	42.75
0	1	1	0.524	1	
1	0	1	0.552	1	
1	1	1	0.865	1	

Table 4 compares the simulation findings of the considered logic functions at 1.55 µm using the proposed waveguide with and without REF. The obtained CRs are much greater with than without REF, according to the cited data.

Table 4. CR without and with REF.

Operation	CR (dB) Without REF	CR (dB) With REF
XOR	6.5	39.64
AND	5.2	31
OR	6.8	42.75

3.4. NOT

A clock light (Clk) and an input beam are, respectively, sent into the proposed waveguide from P_{in1} and P_{in2} in Figure 1 to perform the NOT function. In a manner, and similar to REF, the Clk introduces an additional phase shift to the propagating beams, altering the waveguide balance and producing the desired output. To achieve this function, the phases of the Clk (all '1's) and input beam should be adjusted at θ_{Clk} = 180° and θ_2 = 0°, respectively. The input beams suffer different phases when P_{in2} is set to '1', inducing destructive interference and producing a logical '0' output (i.e., T < T_{th}). The Clk does not go through a differencing phase when P_{in2} is set to '0', producing a logical '1' output (i.e., T > T_{th}) at P_{out}. Thus, the NOT function is realized. Figure 11 depicts the NOT function's light field distributions at 1.55 µm.

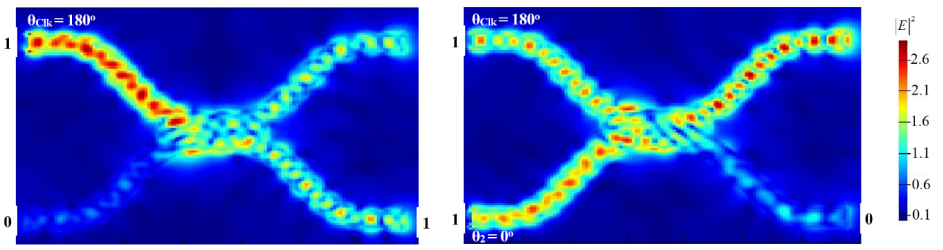

Figure 11. Light field distributions for NOT function utilizing 2 × 2 silicon waveguide at 1.55 µm.

The simulation findings for the NOT function are listed in Table 5. These findings demonstrate that a NOT logic function at 1.55 µm with CR = 24.63 dB can be formed utilizing the suggested waveguide.

Table 5. Simulation findings for NOT (T_{th} = 0.14).

P_{in1} (Clk)	P_{in2}	T	P_{out}	CR (dB)
1	0	0.552	1	24.63
1	1	0.047	0	

3.5. NOR

The Clk beam is injected into P_{in1} to realize the NOR (NOT–OR) function, while the other two beams are injected into P_{in2} and P_{in3}, respectively (see Figure 1). A logical '0' is produced at P_{out} due to the destructive interference when the combination of (01, 10, or 11) OF the input beams is injected at various angles. If the (00) combination of the two beams is launched, the Clk beam with $\theta_{Clk} = 180°$ will cancel the phase balance of the three input ports, thereby resulting in a logical '1' at P_{out}. Thus, the NOR gate is created, as seen in Figure 12.

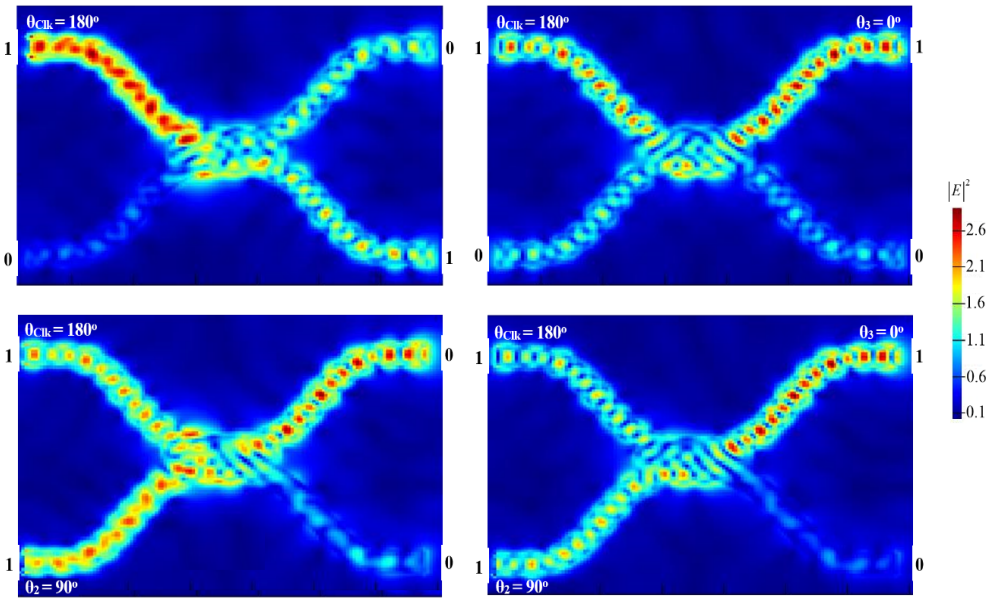

Figure 12. Light field distributions for NOR function utilizing 2 × 2 silicon waveguide at 1.55 µm.

Table 6 provides a summary of the simulation findings for the NOR gate with CR = 25.53 dB.

Table 6. Simulation findings for NOR (T_{th} = 0.14).

P_{in1} (Clk)	P_{in2}	P_{in3}	T	P_{out}	CR (dB)
1	0	0	0.552	1	25.53
1	0	1	0.054	0	
1	1	0	0.052	0	
1	1	1	0.023	0	

3.6. NAND

It is possible to perform the NAND (NOT–AND) operation by injecting the Clk into P_{in1} and the other two beams into P_{in2} and P_{in3}, respectively. Due to the Clk's $\theta_{Clk} = 180°$, the output is '1' when P_{in2} and P_{in3} are 'OFF' (i.e., 00). Constructive interference occurs when (01, 10) is launched with Clk at the same angle of 180°, producing a '1' at the output. When (11) is launched with Clk at different phases, i.e., $\theta_{Clk} = 180°$, $\theta_2 = 90°$, and $\theta_3 = 0°$, as shown in Figure 13, the concomitant destructive interference results in a '0' at the output.

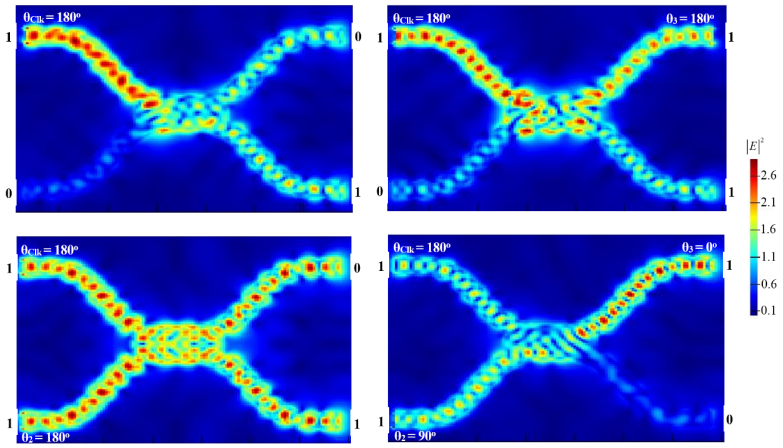

Figure 13. Light field distributions for NAND function utilizing 2 × 2 silicon waveguide at 1.55 µm.

The findings of the NAND function are compiled in Table 7. The mean peak power of '1' is greater than '0' when using our design at 1.55 µm, enabling a high CR = 33.38 dB for the NAND function.

Table 7. Simulation findings for NAND (T_{th} = 0.14).

P_{in1} (Clk)	P_{in2}	P_{in3}	T	P_{out}	CR (dB)
1	0	0	0.552	1	33.38
1	0	1	0.525	1	
1	1	0	0.865	1	
1	1	1	0.023	0	

3.7. XNOR

The Clk enters P_{in1}, and the two additional beams are injected from P_{in2} and P_{in3}, similarly to the NOR and NAND functions, to carry out the XNOR (exclusive-NOR) function. When the input beam combination (11) is introduced along with the Clk at the same phase of 180°, P_{out} produces a '1' output due to constructive interference. The Clk at 180° produces a '1' output for the (00) combination. As depicted in Figure 14, P_{out} comprises a '0' when the beam combinations (01) or (10) are injected with a different phase.

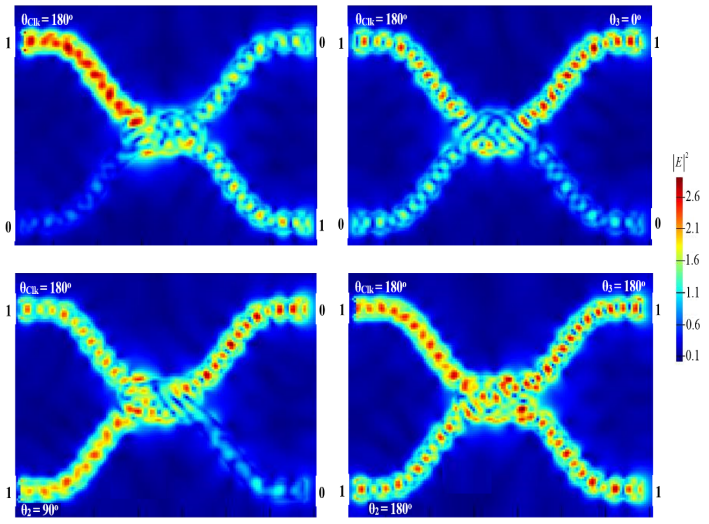

Figure 14. Light field distributions for XNOR function utilizing 2 × 2 silicon waveguide at 1.55 µm.

A high CR = 26 dB for the XNOR function is achieved employed the proposed waveguide. The XNOR simulation findings are provided in Table 8.

Table 8. Simulation findings for XNOR (T_{th} = 0.14).

P_{in1} (Clk)	P_{in2}	P_{in3}	T	P_{out}	CR (dB)
1	0	0	0.552	1	26
1	0	1	0.054	0	
1	1	0	0.052	0	
1	1	1	0.865	1	

The working data rate of the proposed waveguide is calculated to be 120 Gb/s for an optical bandwidth of 30 GHz and four beam levels (i.e., 00, 01, 10, 11) according to the Nyquist formula [33].

The manufacturing constraints are often referred to as a bottleneck. As more applications rely on nanophotonic devices, photonic design is becoming increasingly challenging and sophisticated. Designers are increasingly turning to advanced optimization techniques rather than traditional photonic design methodologies to address this challenge [34–37]. These new techniques examine devices with totally arbitrary geometries rather than modifying relatively straightforward known geometries with a small number of parameters, as is the conventional practice. In order to take advantage of the extra degrees of freedom, devices have been created that have incredibly small footprints, high efficiency, and innovative features that cannot be accomplished using conventional techniques [38–46]. The silicon and silica utilized in the proposed waveguide are common in the Earth's crust and play a significant role in the composition of the mantle. Because the nanofabrication technologies are already in place, it would, therefore, be possible to implement the proposed waveguide based on the key outcomes of the conducted simulation. In fact, it has been reported that several Boolean logic functions can be implemented experimentally based on different waveguides [16,22,47–49].

In order to check whether our work contributes in advancing the relevant the state-of-art, we compared our principal outcomes on the realization of the target logic functions using the proposed waveguides with those of other designs employed for the same purpose. To this end, we constructed Table 9, whose inspection reveals that, in contrast to other reported designs, the suggested waveguides allow for the performance of the specified logic functions at 1550 nm with higher CRs.

Table 9. Evaluation of the proposed design in comparison to other published waveguide-based logic functions.

Operations	Design	Wavelength (nm)	CR (dB)	Ref.
AND, XOR, OR	T-shaped photonic crystal waveguides	1550	8.29–33.05	[11–13]
AND, XOR, OR, NOT, NAND, NOR, XNOR	Photonic crystal waveguides	1550	5.42–9.59	[14]
XOR, AND, OR, NOR, NAND, XNOR	Dielectric-loaded waveguides	471	24.41–33.39	[15]
NOT, XOR, AND, OR, NOR, NAND, XNOR	Metal slot waveguide	632.8	6–16	[16]
NOT, XOR, AND, OR, NOR, NAND, XNOR	Metal–insulator–metal structures	632.8	15	[17]
NOT, XOR, AND, OR, NOR, NAND, XNOR	Dielectric–metal–dielectric design	900 and 1330	5.37–22	[18]
AND, XOR, OR, NOT, NAND, NOR, XNOR	Silicon-on-silica waveguides	1550	20.51–30.33	[19]
AND, XOR, OR, NOT, NAND, NOR, XNOR	K-shaped silicon waveguides	1550	30.5–34	[20]
AND, OR, NOT, NAND	Inverse design on silicon platforms	1300	0.5–5.79	[21]
AND, NOR, XNOR	Silicon photonics platform	1550	>10 dB	[22]
XOR, AND, OR, NOT, NOR, NAND, XNOR	2 × 2 silicon-on-silica waveguides	1550	24.63–42.75	This work

4. Conclusions

We have designed a full family of fundamental Boolean logic functions operated at 1.55 μm, using compact 2 × 2 silicon-on-silica waveguides. The proposed scheme consists of three input waveguides, one output waveguide, and a design area. Lumerical FDTD analysis software was used to perform these logic functions. The key for the proper operation of these functions is inducing and exploiting the appropriate tuning of the phase angle of the input-launched beams. By conducting numerical simulations based on FDTD analysis, we assessed and verified the high performance of the target gates. Moreover, we compared our outcomes to those of other reported similar designs and confirmed that the proposed waveguide results in higher CRs at higher operating speeds of up to 120 Gb/s.

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