All-optical logic operations based on silicon-on-insulator waveguides

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Abstract. Silicon waveguides are particularly appealing for the implementation of all-optical (AO) signal processing devices and switches due to the improved fabrication technology of silicon. Therefore, a silicon-on-silica waveguide is employed as the building block for simulating fundamental AO logic operations, including XOR, AND, OR, NOT, NOR, NAND, and XNOR, at 1.33-μm telecommunications wavelength. The proposed waveguide consists of two microring resonators and three strip waveguides. The operation concept of these logic gates relies on the constructive and destructive interference that results from the phase difference induced by incident optical beams. The performance of the target logic gates is assessed against the contrast ratio (CR) metric. The simulation results suggest that, by exploiting the proposed waveguides, these gates can operate with higher CR and faster speed compared to other designs. [DOI: 10.1117/1.OE.62.4.048101]

Keywords: optical logic operations; silicon-on-insulator waveguide; contrast ratio.

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1 Introduction

Silicon (Si) is too reactive to be found in nature, but it's found in practically all rocks as well as sand, clays, and soils, combined with oxygen as silicon dioxide (silica, SiO_2). Si is produced commercially by the reduction of SiO_2 with coke in an electric furnace. SiO_2, on the other hand, is the most abundant mineral found in the crust of the earth. Si possesses a high optical damage threshold, high quality and stable oxide, low-loss, and significant third-order optical nonlinearities, all of which are important qualities in photonics devices.[1] With fully compatible production techniques, silicon-on-insulator (SOI) material has recently become a prominent platform for both photonic and electronic devices such as modulators, photodetectors, couplers, switches, T- and Y-branches, and gratings.[1] On the other hand, the development of all-optical (AO) logic technologies is fundamental to realize future telecommunication networks with the exponential growth of internet traffic. Several waveguides, including photonic crystal waveguides,[2–9] semiconductor platforms,[10–14] gold nanowire waveguides,[15] metal slot waveguides,[16] metal–insulator–metal structures,[17] dielectric–metal–dielectric design,[18] dielectric–loaded waveguides,[19] graphene–containing compact microdisks,[20] and optical amplifiers,[21] have been used to create AO logic gates in recent years. The majority of these published designs only used photonic crystals to realize one or, at most, two logic gates,[2–13] in contrast to the suggested waveguide, which simultaneously realized seven logic operations. Furthermore, some of these reported projects have utilized more expensive noble metals, such as gold and silver,[15–19] as compared to the materials (i.e., silicon and silica) used in our design. Therefore, implementing multifunctional logic gates with high contrast ratios (CRs) between the output logic states "1" and "0" based on basic and inexpensive waveguides remains a significant challenge. Additionally, the suggested design can address the expanding need for faster speeds by

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transmitting data at a high speed of up to 103 Gb/s with higher CRs than other reported designs.[6,10,16–18] From here, we deduce that specialists in the field are still working and will strive to find simpler and less cost designs that meet future needs. Following these significant efforts, we have designed compact SOI waveguides to perform seven basic Boolean logic functions, including XOR, AND, OR, NOT, NOR, NAND, and XNOR operated at a telecommunications wavelength of 1.33 μm. It is commonly known that Si has a low loss (<2 dB/cm) for wavelengths up to 8 μm; however, at longer wavelengths, there are multiple multiphonon absorption peaks. SiO_2 optical loss, on the other hand, rapidly increases beyond 3.6 μm, making SOI waveguides unsuitable alternatives for longer wavelengths.[22] The proposed device consists of two microring resonators and three strip waveguides, all made of Si patterned on SiO_2. The operation principle for the realization of the proposed logic operations depends on the constructive and destructive interferences between the incident beams. These logic gates could be implemented by running Lumerical finite-difference-time-domain (FDTD) solutions with the convolutional optimally matched layer as an absorbing boundary condition.[23] The CR is employed to evaluate the operations' performance. This scheme can help with the design and implementation of numerous combinational circuits and subsequent applications, which are required for the creation and realization of lightwave systems and networks that fully exploit the advantages of AO solutions for efficiently satisfying customers' demanding needs.

2 SOI Waveguide

The structure consists of two identical microring resonators and three strips made of Si as core (refractive index ~3.45) patterned on SiO_2 insulator substrate as cladding (refractive index ~1.46). This results in substantially stronger light confinement inside SOI waveguides, which is advantageous for linear and nonlinear light applications as well as optical device size management.[1] The proposed device has three input ports (i.e., ports 1 to 3) and one output port (i.e., port 4). The input ports are exposed to the transverse electric mode polarized wave operating at 1.33 μm. The schematic diagram and electric field distributions of the suggested waveguide are illustrated in Fig. 1.

When a beam passes through the two side strips, part of the beam will be coupled into the middle strip through the optical microring resonators. The FDTD intensity monitors are used for recording the light intensities at the input and output ports. The spectral transmission (T) is defined as $T = I_{out}/I_{in} = |E_{out}|^2/|E_{in}|^2$,[14,19] where I_{out} is the intensity at the output port (i.e., P_{out}), and $I_{in} = I_1 + I_2 + I_3$ is the sum of the intensities at the three input ports. The threshold transmission (T_{th}) of 0.2 is first set to decide the desired logic function. The output port (i.e., port 4), produces a logical output of "1" when $T > T_{th}$, but in all other circumstances it produces "0." The input beams have the same intensity and wavelength. The incident beams must satisfy the phase-matching requirements for T to be maximized. Researchers are currently concentrating on on-chip optical phase compensation and reconfiguration employing unique techniques that can be separated into dynamic and static phase control schemes.[24,25] A thermooptic phase shifter is employed to regulate the phase between two distinct waveguides on the chip. Over one of the waveguides where a current can flow, a tiny nickel-chromium electrode is directly deposited. The refractive index changes slightly as a result of the local Ohmic heating, thus inducing an optical phase difference between the two different waveguides. This phase can be adjusted across a full range from 0 to 2π.[24] The addition of a modified line near the standard waveguide with low laser

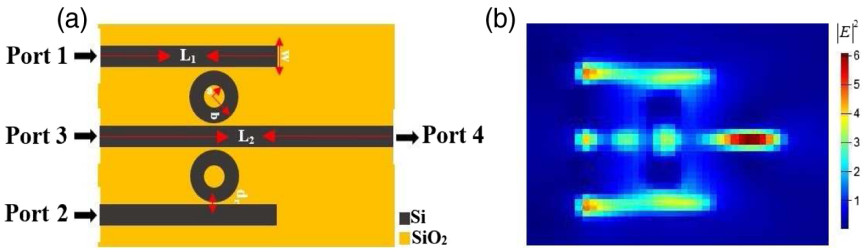

Fig. 1 (a) Schematic diagram and (b) electric field distributions of SOI waveguide.

Table 1 Simulation parameters.

Symbol	Definition	Value	Unit
L_1	Length of side stripes	1.0	μm
L_2	Length of middle stripe	1.5	μm
w	Width of stripe	0.2	μm
d	Thickness of stripe	0.3	μm
a	Radius of inner ring	0.1	μm
b	Radius of outer ring	0.2	μm
d_r	Distance between stripe and ring	0.01	μm
λ_s	Operating wavelength	1.33	μm
T_{th}	Threshold transmission	0.2	—

intensity, on the other hand, is employed as a static phase control strategy method. By keeping its single-mode feature, the changed line can change the waveguide's effective refractive index. The modified line can change the effective refractive index of the waveguide by maintaining its single-mode property.[25] Conversely, destructive interference scatters the incident beams and yields a "0" output when the waveguide and incident beams are out of phase. Typically, the CR is defined as $\text{CR(dB)} = 10\ \ln[P^1_{\text{mean}}/P^0_{\text{mean}}]$[14,21] takes into account the peak power of all outputs bits (i.e., P^1_{mean} and P^0_{mean}), while other metrics, such as the extinction ratio, only take into account the peak power of the minimum and maximum outputs "1" and "0," respectively. Thus, the performance of the logic gate design may thus be evaluated more effectively and accurately using the CR.[26] The default parameters indicated in Table 1 were used for all simulations during preparation and execution using FDTD.

Figure 2 illustrates the spectral transmission (T) utilizing the suggested waveguide as a function of operating wavelength (λ). The incident beams have been injected at the three input ports with the same 180 deg phase when this figure was obtained. This figure demonstrates how the proposed waveguide maintains high T throughout a broad range of telecommunications wavelengths, from 1.3 to 1.6 μm.

The distance between the strip and ring (d_r) plays an important role in the proposed design in order to implement the considered logic gates with high CRs. Thus, the effect of d_r on normalized spectral T at an operating wavelength of 1.33 μm is simulated, as shown in Fig. 3. It is clear from this figure that a high T is obtained up to $d_r = 60$ nm. This result confirms that the proposed design can be fabricated especially with the availability of the 3D capability of the femtosecond laser direct writing technology.[27–36]

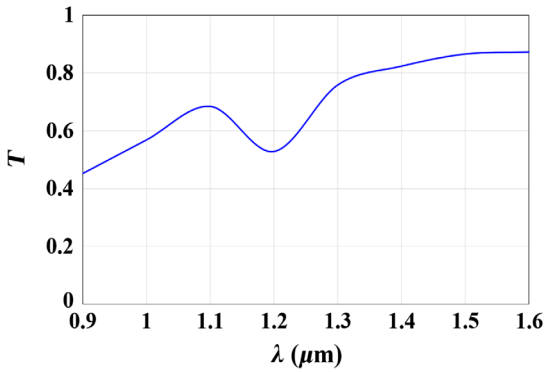

Fig. 2 Spectral transmission (T) versus operating wavelength (λ) using SOI waveguide.

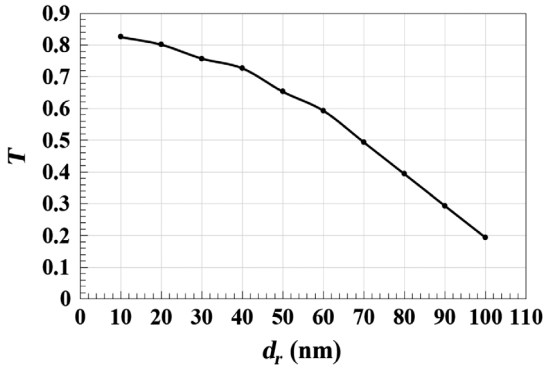

Fig. 3 Normalized spectral transmission (T) versus distance between strip and ring (d_r) using SOI waveguide.

For both production and operating conditions, relaxed tolerances are essential. Production tolerances deal with how geometrical dimensions are handled during processing and how that affects the functionality of the device. While the device's response to changes in wavelength, polarization, temperature, input field distribution, and refractive index is described by operation tolerances.[37,38] Practical wavelength tolerance is generally quite large for laser sources. The actual wavelength of a 1330-nm laser diode, for instance, can be 1330 ± 10 nm due to a wavelength tolerance of ± 10 nm.[39] The dependence of the loss on the wavelength tolerance using the SOI waveguide is depicted in Fig. 4 based on Eqs. (4)–(7).[40]

Shannon-Hartely developed a theoretical formula for calculating the transmission rate; however, they also took into account the signal-to-noise ratio. Shannon-Hartely expresses the speed of transmission as $B \log_2[1 + \mathrm{SNR}]$,[41] where B is the optical bandwidth, which is defined as $B = (c/\lambda^2)\Delta\lambda$, where c is the speed of light in vacuum, $\lambda = 1.33$ μm is the optical carrier wavelength, and $\Delta\lambda$ is the signal's spectral width. $\mathrm{SNR} = P_{\mathrm{out}}/\mathrm{kTB}$, where P_{out} is the total output power; k is Boltzmann's constant; and T is the absolute temperature. This means that in our case at room temperature (i.e., $T = 295$ k), where $P_{\mathrm{out}} = 0.16$ μW and $B = 8.48$ GHz, the speed is 103 Gb/s.

The components Si and SiO_2 used in the proposed waveguide are widely distributed in the earth's crust and have a major impact on the mantle's composition. The primary findings of this simulation can therefore be used as a foundation for experimental verification of the proposed waveguide, given that the required technology is accessible. Numerous optical logic functions, on the other hand, are implementable experimentally based on various waveguides.[10,12,15,42,43] Additional electrical and optical components, such as laser sources, couplers, fibers, phase shifters, amplifiers, filters, etc., should unquestionably be needed for the whole experimental setup for creating logical operations.[44–46]

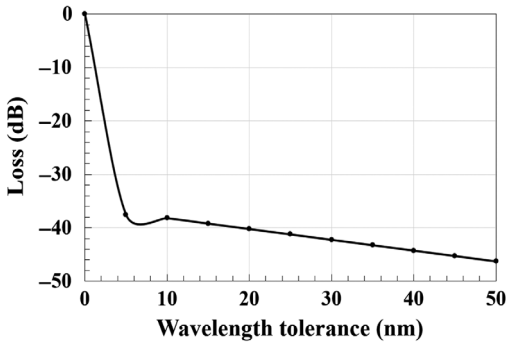

Fig. 4 Loss versus wavelength tolerance using SOI waveguide.

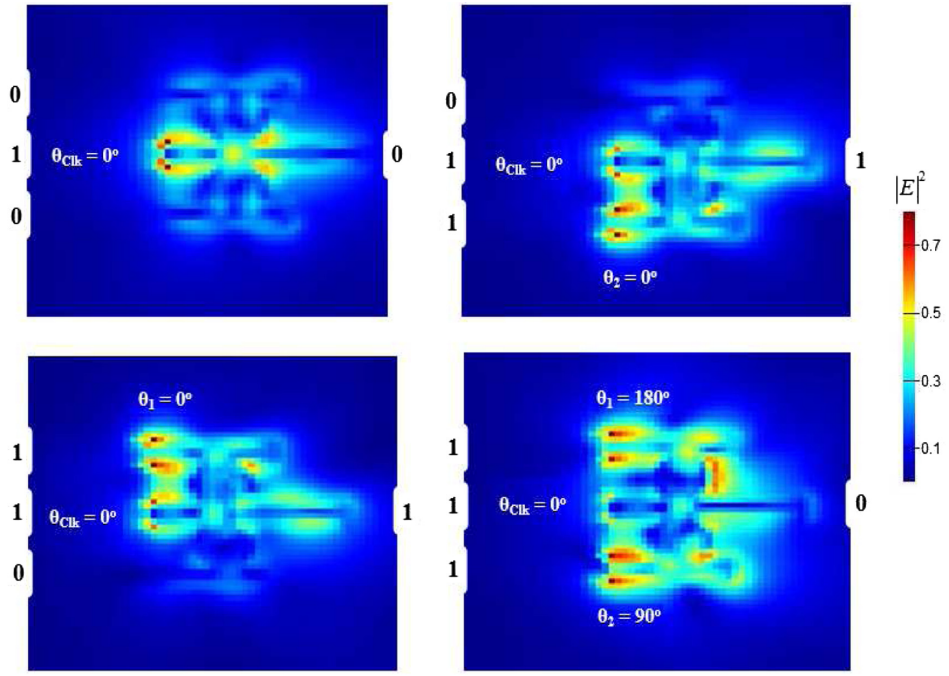

Fig. 5 XOR field intensity distributions using SOI waveguide at 1.33 μm.

3 Gates' Implementation

3.1 *XOR*

The XOR gate gives a "1" output if only one of its inputs is "1". To perform the XOR gate, two input beams are injected into the scheme from ports 1 and 2, respectively. The clock light (Clk) is launched into the middle port (i.e., port 3) while port 4 acts as the output port (see Fig. 1). The Clk (all "1's") should be utilized to produce an input beam reference phase difference that results in either constructive or destructive interference. When two input beams are "0" and "1," or vice versa (i.e., 01 or 10) and Clk all adjusted with the same phase of 0 deg, port 4 generates a higher T than T_{th} due to the constructive interference, resulting in "1" output. When both input beams are "1" having $\Delta\theta = 90$ deg and Clk having $\theta_{\text{Clk}} = 0$ deg, the output of port 4 produces "0" due to the destructive interference between the input beams. The field intensity distributions for the logic XOR gate at 1.33 μm are illustrated in Fig. 5.

Table 2 summarizes the simulation results for the XOR gate. High CR = 25.67 dB is obtained due to the relatively slight difference between the mean peak powers of logical "1" and logical "0".

3.2 *AND*

"1" output results only if all the inputs to the AND gate are "1". Two beams are inserted from ports 1 and 2, while the Clk (all "1's") is inserted from port 3 to perform the AND operation

Table 2 XOR simulation results ($T_{\text{th}} = 0.2$).

Port 1	Port 2	Port 3 (Clk)	Port 4 (output)	T	CR (dB)
0	0	1	0	0.037	25.67
0	1	1	1	0.514	
1	0	1	1	0.514	
1	1	1	0	0.042	

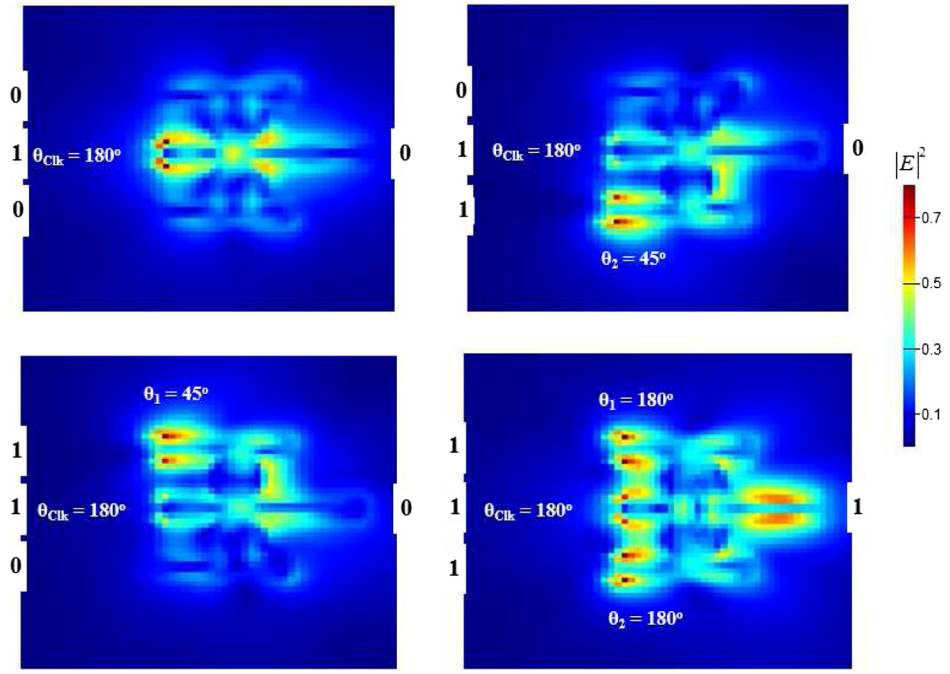

Fig. 6 AND field intensity distributions using SOI waveguide at 1.33 μm.

Table 3 AND simulation results ($T_{th} = 0.2$).

Port 1	Port 2	Port 3 (Clk)	Port 4 (output)	T	CR (dB)
0	0	1	0	0.037	32.73
0	1	1	0	0.029	
1	0	1	0	0.029	
1	1	1	1	0.826	

(see Fig. 1). When the input beams are "1" and "0" or vice versa, the destructive interference results in "0" at port 4 due to the phase difference between the input beams. When both input beams are "1," port 4 generates "1" output due to the constructive interference, occurring as a result of the same phases of the input beams and Clk, i.e., $\theta_1 = \theta_2 = \theta_{Clk} = 180$ deg. This is functionally equivalent to the AND logic operation. Figure 6 shows the AND field intensity distributions at 1.33 μm.

Table 3 shows that the value of the CR = 32.73 dB is very high due to the extreme difference between the mean peak powers of "1" and "0".

3.3 *OR*

The logic OR gate results in "1" output only when one or more of its inputs are "1". For the OR gate, two input beams are supplied into the waveguide from ports 1 and 2, while the Clk is injected into the middle port (i.e., port 3). The OR gate can be realized when the input beams and Clk are propagating with the same phase, i.e., $\theta_1 = \theta_2 = \theta_{Clk} = 0$ deg. Therefore, the normalized T is enhanced by the constructive interference between the input beams. The field intensity distributions for the logic OR gate are depicted in Fig. 7 at 1.33 μm.

Table 4 shows the simulation findings in terms of normalized T and CR for the OR gate at 1.33 μm.

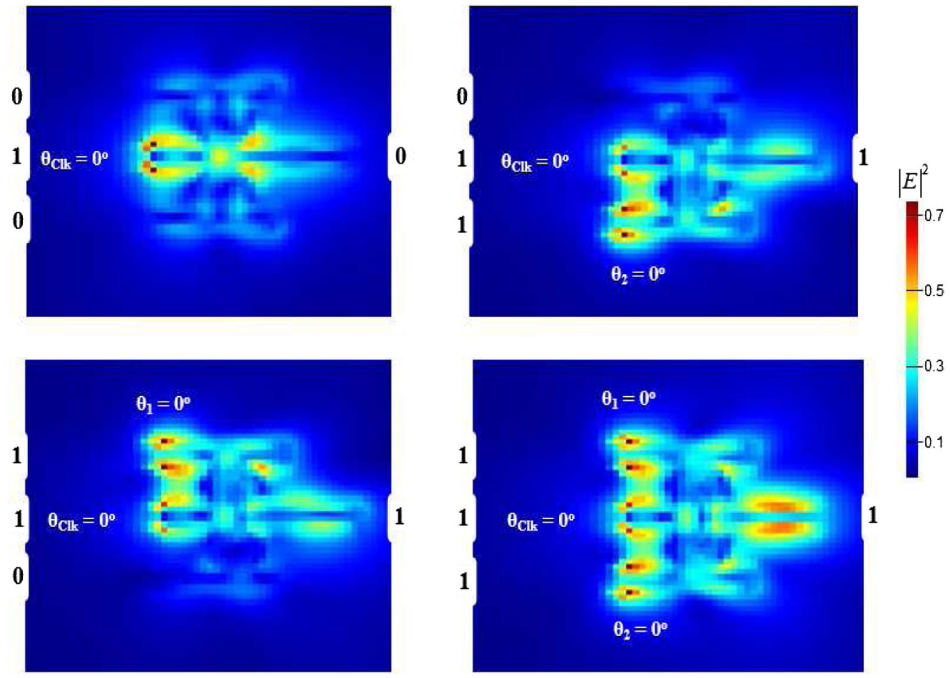

Fig. 7 OR field intensity distributions using SOI waveguide at 1.33 μm.

Table 4 OR simulation results ($T_{th} = 0.2$).

Port 1	Port 2	Port 3 (Clk)	Port 4 (output)	T	CR (dB)
0	0	1	0	0.037	28.43
0	1	1	1	0.514	
1	0	1	1	0.514	
1	1	1	1	0.826	

3.4 *NOT*

The NOT or invert gate provides a "1" output if the input is "0" and vice versa. For the NOT gate, a Clk (all 1's) with $\theta_{Clk} = 180$ deg and an input beam with $\theta = 45$ deg are injected into the proposed structure from ports 1 and 2, respectively. When port 2 is "1", the input beams experience differing phases to destructively interfere, thereby resulting in a logical "0" at the output of port 4. When port 2 is "OFF", the Clk does not experience any phase difference, resulting in logical "1" at port 4. This procedure is analogous to the logic NOT gate. The NOT field intensity distributions at 1.33 μm are shown in Fig. 8.

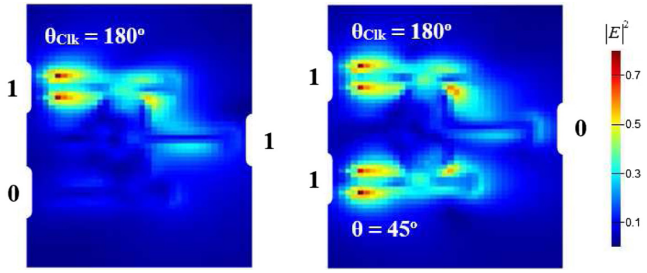

Fig. 8 NOT field intensity distributions using SOI waveguide at 1.33 μm.

Table 5 NOT simulation results ($T_{th} = 0.2$).

Port 1 (Clk)	Port 2	Port 4 (output)	T	CR (dB)
1	0	1	0.310	11.78
1	1	0	0.037	

The simulation results for logic NOT gate are summarized in Table 5. These results show that the NOT logic gates can be implemented at 1.33 μm with better CR = 11.78 dB using the proposed scheme.

3.5 *NOR*

An output "1" results if both the inputs to the NOR (NOT-OR) gate are "0". To perform NOR, the Clk is injected into port 1, while the two input beams are injected into ports 2 and 3 in Fig. 1. Thus, when a combination of input beams is (01, 10, or 11), the logic output is "0" due to the phase difference that leads to destructive interference. When beams with the combination (00) are launched at $\Delta\theta = 0$ deg, the Clk beam at $\theta_{Clk} = 180$ deg breaks the phase balance, resulting in a logical "1" at port 4 due to constructive interference. The Boolean NOR logic gate is thus realized as depicted in Fig. 9.

Table 6 summarizes the simulation results for the NOR gate with CR = 23.70 dB.

3.6 *NAND*

NAND gate (NOT-AND) produces a "0" output only if all its inputs are "1". The NAND gate can be performed by injecting the Clk into port 1 while the two other input beams are launched into ports 2 and 3, respectively. When (00) is launched, the output is "1" due to the Clk injected into with $\theta_{Clk} = 0$ deg. In this case, the spectral T value is slightly above the T_{th}. When (01, 10) is launched with the same phase (i.e., $\Delta\theta = 0$ deg), constructive interference occurs, resulting in a "1" output. Destructive interference happens at port 4 when (00) is launched at different phases, i.e., $\theta_1 = 180$ deg, $\theta_2 = 45$ deg, and $\theta_{Clk} = 0$ deg, as shown in Fig. 10.

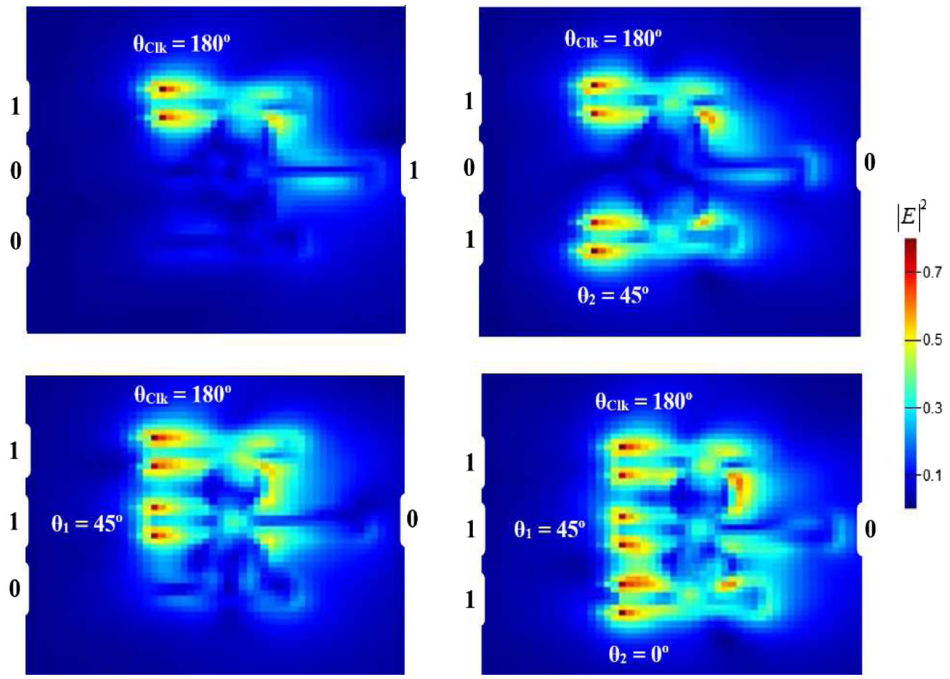

Fig. 9 NOR field intensity distributions using SOI waveguide at 1.33 μm.

Table 6 NOR simulation results ($T_{th} = 0.2$).

Port 1 (Clk)	Port 2	Port 3	Port 4 (output)	T	CR (dB)
1	0	0	1	0.310	23.70
1	0	1	0	0.030	
1	1	0	0	0.027	
1	1	1	0	0.034	

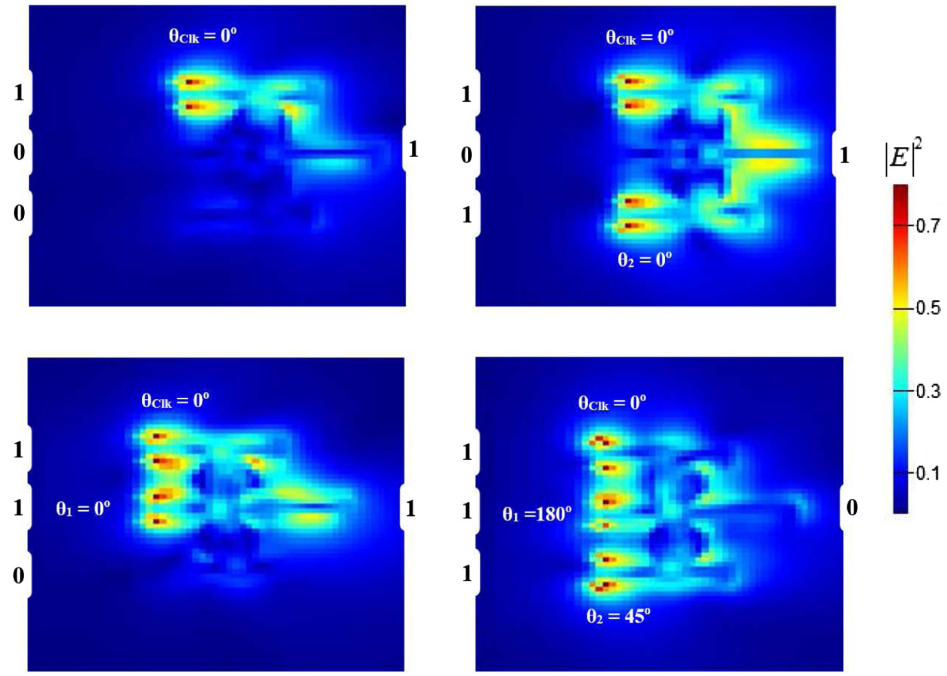

Fig. 10 NAND field intensity distributions using SOI waveguide at 1.33 μm.

Table 7 NAND simulation results ($T_{th} = 0.2$).

Port 1 (Clk)	Port 2	Port 3	Port 4 (output)	T	CR (dB)
1	0	0	1	0.290	30.50
1	0	1	1	0.735	
1	1	0	1	0.684	
1	1	1	0	0.027	

The simulation results for the NAND gate are listed in Table 7. The mean peak power of "1" output is higher than that of "0" producing a high CR = 30.50 dB.

3.7 *XNOR*

An output "1" results if both of the inputs to the XNOR gate are the same (i.e., 00 or 11). As in the NOR and NAND gates, the Clk is going into port 1, while the two beams are into ports 2 and 3, respectively. Both constructive and destructive interferences between the Clk and the input beams are used to perform the XNOR gate. The output port is "1" when input beams'

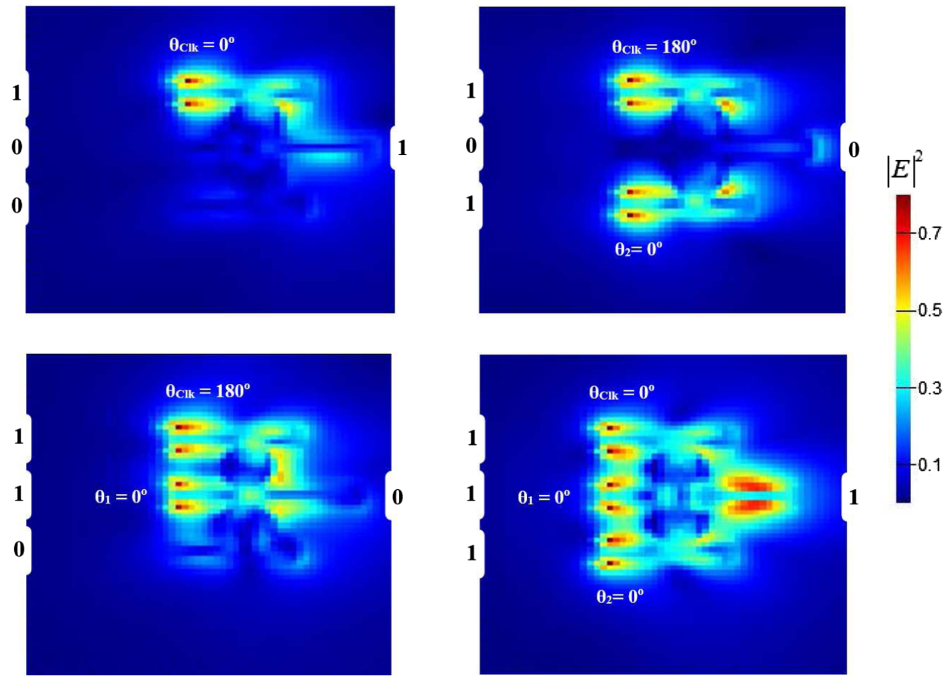

Fig. 11 XNOR field intensity distributions using SOI waveguide at 1.33 μm.

Table 8 XNOR simulation results ($T_{th} = 0.2$).

Port 1 (Clk)	Port 2	Port 3	Port 4 (output)	T	CR (dB)
1	0	0	1	0.310	30.85
1	0	1	0	0.027	
1	1	0	0	0.025	
1	1	1	1	0.827	

combination (00) or (11) is inserted with the same phase, producing constructive interference. By contrast, the output port is "0" when the beams' combination (01) or (10) are launched with different phases, creating destructive interference (Fig. 11).

Because of the wide disparity in the mean peak powers of the "1" and "0" bits, the XNOR gate has a high CR = 30.85 dB. The XNOR simulation results are summarized in Table 8.

4 Comparison

Table 9 summarizes various reported structures operated at different wavelengths for implementing AO logic operations. According to this table, the suggested waveguide can perform logic operations with higher CRs than the other listed schemes.

5 Applications

Possible drawbacks of the analyzed subsystem can be identified concerning issues such as cascadability and scalability. The proposed waveguide is more scalable, as it is simple to use to implement more combinational logic circuits, such as adders and latches. Besides, the operating wavelengths can be turned on or off on demand, which allow for the easy provisioning of services and quick scaling for a growing network. The proposed waveguide is also small and light.

Table 9 Comparison of implemented AO logic gates using various structures at different wavelengths.

Operations	Structure	Wavelength (nm)	CR (dB)	References
AND, XOR, OR, NOT, NAND, NOR XNOR	Photonic crystal waveguides	1550	5.42 to 9.59	6
AND, XOR, OR	T-shaped photonic crystal waveguides	1550	8.29 to 33.05	7–9
AND, NOR, XNOR	Si photonics platform	1550	>10 dB	10
NOT, XOR, AND, OR, NOR, NAND, XNOR	Metal slot waveguide	632.8	6 to 16	16
NOT, XOR, AND, OR, NOR, NAND, XNOR	Metal-insulator-metal structures	632.8	15	17
NOT, XOR, AND, OR, NOR, NAND, XNOR	Dielectric-metal-dielectric design	900 and 1330	5.37 to 22	18
NOT, XOR, AND, OR, NOR, NAND, XNOR	SOI waveguides	1330	11.78 to 32.73	This work

It can typically be placed in optical computers for growth needs up to 15 to 20 years in the future. Furthermore, additional optical components can be installed later to make way for network expansion. However, the optical losses limit the scalability.[47] Thus, the losses must be minimized at the coupling interfaces between the strips and microrings by optimizing the waveguide operational parameters as in our case. On the other hand, the fan-out capability should be attainable in a straightforward manner so as to facilitate the process of building more complex all-optical circuits of enhanced functionality. However, in our case, the operation of the reconfigurable gates is sensitive to the phase of the input beams, whose wavelengths must be carefully assigned. The gates should be able to accommodate more than two input data beams towards implementing multibit logic processing and constructing large switch fabrics. However, increasing the number of data inputs could complicate the process of managing the broadened spectra of these beams. These spectra should be suppressed so as not to spectrally overlap with that of the clock and deteriorate the performance of the gates. Still, these drawbacks are compensated for by the potential of the scheme to realize a suite of different logic functions without change in its fundamental design or architecture. In particular, these logic functions, including XOR, AND, OR, and INVERT, are fundamental in the implementation of various AO systems, such as packet switches, binary adders, binary counters, decision circuits, optical processors, data encoders, parity generation and checking, encryption/decryption, bit pattern recognition circuits, and complex combinational logic circuits. Depending on the outcomes of this simulation, these computational logic circuits can be easily implemented. For example, the SUM and CARRY are two logic functions necessary to realize a binary half-adder. The logical outcome of the SUM function is "1" when only both inputs are "1" and "0," which is equivalent to the logical XOR operation. The logical outcome of the CARRY function is "1" when only both inputs are "1," which is equivalent to the logic AND gate.[48] These two functions are then routed through a similar operation with suitable delay to carry out a full-adder function.[49] The AO latches are also one of the most fundamental sequential logic circuits. 2-input NAND logic gates connected is the simplest approach to build a set-reset latch while two logic functions NAND and NOT are used to build the D flip-flop.[50] The other AO JK and T flip-flops are also can be performed.[51] The parity generator can be also constructed using optical XOR gates.[49] The AO pseudorandom bit stream generators can be made with an optical delay line and XOR gates.[49] Additionally, OA encoder, half-subtractor, and comparator logic circuits can also be performed based on AND, NOR, and XNOR logic gates.[52,53] These logic functions have relied on the compactness, low power consumption, and integrability of the proposed SOI waveguide.

6 Conclusions

We implemented a whole set of fundamental optical logic operations, including XOR, AND, OR, NOT, NOR, NAND, and XNOR, operated at a telecommunications wavelength of 1.33 μm using compact silicon-on-silica waveguides. Lumerical FDTD solutions were employed to simulate these operations. Two ring resonators and three identical slots make up the suggested microwaveguide. The proper operation of these logic gates is based on the constructive and destructive interferences that are caused by the phase difference of the input beams. With a speed of 103 Gb/s, the proposed waveguide achieves higher CR values than those previously reported.

Acknowledgments

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