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Fermi-Level Depinning in Metal/Ge Junctions by Inserting a Carbon Nanotube Layer

Yu-Ning Wei, Xian-Gang Hu, Jian-Wei Zhang, Bo Tong, Jin-Hong Du, Chang Liu, Dong-Ming Sun, and Chi Liu**

Germanium (Ge)-based devices are recognized as one of the most promising next-generation technologies for extending Moore's law. However, one of the critical issues is Fermi-level pinning (FLP) at the metal/n-Ge interface, and the resulting large contact resistance seriously degrades their performance. The insertion of a thin layer is one main technique for FLP modulation; however, the contact resistance is still limited by the remaining barrier height and the resistance induced by the insertion layer. In addition, the proposed depinning mechanisms are also controversial. Here, the authors report a wafer-scale carbon nanotube (CNT) insertion method to alleviate FLP. The inserted conductive film reduces the effective Schottky barrier height without inducing a large resistance, leading to ohmic contact and the smallest contact resistance between a metal and a lightly doped n-Ge. These devices also indicate that the metal-induced gap states mechanism is responsible for the pinning. Based on the proposed technology, a wafer-scale planar diode array is fabricated at room temperature without using the traditional ion-implantation and annealing technology, achieving an on-to-off current ratio of 4.59×10^4. This work provides a new way of FLP modulation that helps to improve device performance with new materials.

1. Introduction

As Si semiconductor technology approaches its physical limits, Germanium (Ge)-based devices are recognized as a promising next-generation technology for continuing Moore's law, not only because Ge has an obvious electron mobility advantage over Si, but also because its manufacturing process is compatible with that of Si.[1–25] However, one of the critical issues for Ge semiconductor technology is the relatively large contact resistance at the metal/n-Ge interface. The contact resistance is exponentially dependent on $\varphi N^{-0.5}$, where φ is the Schottky barrier height and N is the doping concentration of Ge. Ge has an inherent problem of relatively low impurity solubility; therefore it is necessary to select metals for a small φ. However, generally for metal/n-Ge junctions, the Fermi level of Ge at the interface is almost perfectly pinned near the valence band edge, making metal selection meaningless. Therefore, it is essential to alleviate the Fermi-level pinning (FLP) to obtain a small φ and contact resistance.[26–28]

Several strategies have been proposed for FLP modulation,[26–45] and one of the main ones is the insertion of a thin layer of material between metal and n-Ge.[29–39] Nishimura et al. modulated the FLP by inserting a 2 nm-thick GeO_2 layer, however the on-current was weak because of the tunneling resistance caused by the inserted insulating layer.[29] Kobayashi et al. inserted an ultrathin SiN layer and obtained ohmic contact between metal and n-Ge, but the contact resistance was large due to the large resistance of the insertion layer.[31] Baek et al. inserted a graphene layer between metal and n^+-Ge leading to FLP modulation, however, the large tunneling resistance resulting from carrier transmission perpendicular to the graphene layers lead to a large contact resistance.[38] Kumari et al. recently used multilayer black phosphorus as an insertion layer, however a large remaining Schottky barrier height of 0.34 eV[39] resulted in a large resistance. The remaining barrier height and the resistance induced by the insertion layer generally limit the contact resistance in the insertion structures. In addition to the limited performance improvement, the mechanism is under debate. The alleviation of FLP may be due to a metal-induced gap states (MIGS) effect reduction or interfacial states passivation by the interfacial layer.[28–45] Seo et al. showed that the surface state that determines the charge neutrality level is actually a surface resonance in Ge, indicating that the evanescent states near the Ge surface play an essential role in the FLP.[46] Kuzmin et al. showed that the FLP on n-Ge is not due to the

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defect states, but is strongly contributed by the evanescent state of the Ge bulk, and the pinning effect can be eliminated at the epitaxial crystalline BaO/Ge (001) interface where BaO and Ge (001) lattices are perfectly matched.[47]

Here, we propose a method of inserting a wafer-scale carbon nanotube (CNT) layer between metal and n-Ge to reduce the effective Schottky barrier height without inducing a large resistance. The layer produces ohmic contact for germanium devices via a wafer-scale room-temperature process, and the smallest contact resistance between a metal and a lightly doped n-Ge has been achieved. The devices also provide a platform to investigate the mechanism of the pinning effect, where experimental evidence shows that the MIGS mechanism is responsible for the pinning. Based on the CNT layer insertion technology, a wafer-scale planar diode array is fabricated at room temperature without using the traditional ion-implantation and annealing technology, demonstrating high and uniform electrical and optoelectronic properties including an on-to-off current ratio of 4.59×10^4 at ± 1 V and a responsibility of 38.02 A W^{-1} using a 1065-nm laser illumination.

2. Results

2.1. Carbon Nanotube Insertion

The metal/CNT/Ge junction was fabricated by transferring a CNT film onto an n-Ge (100) substrate (resistivity: 1–5 Ω cm, doping concentration: about 5×10^{14} cm^{-3}), followed by a metallization of Au/Ti/Al (50/5/150 nm) and CNT patterning (**Figure 1**a). The device structure and optical images are shown in Figure 1b,c. For more details, see the Experimental Section. Large-area CNT films of different thicknesses were collected by a floating catalyst chemical vapor deposition (FCCVD) method using different collection times[48] (Figure 1d). The conductive transferred CNT film network is composed of numerous single-wall CNT (SWCNT) bundles where diameters of SWCNTs are in the range of 1.7–3.0 nm with a mean value of about 2.2 nm[48] (Figure 1e). Thicknesses of the CNT films are 2–40 nm, leading to devices D2–D12, which were characterized by an atomic force microscope (AFM) (Figure S1, Supporting Information) and a scanning electron microscope (SEM) (Figure S2, Supporting Information). For device D1, no CNT film was inserted. A secondary ion mass spectroscopy (SIMS) confirmed that oxidation of germanium surface in the structure was negligible (Figure S3, Supporting Information). In contrast to the germanide–Ge junctions,[49] Al can form abrupt junctions with Ge which provides a reproducible interface of high quality[50] to study the effect of CNT insertion.

2.2. Electrical Characteristics of Al/CNT/Ge Junctions

For each of the devices with different CNT thicknesses, 20 devices were measured with the top Al electrode grounded and showed good electrical uniformity in terms of *I–V* characteristics (Figure S4, Supporting Information). The typical *I–V* characteristics of each device are shown in **Figure 2**a with a clear variation in the reverse leakage current. Device D8 showed the highest leakage current and almost symmetrical *I–V* characteristics, indicating effective Fermi-level depinning and quasi-ohmic contact. A boxplot was used to show the statistical distribution of the leakage currents of the junctions showing that as the thickness of the CNT film increases, the leakage current increases and then decreases, with a peak value achieved by device D8 (Figure 2b). This is supported by a histogram analysis (Figure S5, Supporting Information). The CNT thickness effect differs with metals.

In order to analyze the effective Schottky barrier height[50,51] of the Al/CNT/Ge junction, the *I–V* characteristics were measured at temperatures from 224.2 to 331.0 K.[52] The characteristic of device D1 without a CNT film shows an obvious temperature dependence, which is the feature of the thermionic emission of a Schottky junction (Figure 2c). A Richardson plot shows that the effective Schottky barrier height extracted from the experimental results is about 0.62 eV[53,54] (Experimental Section, Figure S6, Supporting Information). In contrast, for device D8 with a 14-nm CNT film insertion, the *I–V* characteristics are almost independent of temperature (Figure 2d), indicating a reduction of the effective Schottky barrier height after the CNT film insertion. Using a p-type Ge (100) substrate (resistivity: 1–10 Ω cm, doping concentration: about 9×10^{14} cm^{-3}),

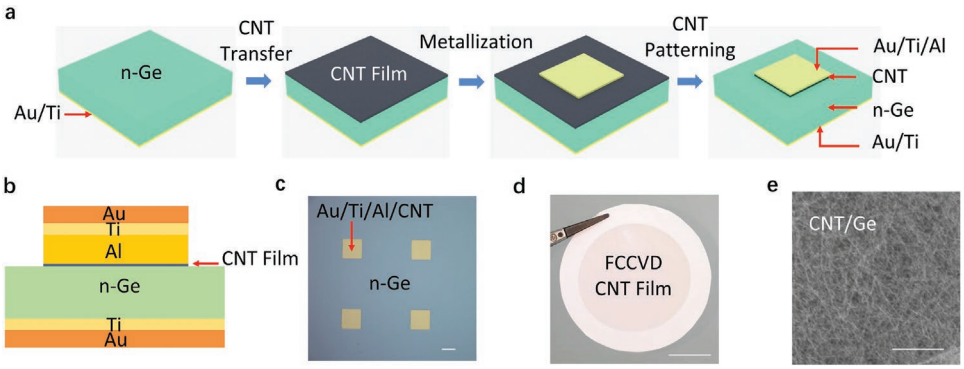

Figure 1. Carbon nanotube insertion layer. a) Fabrication of an Al/CNT/Ge junction by directly stacking a metal electrode, a CNT film and a Ge substrate with a bottom ohmic contact. b) A schematic of an Al/CNT/Ge junction. c) An optical image of an array of Al/CNT/Ge junctions (scale bar: 50 μm). d) A CNT film with a diameter of 55 mm (scale bar: 20 mm) collected by the FCCVD method. e) An SEM image of a 12-nm-thick CNT film transferred onto an n-Ge substrate (scale bar: 5 μm).

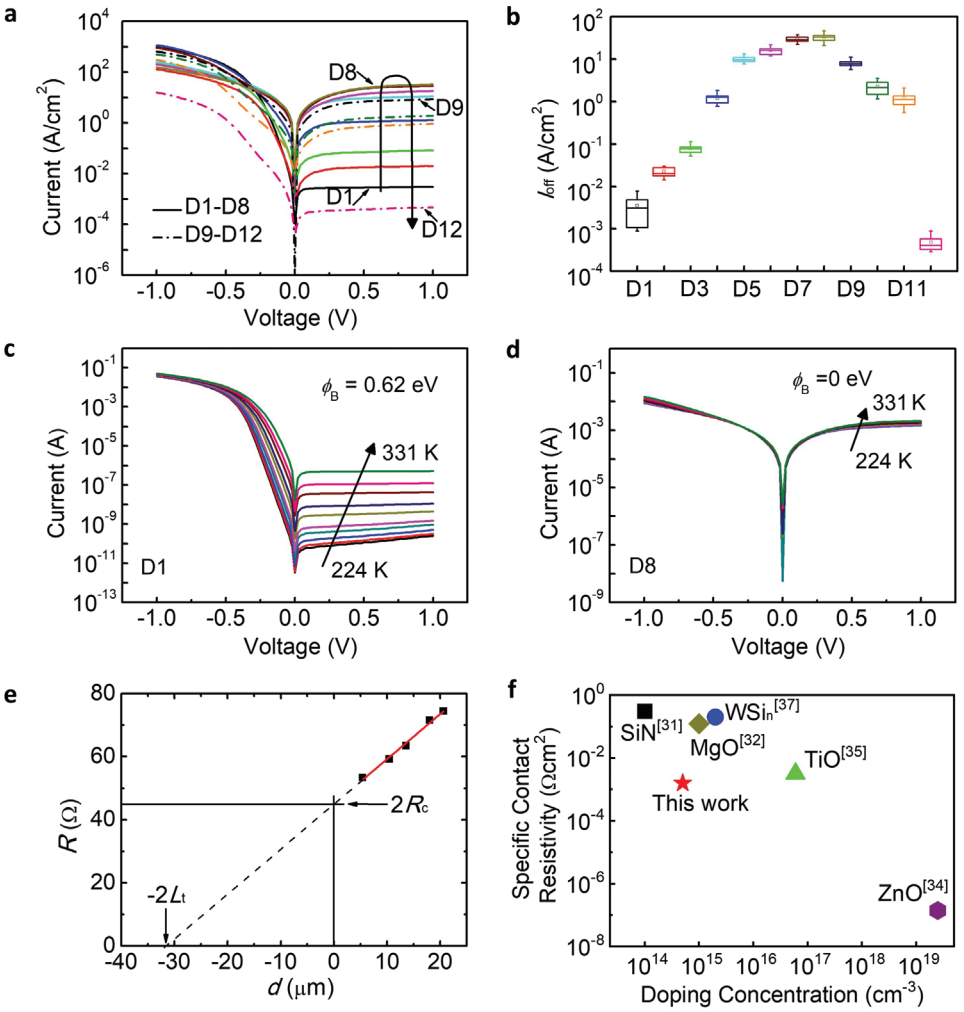

Figure 2. Electrical characteristics of Al/CNT/Ge junctions. a) Typical *I–V* characteristics for devices D1–D12 with clear differences in reverse leakage current. b) Boxplots of the leakage current of the junctions D1–D12 at a reverse bias of 1 V. For each of the devices with different CNT thicknesses, 20 devices were measured ($n = 20$), showing leakage currents of D1–D12 are $3.51 \times 10^{-3} \pm 2.17 \times 10^{-3}$ ($p = 0.04$, $\alpha = 0.05$), $2.25 \times 10^{-2} \pm 5.58 \times 10^{-3}$ ($p = 0.03$, $\alpha = 0.05$), $7.73 \times 10^{-2} \pm 1.64 \times 10^{-2}$ ($p = 0.23$, $\alpha = 0.05$), 1.21 ± 0.29 ($p = 0.50$, $\alpha = 0.05$), 10.15 ± 2.29 ($p = 0.11$, $\alpha = 0.05$), 15.95 ± 2.81 ($p = 0.42$, $\alpha = 0.05$), 29.86 ± 5.10 ($p = 0.17$, $\alpha = 0.05$), 33.02 ± 6.48 ($p = 0.88$, $\alpha = 0.05$), 7.98 ± 1.45 ($p = 0.52$, $\alpha = 0.05$), 2.28 ± 0.76 ($p = 0.20$, $\alpha = 0.05$), 1.18 ± 0.45 ($p = 0.08$, $\alpha = 0.05$), $4.80 \times 10^{-4} \pm 1.73 \times 10^{-4}$ ($p = 0.05$, $\alpha = 0.05$) A cm^{-2}, respectively. c) *I–V* characteristics measured at different temperatures in the range 224.2–331.0 K. d) For device D8 the *I–V* characteristic is almost temperature independent. e) Resistance *R* between the inner circle and the external part in a CTLM test structure with an inner circle radius *L* and annular space widths *d* for Al/CNT/Ge junctions. f) Benchmark of contact resistivity against the impurity concentration in Ge.

Au/Ti/Al/p-Ge and Au/Ti/Al/CNT/p-Ge devices were also fabricated, demonstrating an increase of the effective Schottky barrier height after the CNT film insertion (Figure S7, Supporting Information).

We used a circular transmission line model (CTLM) method[53] to measure the specific contact resistivity of device D8 (Figure S8, Supporting Information). Figure 2e shows the resistance (R) between the inner circle and the external part as a function of annular space width (d) on Ge substrate. The transfer line length L_T and contact resistance R_c are determined from the intercept of the x- and y-axes as 15.73 μm and 22 Ω, respectively. The sheet resistance R_{sh} obtained from the slope is 637 Ω sq^{-1}. The specific contact resistivity ρ_c is determined from L_T and R_{sh} to be 1.58×10^{-3} Ω cm^2 (Experimental Section). The *I–V* characteristics in Figure S8, Supporting Information also show ohmic contact between the metal and n-Ge after inserting the CNT film.

To benchmark our results, Figure 2f shows the contact resistivity against the impurity concentration in Ge. Our work shows the smallest contact resistance between a metal and a lightly doped n-Ge, providing an effective Fermi-level depinning strategy.

2.3. Mechanism of Fermi-Level Pinning

Our device with the inserted CNT layer provides a platform to investigate the FLP mechanism. For devices with different CNT thicknesses, the contact interface quality between the CNT and Ge hardly changes. For devices D1–D8, as the thickness of the CNT film increases, the MIGS effect of the metal weakens,

leading to the FLP modulation. At the same time the effective Schottky barrier height decreases and the leakage current increases. However, for devices D8–D12, as the thickness of the CNT film increases, the density of CNT film also increases[55] (Figure S2, Supporting Information). The increased electron density of the CNT film increases the MIGS effect,[26] resulting in a decrease in the leakage current.

To support this theory, we designed devices M1–M5 using CNT films with thickness increasing from 2 to 40 nm to form a CNT/n-Ge junction (**Figure 3**a, Experimental Section). The fabricated device array is shown in Figure 3b. 20 devices were measured for each CNT film thickness. With the CNT electrode grounded, *I–V* characteristics for each device showed good uniformity (Figure S9, Supporting Information). The typical *I–V* characteristics in Figure 3c shows that as the thickness of the CNT film increases, the leakage current gradually decreases from device M1 to device M5, indicating that the pinning effect is enhanced as the CNT density increases. The boxplot in Figure 3d and a histogram in Figure S10, Supporting Information further clarify this tendency. In addition, an increased on-current was also observed which is due to a lower series resistance as the CNT thickness increases (Figure 3c,d). Since the quality of the contact interface between the Ge and CNT films with different thicknesses was not changed, the MIGS effect is considered to be responsible for the FLP effect.

2.4. A Planar Diode Array Fabricated at Room Temperature

The proposed CNT layer insertion method is a wafer-scale room-temperature technique for ohmic contact formation for Ge devices, which does not require ion implantation and annealing with the high thermal budget. This is important not only for Ge CMOS aimed at high-performance transistors,[26] but also for multi-functional Ge devices built on the upper layer of a monolithic 3D integration.[56] As a demonstration, a large-area Al/Ge diode array with uniform performances was fabricated in room temperature. After transferring a 14-nm-thick CNT film on to a 2-in. Ge wafer (**Figure 4**a), a planar Al/Ge diode array of 2 × 2 cm^2 was fabricated using a standard photolithography. The Al/Ge diode was composed of an Al/Ge Schottky junction on one side and an Al/CNT/Ge ohmic contact on the other (Figure 4b,c), showing a rectifying characteristic in the dark and a photo response under a 1065-nm laser illumination with a power density of 0.483 W cm^{-2} (Figure 4d and Figure S11, Supporting Information). 100 devices were measured showing a uniform on-to-off current ratio at ±1 V of $2.96 \times 10^4 \pm 6.56 \times 10^3$ ($p = 0.03$, $\alpha = 0.05$, best 4.59×10^4) (Figures S12–S14 and Table S1, Supporting Information). Various Ge photodetectors are widely used in optoelectronic systems,[57–69] and our CNT insertion technique demonstrates the potential to fabricate high-performance

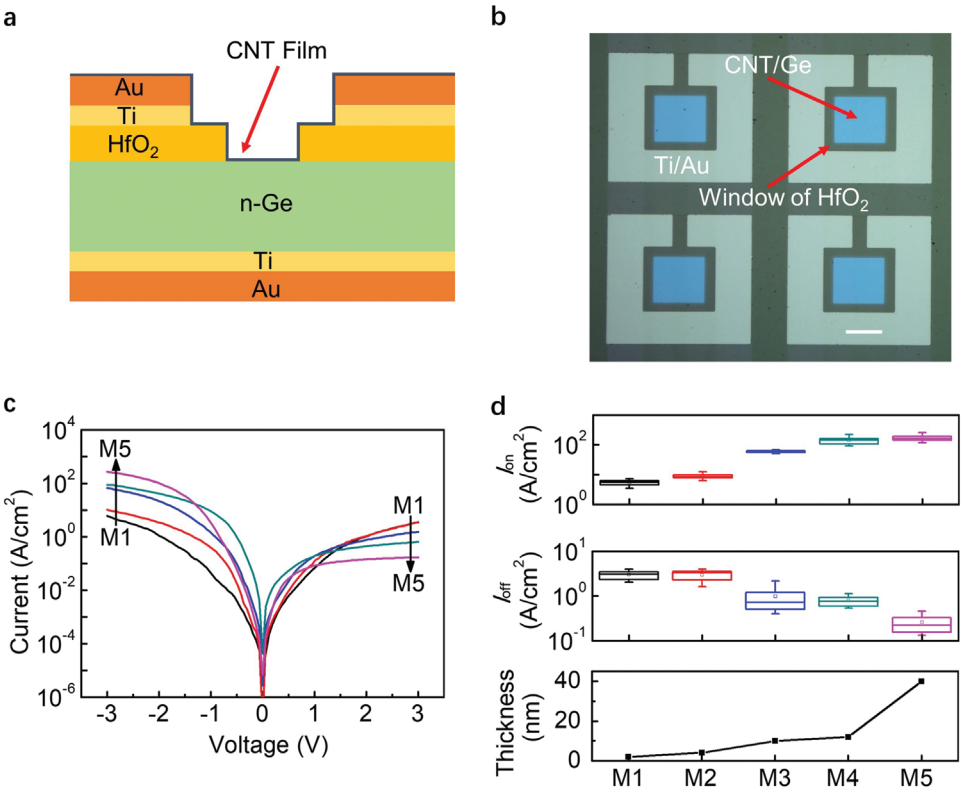

Figure 3. Mechanism of Fermi-level pinning. a) A schematic of a CNT/n-Ge junction. b) An optical image of a CNT/n-Ge junction array (scale bar: 50 µm). c) Typical *I–V* characteristics for devices M1–M5 with CNT thicknesses of 2, 4, 12, 14, and 40 nm. d) Boxplots of on and off current and the CNT thicknesses for devices M1–M5. 20 devices were measured for each CNT film thickness ($n = 20$), showing the on-current of M1–M5 are 5.49 ± 1.07 ($p = 0.47$, $\alpha = 0.05$), 8.75 ± 1.54 ($p = 0.53$, $\alpha = 0.05$), 58.69 ± 4.94 ($p = 0.72$, $\alpha = 0.05$), 140.74 ± 36.22 ($p = 0.43$, $\alpha = 0.05$), 175.64 ± 45.34 ($p = 0.12$, $\alpha = 0.05$) A cm^{-2}, respectively, and the off-current are 2.99 ± 0.58 ($p = 0.13$, $\alpha = 0.05$), 2.98 ± 0.78 ($p = 0.04$, $\alpha = 0.05$), 0.97 ± 0.55 ($p < 0.01$, $\alpha = 0.05$), 0.79 ± 0.19 ($p = 0.20$, $\alpha = 0.05$), 0.26 ± 0.11 ($p = 0.04$, $\alpha = 0.05$) A cm^{-2}, respectively.

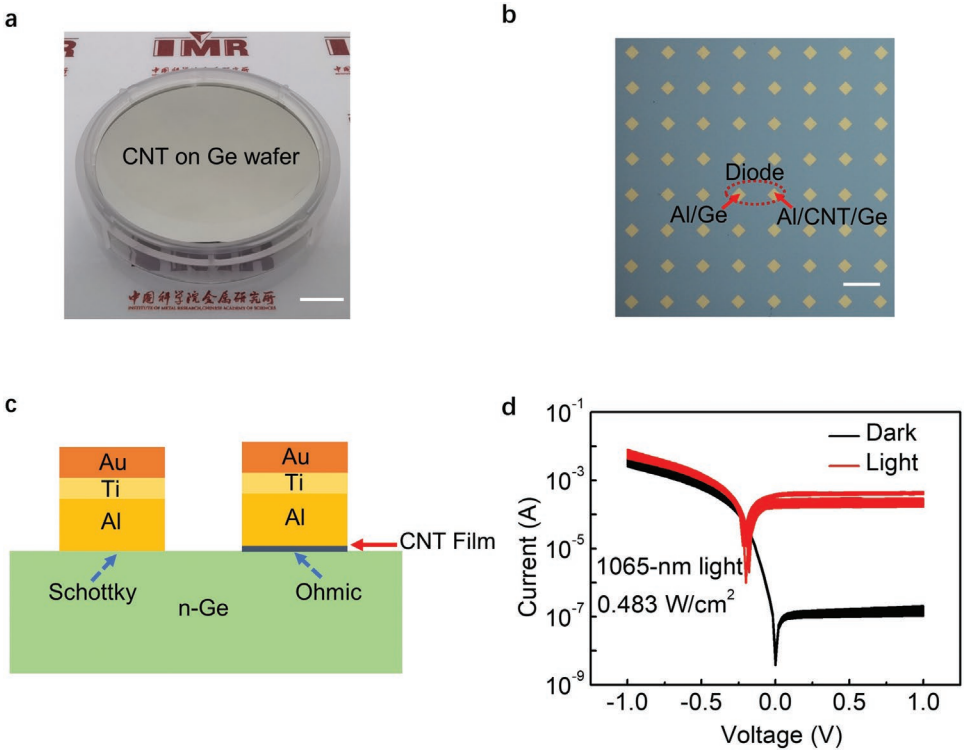

Figure 4. Design of a photovoltaic diodes array. a) An optical image of 2-in. Ge substrate with a transferred wafer-scale CNT film (scale bar: 1 cm). b) An optical image of an array of Al/Ge diodes composed of an Al/Ge junction and an Al/CNT/Ge junction (scale bar: 200 µm). c) Schematic of an Al/Ge diode. d) *I–V* characteristics of 100 Al/Ge diodes in dark and under a 1065-nm laser illumination with a power density of 0.483 W cm^{-2}.

Ge-based photodetectors where ohmic contact can be formed without ion implantation and annealing with high thermal budget.

3. Conclusion

The insertion of a CNT film between metal and n-Ge has been performed to produce Fermi-level depinning. The conductive CNT layer produces a reduced effective Schottky barrier height without inducing a large resistance, leading to a smallest reported contact resistance between a metal and a lightly doped n-Ge. The device platform also shows that the MIGS effect is responsible for the pinning. A wafer-scale planar diode array is fabricated at room temperature demonstrating uniform electrical and optoelectronic properties. The work provides a new way of FLP modulation and obtaining ohmic contact to improve performance of Ge devices and may be also applicable for nano-materials in the future.[70]

4. Experimental Section

Preparation of Ge Substrate: A 1 cm × 1 cm n-Ge (100) (resistivity: 1–5 Ω cm) wafer was used as the substrate. The back surface was scratched for ohmic contact,[52] followed by metallization of Au/Ti (50/5 nm) by electron beam evaporation (EBE). The substrate was ultrasonically cleaned in CMOS-grade acetone and isopropanol (>99.8%) for 5 min, followed by cleaning in dilute HF for 1 min to remove native oxides.

Fabrication of CNT Film: The CNT film was collected on a membrane via a gas-phase filtration system by a FCCVD method.[55] A series of CNT films with different thicknesses of 2, 4, 6, 8, 10, 12, 14, 18, 20, 24, and 40 nm were obtained by using different deposition times of 10 s, 2 min, 2 min and 20 s, 2 min and 40 s, 3 min, 3 min and 20 s, 4 min, 5 min, 6 min, and 12 min. Small bundles of the CNT films were composed of isolated SWCNTs whose diameters were in the range of 1.7–3.0 nm with a mean value of ≈2.2 nm.[48] In the future, CNT films are expected be directly prepared on the Ge substrate to further enhance the uniformity for application in small-size Ge devices with ultra-scaled contact areas.

Transfer of CNT Films: A 1 cm × 1 cm membrane of the collected CNT film was placed onto the Ge substrate. Two to three drops of isopropanol were added to the substrate to obtain close contact between the membrane and the Ge substrate. When the isopropanol evaporated, the membrane was pressed against the substrate to transfer the CNT film onto the Ge substrate. The membrane was then slowly peeled away after the isopropanol had evaporated. By using CNT films produced by different deposition times, films with different thicknesses and densities were produced for insertion in devices D1–D12 (0 to 40 nm).

Fabrication of the Al/CNT/Ge Junction: After CNT transfer, the top electrode metallization of Au/Ti/Al (50/5/150 nm) was made by standard photolithography and EBE. The excess CNT film outside the top electrodes was etched by O_2 plasma (200 W, 180 sccm, 2 min).

Fabrication of CNT/Ge Junction: A 30-nm HfO_2 insulating layer was deposited on top of the Ge substrate by atomic layer deposition (ALD) at 200 °C (precursors: tetrakis(dimethylamido)hafnium ($Hf(NMe_2)_4$) and water), followed by Au/Ti (50/5 nm) metallization of both the top and bottom electrodes. In order to make a HfO_2 window (70 µm × 70 µm), a mask was produced by photolithography and the HfO_2 was etched by a reactive ion etching (RIE) (CF_4 = 50 sccm, 5.0 Pa,

RF power = 100 W, 5 min), followed by dilute HF etching for 30 s. Finally, the CNT films were transferred and patterned.

Effective Schottky Barrier Height Measurement: Analysis was based on the relationship between the junction current and temperature as $\ln(I/T^2) = C - q(\phi_B - V/\eta)/k\cdot(1/T)$, where I is current, T is temperature, C is a constant, q is elementary charge, ϕ_B is effective Schottky barrier height, V is voltage, η is the ideality factor, and k is the Boltzmann constant.[50,53] I–V characteristics of junctions were measured using temperatures of 224.2, 232.5, 241.5, 251.2, 261.7, 273.2, 285.6, 299.3, 314.4, and 331.0 K in vacuum. For each temperature, $\ln(I/T^2)$ was plotted against $1000/T$ for various V biases from 0.1 to 0.3 V (Figure S6, Supporting Information). The slope $-q(\phi_B - V/\eta)/1000k$ was plotted against V, and the y-intercept at 0 V (S_0) is $-q\phi_B/1000k$ from which ϕ_B was obtained.[53,54]

Specific Contact Resistivity Measurement: For device fabrication, a CNT film with the same thickness as D8 was inserted between the Au/Ti/Al electrode and n-Ge. An inner electrode circle with a radius L and an annular region width d of Ge substrate were formed by photolithography and O_2 plasma cleaning (Figure S8, Supporting Information). For device measurement, the four-probe method was used to give the I–V characteristics between the inner circle and the external part to eliminate any parasitic resistance caused by cables and probes.[45] d values were 5.4, 10.4, 13.6, 18.0, and 20.6 µm. For CTLM analysis, the analysis was based on $R = R_{sh}\ (d + 2L_t)/2\pi L$, where R is resistance, R_{sh} is sheet resistance, L_t is transfer length.[53] I–V characteristics of CTLM devices are used to determine R in Figure S8, Supporting Information. The R–d relationship is plotted in Figure 2e, where L_t and R_{sh} are determined from the x-axis interception and slope. Specific contact resistivity ρ_c is calculated by $\rho_c = L_t^2 \cdot R_{sh}$.

Statistical Analysis: After removing few abnormal data caused by critical device defects, data was presented using sample size (n), mean, standard deviation, p and α values using Origin software and Shapiro–Wilk test for normality evaluation. In Figure 2b, for each of the devices with different CNT thicknesses, 20 devices were measured (n = 20), showing leakage currents of D1–D12 were $3.51 \times 10^{-3} \pm 2.17 \times 10^{-3}$ (p = 0.04, α = 0.05), $2.25 \times 10^{-2} \pm 5.58 \times 10^{-3}$ (p = 0.03, α = 0.05), $7.73 \times 10^{-2} \pm 1.64 \times 10^{-2}$ (p = 0.23, α = 0.05), 1.21 ± 0.29 (p = 0.50, α = 0.05), 10.15 ± 2.29 (p = 0.11, α = 0.05), 15.95 ± 2.81 (p = 0.42, α = 0.05), 29.86 ± 5.10 (p = 0.17, α = 0.05), 33.02 ± 6.48 (p = 0.88, α = 0.05), 7.98 ± 1.45 (p = 0.52, α = 0.05), 2.28 ± 0.76 (p = 0.20, α = 0.05), 1.18 ± 0.45 (p = 0.08, α = 0.05), $4.80 \times 10^{-4} \pm 1.73 \times 10^{-4}$ (p = 0.05, α = 0.05) A/cm^{-2}, respectively. In Figure 3d, 20 devices were measured for each CNT film thickness (n = 20), showing the on-current of M1–M5 were 5.49 ± 1.07 (p = 0.47, α = 0.05), 8.75 ± 1.54 (p = 0.53, α = 0.05), 58.69 ± 4.94 (p = 0.72, α = 0.05), 140.74 ± 36.22 (p = 0.43, α = 0.05), 175.64 ± 45.34 (p = 0.12, α = 0.05) A/cm^{-2}, respectively, and the off-current were 2.99 ± 0.58 (p = 0.13, α = 0.05), 2.98 ± 0.78 (p = 0.04, α = 0.05), 0.97 ± 0.55 (p < 0.01, α = 0.05), 0.79 ± 0.19 (p = 0.20, α = 0.05), 0.26 ± 0.11 (p = 0.04, α = 0.05) A/cm^{-2}, respectively. In Figure 4d, 100 diodes on the wafer were measured (n = 100), showing an on-to-off current ratio at ±1 V of $2.96 \times 10^4 \pm 6.56 \times 10^3$ (p = 0.03, α = 0.05).

Characterization: Materials were characterized by an optical microscope (Nikon LV100ND), an SEM (FEI Nova Nano SEM 430 using an accelerating voltage of 2.0 kV), an AFM (Bruker Multimode 8, tapping mode), and a SIMS (ION TOF-SIMS 5). Electrical characteristics were measured using a semiconductor analyzer (Agilent B1500A) and a probe station (Cascade Microtech Inc. 150-PK-PROMOTION) under ambient conditions, and a vacuum probe station (Lake Shore TTPX/TSM1D1001) under low temperature conditions. Optical characteristics were measured using a laser diode controller (Thorlabs ITC4001, with 1065-nm laser) in a darkroom at room temperature.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

Chi.L. and D.-M.S. conceived the project. Y.-N.W. conducted device fabrication assisted by J.-W.Z. X.-G.H. provided CNT films supervised by C.L. Y.-N.W. performed AFM, SEM, and SIMS characterizations assisted by B.T. supervised by J.-H.D. Chi.L. proposed the mechanism of the device. Chi.L., Y.-N.W., and D.-M.S. wrote the paper. All authors discussed the results and commented on the manuscript.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

carbon nanotube films, Fermi-level pinning, germanium, metal-induced gap states, ohmic contacts

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