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All-optical latches using carrier reservoir semiconductor optical amplifiers

Amer Kotb [a,b,*], Kyriakos E. Zoiros [c], Wei Li [a,*]

[a] GPL, State Key Laboratory of Applied Optics, Changchun Institute of Optics, Fine Mechanics, and Physics, Chinese Academy of Sciences, Changchun 130033, China
[b] Department of Physics, Faculty of Science, University of Fayoum, Fayoum 63514, Egypt
[c] Lightwave Communications Research Group, Department of Electrical and Computer Engineering, School of Engineering, Democritus University of Thrace, Xanthi 67100, Greece

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ABSTRACT

Lightwave communication systems, optical random memories, and photonic encryption/decryption are important applications that rely on all-optical latches. For the first time, the carrier reservoir semiconductor optical amplifiers (CR-SOAs) are employed to simulate two basic optical latches, Set-Reset (SR) latch, and D Flip-Flop, at a data rate of 120 Gb/s. All-optical NAND and NOT logic operations are used to build these latches, which are implemented using Mach-Zehnder interferometers (MZIs) with CR-SOAs. In the presence of the amplified spontaneous emission noise, the variation of the output quality factor (Q-factor) against the CR-SOA key operating parameters is studied. This is achieved by exploiting and numerically solving a set of coupled partial differential equations that describe the CR-SOAs gain and phase dynamics when operated as nonlinear elements and embedded in MZIs. The results demonstrate that CR-SOAs-based MZIs can achieve a high Q-factor while implementing the logical SR latch and D Flip-Flop at a high speed of 120 Gb/s.

1. Introduction

Optical latches have attracted research interest due to their importance in a variety of applications, such as optical networks, optical random memories, and photonic encryption/decryption. Their recent implementations have relied on semiconductor optical amplifiers (SOAs), whose finite carrier lifetime limits however operation and performance at modern data rates [1]. To overcome this obstacle, the technology of carrier reservoir semiconductor optical amplifier (CR-SOA) has been proposed as an efficient alternative to conventional SOAs, since it offers faster gain and phase recovery that allows to perform all-optical Boolean functions and subsequently all-optical logic functionalities at higher speeds [2–5]. In this research, we propose to explore CR-SOAs for all-optical latching purposes. Although CR-SOAs have recently been shown to be capable of enabling the execution of all-optical Boolean logic functions [2–5], yet so far this potential has not been explored and demonstrated when these functions are combined to form more complex all-optical circuits. To this aim, in this work, we simulate Set-Reset (SR) latch, and D Flip-Flop at 120 Gb/s return-to-zero (RZ) modulation data using CR-SOAs-based Mach-Zehnder interferometers (MZIs), for the first time to our knowledge. The MZI constitutes the primary candidate for realizing Boolean logic functions due to its attractive features such as stable, compact, simple, efficient operation, and straightforward implementation [6]. These latches are realized using all-optical NAND and NOT logic operations. The NAND logic gate is important in the implementation of any other Boolean logic functions [7] as well as in the construction of complicated combinational logic circuits [8]. The dependence of the quality factor (Q-factor) on the key operating parameters is examined and assessed in the presence of the amplified spontaneous emission (ASE) noise. The results reveal that CR-SOAs-based MZIs can realize the logical SR latch and D Flip-Flop at 120 Gb/s with logical correctness and high Q-factor. This suggests that CR-SOA-based all-optical latching competes favorably with other SOA-based technologies and holds the promise of being established as a viable alternative for the intended purpose.

2. CR-SOA model

Unlike quantum-dot SOAs (QD-SOAs), where the fast response is due to the existence of the wetting layer (WL), which works as a carrier storage layer, CR-SOAs allow to accelerate the operation speed of the application in which they are involved by utilizing the so-called “carrier

* Corresponding authors at: The GPL, State Key Laboratory of Applied Optics, Changchun Institute of Optics, Fine Mechanics, and Physics, Chinese Academy of Sciences, Changchun 130033, China.
E-mail addresses: amer@ciomp.ac.cn (A. Kotb), weili1@ciomp.ac.cn (W. Li).

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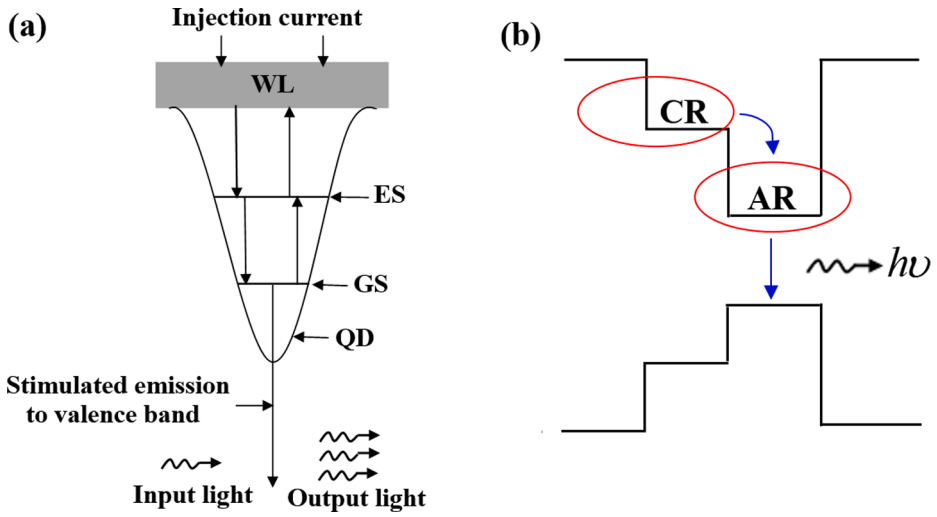


Fig. 1. (a) Energy levels and carrier transitions of QD and (b) band diagram of CR-SOA.

reservoir," but in a different physical method. In QD-SOAs, carriers injected into the WL by the bias current make a transition to the excited state (ES) followed by the transition to the ground state (GS) in the conduction band, as shown in Fig. 1(a) [9]. Carriers in the GS are depleted by the input pulse energy and are quickly replaced by carriers transferred from the WL layer via the ES, thus resulting in a faster response speed [9]. On the other hand, in CR-SOAs, in which the CR region is grown near the active region (AR), as shown in Fig. 1(b) [4,5], the CR region supplies the AR with carriers with nearly the same transition time as that for QD-SOAs, i.e. 0.5–10 ps [4,5]. Because of this ultrafast transition, CR-SOAs have similarly fast gain and phase response as QD-SOAs.

The following are the CR-SOA time-dependent gain equations, which include carrier recombination between CR and AR, as well as the ultrafast intraband effects of the carrier heating (CH) and spectral hole burning (SHB) [4,5]:

$$\frac{dh_{AR}(t)}{dt} = \frac{h_{CR}(t)-h_{AR}(t)}{\tau_t(1+\eta)} + \frac{\eta h_0}{\tau_c(1+\eta)} - \frac{h_{AR}(t)}{\tau_c} - (exp\,[h_{AR}(t) + h_{CH}(t) + h_{SHB}(t)] - 1)\,\frac{P_{in,\ CR-SOA}(t)}{E_{sat}} \quad (1)$$

$$\frac{dh_{CR}(t)}{dt} = -\frac{\eta(h_{CR}(t)-h_{AR}(t)}{\tau_t(1+\eta)} + \frac{h_0-h_{CR}(t)}{\tau_c(1+\eta)} - \frac{h_{CR}(t)}{\tau_c} \quad (2)$$

$$\frac{dh_{CH}(t)}{dt} = -\frac{h_{CH}(t)}{\tau_{CH}} - \frac{\varepsilon_{CH}}{\tau_{CH}}(\exp\,[h_{AR}(t) + h_{CH}(t) + h_{SHB}(t)] - 1)\,P_{in,\ CR-SOA}(t) \quad (3)$$

$$\frac{dh_{SHB}(t)}{dt} = -\frac{h_{SHB}(t)}{\tau_{SHB}} - \frac{\varepsilon_{SHB}}{\tau_{SHB}}(\exp\,[h_{AR}(t) + h_{CH}(t) + h_{SHB}(t)] - 1)\,P_{in,\ CR-SOA}(t) - \frac{dh_{AR}(t)}{dt} - \frac{dh_{CH}(t)}{dt} \quad (4)$$

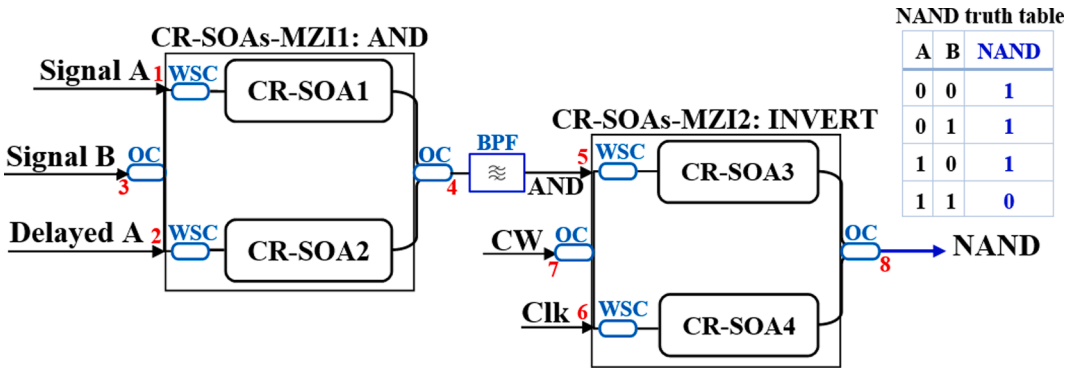
Table 1
Default numerical parameters [2–6,10,12–14].

Symbol	Definition	Value	Unit
E_0	Pulse energy	0.7	pJ
τ_{FWHM}	Pulse width	1	ps
T	Bit period	8.33	ps
N	PRBS length	127	-
$\Delta\tau$	Time delay of delayed data signal A	0.5	ps
I	Injection current	200	mA
P_{sat}	Saturation power	30	mW
τ_c	Carrier lifetime	200	ps
τ_t	Transition lifetime from CR to AR	5	ps
η	Population inversion factor	0.3	-
α	α-factor	5	-
α_{CH}	CH linewidth enhancement factor	1	-
α_{SHB}	SHB linewidth enhancement factor	0	-
ε_{CH}	CH nonlinear gain suppression factor	0.2	W^{-1}
ε_{SHB}	SHB nonlinear gain suppression factor	0.2	W^{-1}
τ_{CH}	Temperature relaxation rate	0.3	ps
τ_{SHB}	Carrier-carrier scattering rate	0.1	ps
Γ	Optical confinement factor	0.3	-
a	Differential gain	Oct-20	m^{-2}
N_{tr}	Transparency carrier density	1024	m^{-3}
L	Length of AR	500	μm
d	Thickness of AR	0.3	μm
w	Width of AR	3	μm
G_0	Unsaturated power gain	30	dB
ω_0	Central optical frequency	193.55	THz
N_{SP}	Spontaneous emission factor	2	-
B_0	Optical bandwidth	2	nm

where the overall integrated gain of the CR-SOA due to carrier recombination between AR and CR, CH, and SHB is represented by the functions h_{AR}, h_{CR}, h_{CH}, and h_{SHB}, respectively. The population inversion factor (η) is defined as the ratio of the carrier densities in the AR and the CR, i.e. $= N_{AR}/N_{CR}$, τ_t is defined as the transition time from the CR to the AR, and τ_c is the carrier lifetime in both the AR and the CR. $h_0 = \ln[G_0]$, where G_0 is the unsaturated power gain given by $G_0 = \Gamma a N_{tr}\,(I\tau_c / eVN_{tr} - 1)$ [10], where G_0 is the unsaturated power gain, Γ is the optical confinement factor, a is the differential gain, N_{tr} is the transparency carrier density, I is the injection current, e is the electron charge, and V is the AR volume given by V = wdL, where w is the AR width, d is the AR thickness, and L is the AR length. $E_{sat} = P_{sat}\,\tau_c = wd\hbar\omega_0/a\Gamma$ [10], where E_{sat} is the saturation energy, P_{sat} is the saturation power, ħ is Planck's constant divided by 2π, and ω_0 is the central optical frequency. The temperature relaxation rates owing to the CH and SHB, respectively, are τ_{CH} and τ_{SHB}. The nonlinear gain suppression factors owing to the CH and SHB, respectively, are ε_{CH} and ε_{SHB}. Inside a pseudorandom binary sequence (PRBS) of length N, the RZ input power pulses ($P_{in,\ CR\text{-}SOA}(t)$) are considered to be Gaussian-shaped with energy E_0, full-wave at half maximum (FWHM) pulse width τ_{FWHM}, and bit period T [2–6]:

$$P_{A,\,B,\,Clk}(t) \equiv P_{in,\ CR-SOA}(t) = \sum_{n=1}^{N} a_{n(A,B,Clk)}\frac{2\sqrt{\ln[2]}\,E_0}{\sqrt{\pi}\,\tau_{FWHM}}\exp\left[-\frac{4\ln[2](t-nT)^2}{\tau_{FWHM}^2}\right] \quad (5)$$

where $\alpha_{n(A,B,Clk)}$ represents the *n*-th bit-long PRBS data streams A, B, or a clock signal (Clk), i.e. $\alpha_{n(A,B)} = 0$, 1, or $\alpha_{n(Clk)} = 1$.



NAND truth table

A	B	NAND
0	0	1
0	1	1
1	0	1
1	1	0

Fig. 2. Schematic and truth table of NAND gate using CR-SOAs-MZIs. OC: 3 dB optical coupler. WSC: wavelength selective coupler. BPF: bandpass filter. CW: continuous wave beam. Clk: clock signal (all '1's).

The sum of h_{AR}, h_{CH}, and h_{SHB} is the overall gain of each i-th CR-SOA, i.e. [3–5]:

$$G_{CR-SOA_i}(t) = \exp\left[h_{AR}(t) + h_{CH}(t) + h_{SHB}(t)\right],\ i = 1,2,3,4 \tag{6}$$

The induced phase change of each i-th CR-SOA is given by [3–5]:

$$\phi_{CR-SOA_i}(t) = -0.5\ (\alpha\, h_{AR}(t) + \alpha_{CH}\, h_{CH}(t)),\ i = 1,2,3,4 \tag{7}$$

where α is the traditional linewidth enhancement factor (α-factor) and α_{CH} is the linewidth enhancement factor for CH. The equivalent contribution of SHB is zero, as predicted by Eq. (7), i.e. $\alpha_{SHB} \sim 0$ [2–5].

The Q-factor [2–6] is employed in this numerical investigation to evaluate the performance of the considered optical functions. The Q-factor has been employed as the performance evaluation criterion for two main reasons, namely because a) it is directly associated to the bit error rate (BER), which is the ultimate performance measurement metric, and b) by definition it characterizes the response of a circuit for the entire length of the input data patterns, thereby allowing to investigate and assess its performance when its operation is heavily stressed [11]. To obtain acceptable performance, the Q-factor value must be greater than 6 to keep the corresponding BER [12] less than 10^{-9} [2–5]. The Adams numerical approach implemented in Wolfram Mathematica® is used to solve all time-dependent equations using the default numerical parameters listed in Table 1 [2–6,10,12–14].

3. NAND gate

The all-optical NAND gate is constructed by a series combination of AND and INVERT logic operations, which are achieved using CR-SOAs-MZI1 and CR-SOAs-MZI2, respectively, as illustrated in Fig. 2 [2,4]. To implement the AND gate, data signal A from port 1 and its delayed version from port 2 at 1550 nm wavelength are injected into CR-SOA1 and CR-SOA2 placed in the MZI's upper and lower arms, respectively. Concurrently, data signal B at 1555 nm wavelength is divided by a 3 dB optical coupler (OC) into two equal parts to be launched into CR-SOA1 and CR-SOA2, through the MZI's middle arm from port 3. Signal A and delayed signal A create a phase window perceived by the co-propagating components of signal B. Thus, if A = '0' and B = '1' or B = '0', no phase window is produced, and so the MZI output is '0'. Similarly, if A = '1' and B = '0', there is no signal on which to map the incurred differential phase and thus the MZI output is also '0'. However, if A = '1' and B = '1', then the existence of the phase window makes signal B constituents interfere constructively at the CR-SOAs-MZI1 output, producing a logical '1'. Therefore, output '1' is obtained only if both logic inputs are '1', which corresponds to the AND logic gate. The next serial building step is the INVERT (NOT) operation, which is similar to the XOR if one of the logic inputs is a Clk (all '1's). Then the output from the AND gate, which is spectrally selected using a bandpass filter (BPF) centered at 1555 nm, is injected into CR-SOA3 of CR-SOAs-MZI2. A Clk signal at 1555 nm is injected into CR-SOA4 from port 6. Concurrently a continuous wave (CW) beam at 1550 is injected into both CR-SOA3 and CR-SOA4 from port 7 to map the gain dynamics perturbation and convert it to amplitude change transferred at the output. According to the relevant truth table attached to Fig. 2, the result in this manner is logic A NAND B from port 8.

To execute the AND operation numerically, the input optical powers entered into CR-SOA1 and CR-SOA2 are expressed as [2,4]:

$$P_{in,\,CR-SOA_1}(t) = P_A(t) + 0.5\,P_B(t) \tag{8}$$

$$P_{in,\,CR-SOA_2}(t) = P_A(t-\Delta\tau) + 0.5\,P_B(t) \tag{9}$$

where $\triangle\tau$ is the temporal offset of delayed data signal A. The coefficient 0.5 denotes the signal B being divided as it enters the middle port of CR-SOAs-MZI1. Then, at the CR-SOAs-MZI1 output, the power of the AND operation is given by [2,4]:

$$P_{AND}(t) = 0.25\,P_B(t)\left(G_{CR-SOA_1}(t) + G_{CR-SOA_2}(t) - 2\sqrt{G_{CR-SOA_1}(t)\,G_{CR-SOA_2}(t)}\,\cos\left[\Phi_{CR-SOA_1}(t) - \Phi_{CR-SOA_2}(t)\right]\right) \tag{10}$$

where the total gains and phase shifts of CR-SOA1 and CR-SOA2 are denoted by $G_{CR\text{-}SOA1,2}(t)$ and $\Phi_{CR\text{-}SOA1,2}(t)$, respectively.

In order to execute the INVERT operation, the input signal powers into CR-SOA3 and CR-SOA4 are expressed as follows [2,4]:

$$P_{in,\,CR-SOA_3}(t) = P_{AND}(t) + 0.5\,P_{CW} \tag{11}$$

$$P_{in,\,CR-SOA_4}(t) = P_{Clk}(t) + 0.5\,P_{CW} \tag{12}$$

The coefficient 0.5 denotes the CW beam being divided as it enters the middle port of CR-SOAs-MZI2. Then, the power of the NAND operation at CR-SOAs-MZI2 output is given by [2,4]:

$$P_{NAND}(t) = 0.25\,P_{CW}\left(G_{CR-SOA_3}(t) + G_{CR-SOA_4}(t) - 2\sqrt{G_{CR-SOA_3}(t)\,G_{CR-SOA_4}(t)}\,\cos\left[\Phi_{CR-SOA_3}(t) - \Phi_{CR-SOA_4}(t)\right]\right) \tag{13}$$

where the total gains and phase shifts of CR-SOA3 and CR-SOA4 are $G_{CR\text{-}SOA3,4}(t)$ and $\Phi_{CR\text{-}SOA3,4}(t)$, respectively.

4. SR latch

The SR latch is one of the most fundamental sequential logic circuits. The SR latch is a one-bit memory-bistable device with two inputs: one to

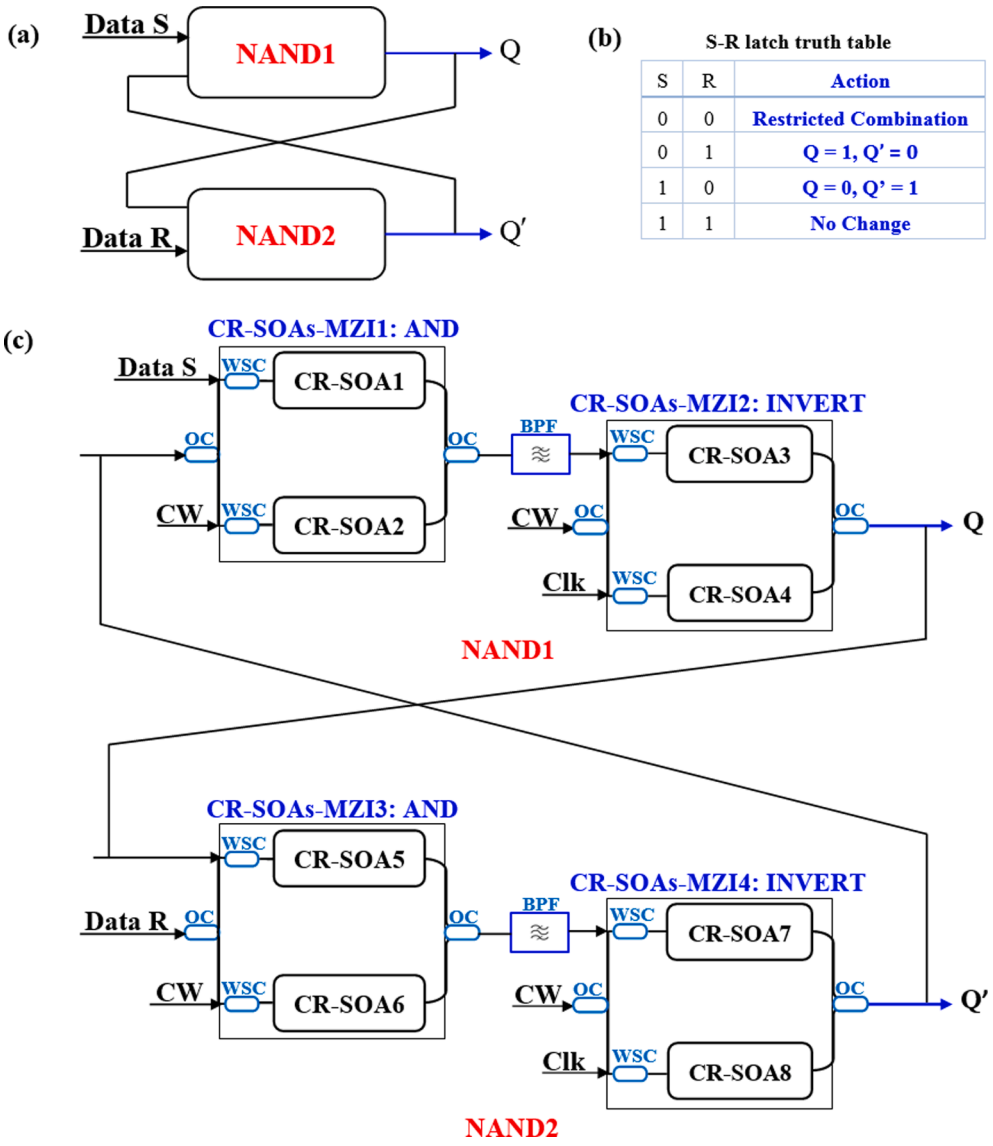


Fig. 3. (a) Block diagram of SR latch using 2-input NAND operations, (b) truth table of SR latch, and (c) schematic diagram of SR latch implementation using CR-SOAs-MZIs.

'SET' the device (which means the output Q = '1′), and the other to 'RESET' the device (which means the output Q = '0′). The reset input returns the Flip-Flop to its initial state, with an output Q that is either at logic level '1′ or logic level '0′, depending on the set/reset situation. 2-input NAND logic gates connected together is the simplest approach to build a SR latch. Fig. 3 shows the diagrams and truth table for the SR latch based on two NAND logic operations using CR-SOAs-based MZIs. It's worth noting that when both data inputs R and S are '1′, Q does not change from the prior state; Q remains '0′ or '1′ based on the preceding Q's result.

The total input powers to CR-SOAs-MZI1 and CR-SOAs-MZI2 for the optical NAND1 gate are calculated as follows:

$$P_{in,\,CR-SOA_1}(t) = P_S(t) + 0.5\,P_{Q'}(t) \tag{14}$$

$$P_{in,\,CR-SOA_2}(t) = P_{CW} + 0.5\,P_{Q'}(t) \tag{15}$$

$$P_{in,\,CR-SOA_3}(t) = P_{AND}(t) + 0.5\,P_{CW} \tag{16}$$

$$P_{in,\,CR-SOA_4}(t) = P_{Clk}(t) + 0.5\,P_{CW} \tag{17}$$

For the NAND2 operation, the total input powers going into CR-SOAs-MZI3 and CR-SOAs-MZI4 are expressed as:

$$P_{in,\,CR-SOA_5}(t) = P_Q(t) + 0.5\,P_R(t) \tag{18}$$

$$P_{in,\,CR-SOA_6}(t) = P_{CW} + 0.5\,P_R(t) \tag{19}$$

$$P_{in,\,CR-SOA_7}(t) = P_{AND}(t) + 0.5\,P_{CW} \tag{20}$$

$$P_{in,\,CR-SOA_8}(t) = P_{Clk}(t) + 0.5\,P_{CW} \tag{21}$$

The output powers of the MZIs for the AND and NAND operations are given in Eqs. (10) and (13), respectively.

5. Flip-Flop function

The D Flip-Flop is a common building component for logic functions. A memory cell, a zero-order hold, or a delay line can all be used to describe the D Flip-Flop. It captures the value of the data input D at a definite portion of the gate cycle, resulting in the output Q. At other times instants when D = '1′ and G = '0′, the output Q does not change; Q remains '0′ or '1′ based on the previous output state. Two logic functions NAND and NOT are used to build the D Flip-Flop. The diagrams and the

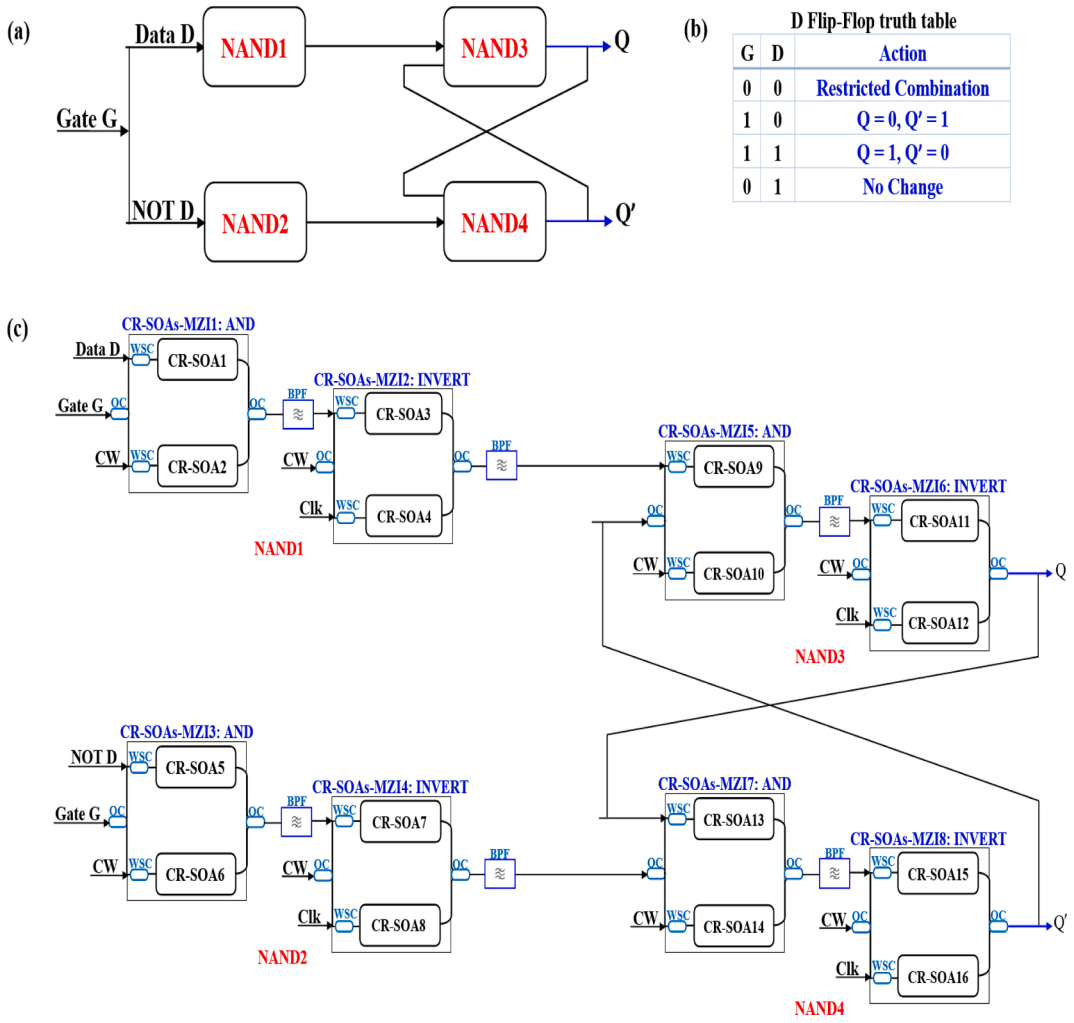


Fig. 4. (a) Block diagram of D Flip-Flop, (b) truth table of D Flip-Flop, and (c) schematic diagram of D Flip-Flop implementation using CR-SOAs-MZIs.

truth table of D Flip-Flop using CR-SOAs-MZIs are shown in Fig. 4.

For NAND1 operation, the total input powers to CR-SOAs-MZI1 and CR-SOAs-MZI2 are formulated as follows:

$$P_{in,\,CR-SOA_1}(t) = P_D(t) + 0.5\,P_G(t) \quad (22)$$

$$P_{in,\,CR-SOA_2}(t) = P_{CW} + 0.5\,P_G(t) \quad (23)$$

$$P_{in,\,CR-SOA_3}(t) = P_{AND}(t) + 0.5\,P_{CW} \quad (24)$$

$$P_{in,\,CR-SOA_4}(t) = P_{Clk}(t) + 0.5\,P_{CW} \quad (25)$$

For NAND2 operation, the total input powers to CR-SOAs-MZI3 and CR-SOAs-MZI4 are formulated as follows:

$$P_{in,\,CR-SOA_5}(t) = P_{NOT\,D}(t) + 0.5\,P_G(t) \quad (26)$$

$$P_{in,\,CR-SOA_6}(t) = P_{CW} + 0.5\,P_G(t) \quad (27)$$

$$P_{in,\,CR-SOA_7}(t) = P_{AND}(t) + 0.5\,P_{CW} \quad (28)$$

$$P_{in,\,CR-SOA_8}(t) = P_{Clk}(t) + 0.5\,P_{CW} \quad (29)$$

For NAND3 operation, the total input powers to CR-SOAs-MZI5 and CR-SOAs-MZI6 are formulated as follows:

$$P_{in,\,CR-SOA_9}(t) = P_{NAND1}(t) + 0.5\,P_{Q'}(t) \quad (30)$$

$$P_{in,\,CR-SOA_{10}}(t) = P_{CW} + 0.5\,P_{Q'}(t) \quad (31)$$

$$P_{in,\,CR-SOA_{11}}(t) = P_{AND}(t) + 0.5\,P_{CW} \quad (32)$$

$$P_{in,\,CR-SOA_{12}}(t) = P_{Clk}(t) + 0.5\,P_{CW} \quad (33)$$

For NAND4 operation, the total input powers to CR-SOAs-MZI7 and CR-SOAs-MZI8 are formulated as follows:

$$P_{in,\,CR-SOA_{13}}(t) = P_Q(t) + 0.5\,P_{NAND2}(t) \quad (34)$$

$$P_{in,\,CR-SOA_{14}}(t) = P_{CW} + 0.5\,P_{NAND2}(t) \quad (35)$$

$$P_{in,\,CR-SOA_{15}}(t) = P_{AND}(t) + 0.5\,P_{CW} \quad (36)$$

$$P_{in,\,CR-SOA_{16}}(t) = P_{Clk}(t) + 0.5\,P_{CW} \quad (37)$$

6. Results

The SR latch and the D Flip-Flop are generated using similar NAND logic operations. In the SR latch, the input set/rest pulses pass through two NAND operations while in the D Flip-Flop the input data/gate pulses pass through four NAND operations. Although the input signals undergo long different amounts of nonlinear logic processes, the output Q pulses are not tainted by a noise accumulation or time jitter due to the faster response of the CR-SOA, resulting in open and clear eye diagrams. The output eye diagrams with the respective Q-factors using CR-SOAs-based MZIs at 120 Gb/s for the NAND operation, SR latch, and D Flip-Flop are plotted in Figs. 5, 6, and 7, respectively. The calculated Q-factors for the

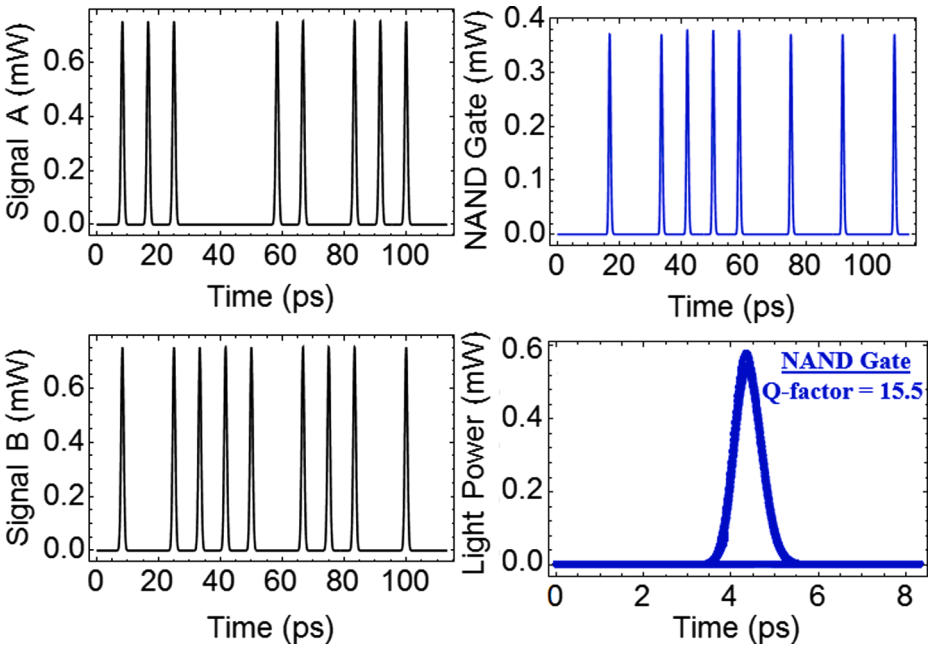


Fig. 5. Numerical results for output NAND function using CR-SOAs-MZIs at 120 Gb/s.

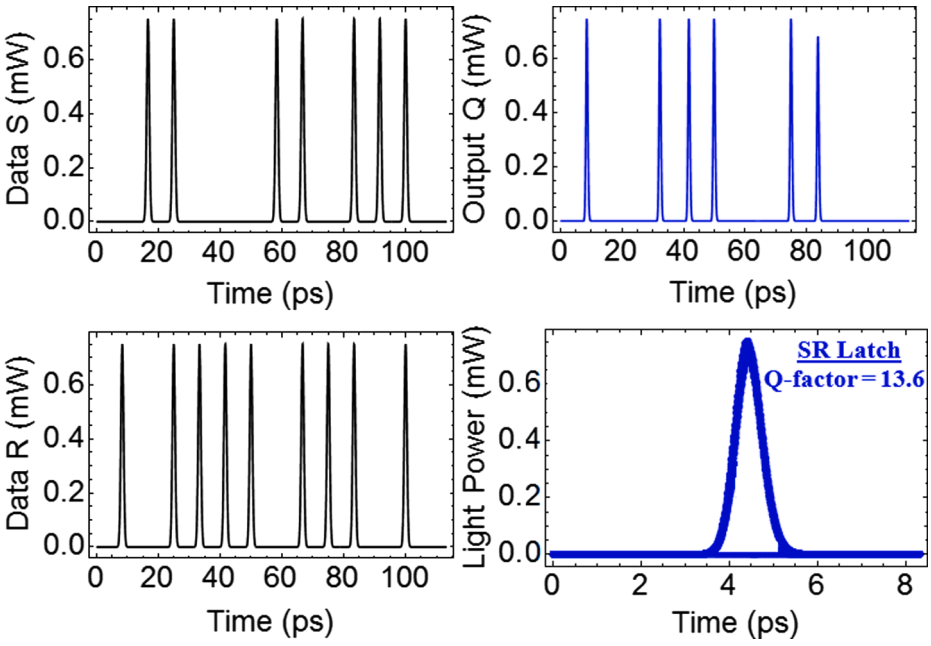


Fig. 6. Numerical results for SR latch (output Q) using two NAND operations with CR-SOAs-MZIs at 120 Gb/s.

NAND gate, SR latch, and D Flip-Flop are, respectively, 15.5, 13.6, and 10.7, which represent very low BER.

Fig. 8 shows the dependence of the Q-factor on the injection bias current and input pulse energy for the NAND gate, SR latch, and D Flip-Flop employing CR-SOAs-based MZIs at 120 Gb/s. When a higher current is applied, more carriers are injected into the CR layer. This allows for faster recovery and refilling of the AR layer after it has been depleted by a powerful input pulse. Accordingly, the Q-factor is increased, as illustrated in Fig. 8(a). On the other hand, when the input pulse energy is increased, a stronger carrier depletion is caused and hence the Q-factor is reduced. Nevertheless, owing to the CR layer in the CR-SOA, the Q-factor remains acceptable practically for the whole range of input pulse energies, as shown in Fig. 8(b).

Fig. 9 shows the Q-factor versus the input pulse width (τ_{FWHM}) for the D Flip-Flop using CR-SOAs-MZIs at 120 Gb/s for three different input pulse shapes, including Secant hyperbolic, Gaussian, and Lorentzian [15]. Overall, the Q-factor is decreased by increasing the pulse width because two neighboring pulses tend to overlap for wider τ_{FWHM}. Comparing among the three pulse shapes, it is clearly observed that a higher Q-factor is achieved by Secant hyperbolic [16] and a lower Q-factor is achieved by Lorentzian pulse.

A time-dependent phase change leads to a variation in the pulse's frequency chirp ($\Delta\upsilon$), which is given by $\Delta\upsilon = \frac{\alpha}{4\pi}\frac{dh}{dt}T = |E_{out}|^2/|E_{in}|^2$ [10]. The effect of frequency chirping on the performance of the NAND gate, SR latch, and D Flip-Flop is analyzed theoretically using CR-SOAs-MZIs at 120 Gb/s, as depicted in Fig. 10. This figure shows that when the chirp

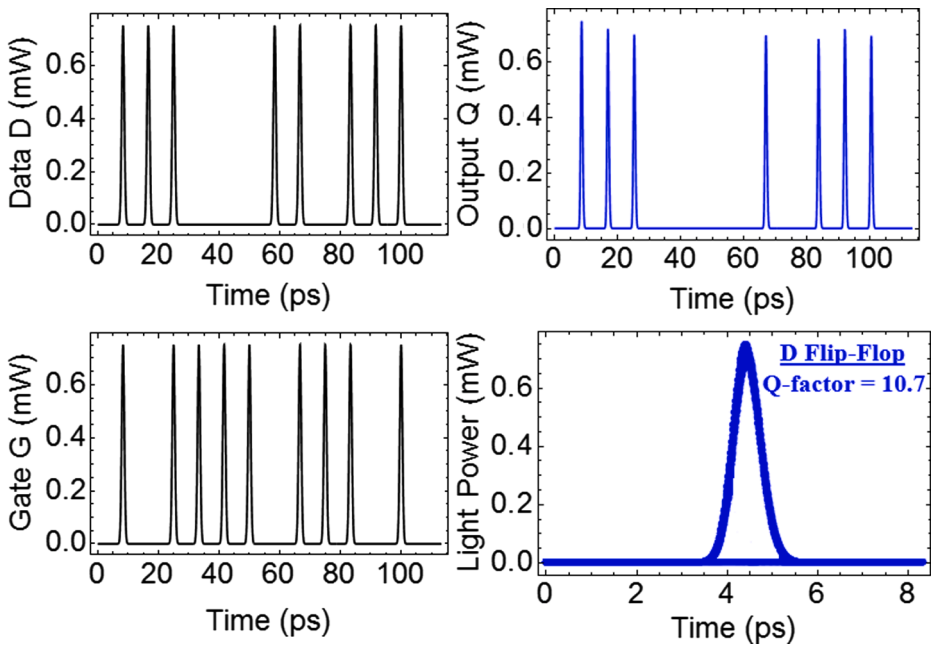


Fig. 7. Numerical results for D Flip-Flop (output Q) using four NAND operations with CR-SOAs-MZIs at 120 Gb/s.

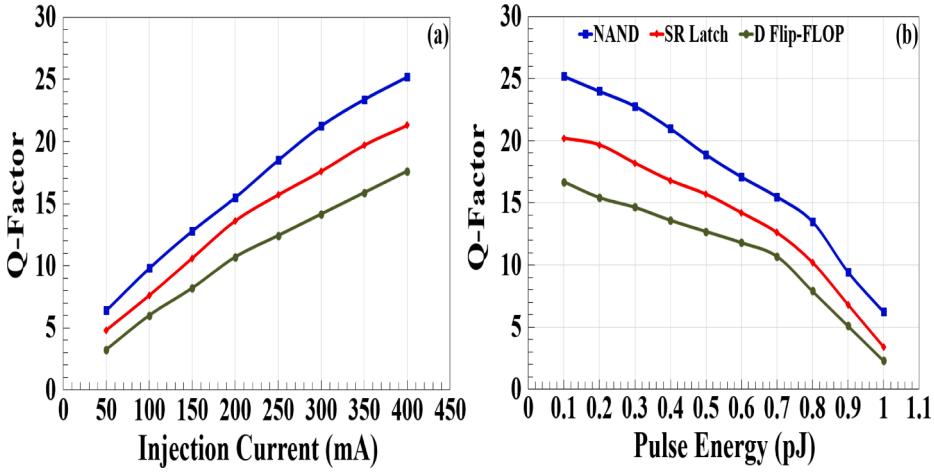


Fig. 8. Q-factor of NAND gate, SR latch, and D Flip-Flop employing CR-SOAs-MZIs at 120 Gb/s as a function of (a) injection current and (b) input pulse energy.

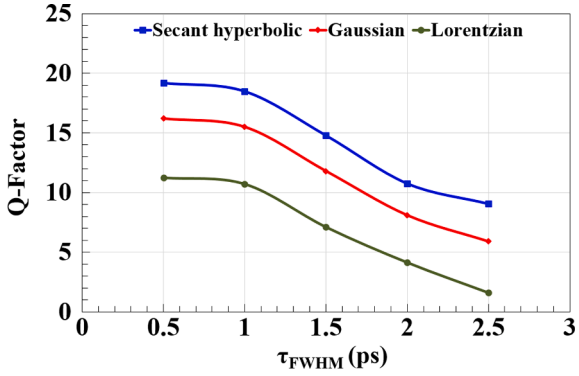


Fig. 9. Q-factor of D Flip-Flop employing CR-SOAs-MZIs at 120 Gb/s as a function of pulse width (τ_{FWHM}) for three different input pulse shapes.

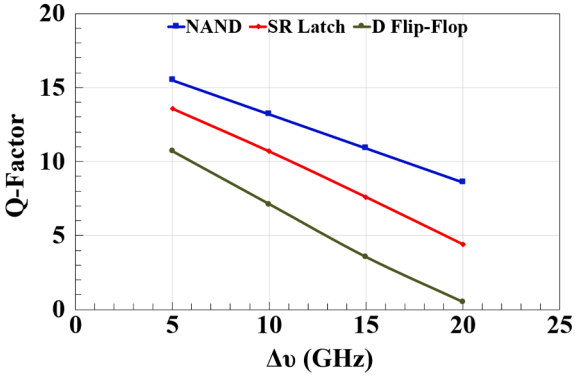


Fig. 10. Q-factor of NAND gate, SR latch, and D Flip-Flop employing CR-SOAs-MZIs at 120 Gb/s as a function of frequency chirp ($\Delta\upsilon$).

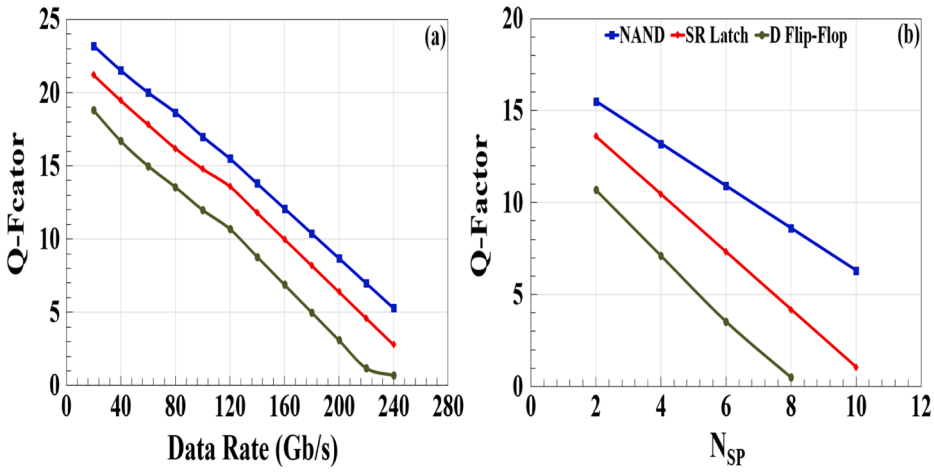


Fig. 11. Q-factor of NAND gate, SR latch, and D Flip-Flop employing CR-SOAs-MZIs at 120 Gb/s as a function of (a) operating data rate and (b) spontaneous emission factor (N_{SP}).

is increased, the Q-factor is reduced. The Q-factor remains acceptable even at high chirp owing to the CR layer in the CR-SOA, resulting in a faster response. In fact, it is possible to compensate for the added chirp by passing the output signal through an optical delayed interferometer [17] or an appropriate filter such as a fiber Bragg grating [18].

CR-SOA is expected to operate at higher speeds while maintaining acceptable performance. For this reason, the variation of the Q-factor with the operating data rate for each NAND gate, SR latch, and D Flip-Flop using CR-SOAs-assisted MZIs at 120 Gb/s is examined and shown in Fig. 11(a). The considered optical gates achieve an acceptable Q-factor at high rates, thanks to the rapid transitions enabled by the CR layer. For example, the NAND gate has a Q-factor = 7 at a rate of 220 Gb/s, SR latch has a Q-factor = 6.4 at 200 Gb/s, and D Flip-Flop has a Q-factor = 6.9 at 160 Gb/s. Operation at higher data rates is feasible if the CR-SOA is biased with a higher current (~ 300 mA) and the energy of the input pulses is lowered (~ 0.3 pJ). Since CR-SOAs introduce ASE noise, the contribution of this effect should also be taken into account. $P_{ASE} = N_{SP}\,(G_0 - 1)\,2\pi\hbar\upsilon B_0$ [10] is used to calculate and mathematically add the ASE noise to the output powers. The previous results were obtained under favorable CR-SOAs working conditions, i.e. $N_{SP} = 2$. The noise term is added to the average intensities of the output bits '0′ and '1′ via ASE. As a result, a greater ASE (i.e. a higher N_{SP}) increases the average value of '0′ and thus lowers the Q-factor. 8 CR-SOAs are interconnected to perform the SR latch, while 16 CR-SOAs are interconnected to perform the D Flip-Flop. Thus, in this simulation, the ASE noise was calculated for each CR-SOA separately and then aggregated to obtain the total ASE extracted from each scheme, as shown in Fig. 11(b). The NAND function has a Q-factor = 6.3 at a high $N_{SP} = 10$, SR latch has a Q-factor = 7.3 at $N_{SP} = 6$, and D Flip-Flop has a Q-factor = 7.1 at $N_{SP} = 4$. This is conceivable because ASE is inhibited by the CR-SOA's faster gain dynamics.

The primary findings of our study could be applied to the experimental verification of the suggested logic structures utilizing CR-SOAs, if the necessary technology is available. Controlling 1) the peak input data power level and 2) the degree of the phase difference between the MZI arms would be necessary to do this. This is more a technology issue that can be resolved in practice rather than a fundamental impediment. Erbium-doped fiber amplifiers, which are commercially available, can handle issue 1. However, for issue 2, the differential phase should be adjusted to fall within the necessary range depending on the binary combination of the input data and the expected logic output from each target gate's truth table [19]. To do this, active phase shifters can be used after each CR-SOA to add a phase difference between the upper and lower MZI arms [20] for efficient switching. These shifters can be integrated onto the same planar lightwave circuit substrate as the CR-SOAs-based devices [21] and are thermo-optic elements with low tuning voltage and power dissipation [22]. With the exception of the OR gate, for which the necessary DI is also technologically feasible [23], these rules apply to the considered logic gates.

Table 2
Comparison of optical latches realizations for different SOAs-based schemes and data rates.

Scheme	Data rate (Gb/s)	Q-factor	Ref.
SOA-TPA:			
SR latch	100	11.8	[6]
	160	11	[6]
	250	10.2	[6]
D Flip-Flop	100	11	[6]
	160	10.7	[6]
	250	9	[6]
QD-SOA:			
SR latch	100	12	[13]
	160	10.8	[13]
	250	9	[13]
D Flip-Flop	100	11.4	[13]
	160	10	[13]
	250	8.2	[13]
CR-SOA:			
SR latch	60	17.8	This work
	120	13.6	This work
	180	8.2	This work
D Flip-Flop	60	15	This work
	120	10.7	This work
	180	6.2	This work

Finally, the proposed CR-SOA-based optical latching scheme was compared to other SOA-based schemes and data rates that have been reported on the considered logic functionality, as shown in Table 2. The benefits of using the CR-SOAs-MZIs scheme to execute the SR latch and D Flip-Flop at 120 Gb/s with a high Q-factor are highlighted in this table. Placing QDs in the SOA's active region [9,13] or making use of the potential of nonlinear phenomena like two-photon absorption (TPA) [2,6], can enhance operating data rates further while maintaining acceptable logic performance.

7. Conclusion

In this paper, we modeled the SR latch and D Flip-Flop at 120 Gb/s using two all-optical logic NAND and NOT operations, which were realized using CR-SOAs-assisted MZIs. The performance of the considered operations was evaluated by the Q-factor. The variation of the Q-factor against various key operating parameters, including the impact of

ASE noise, was examined and assessed. The results showed that employing CR-SOAs as nonlinear elements can help realize the SR latch and D Flip-Flop at high speeds with logical correctness and high Q-factor. The performance of the proposed latches was also compared to previous works, and showed that the former can compete favorably against the latter owing to CR-SOAs inherent advantages. The obtained results extend CR-SOAs suite of all-optical logic functionalities to include advanced circuit level applications, and enhance their capability for serving this purpose as efficient nonlinear elements.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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