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All-optical half adder using carrier reservoir semiconductor optical amplifiers at 120 Gb/s

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Abstract. In this paper, carrier reservoir semiconductor optical amplifiers (CR-SOAs) are employed for the first time to design an all-optical (AO) half adder at 120 Gb/s. The CR-SOAs are incorporated in Mach–Zehnder interferometers (MZIs) configured as XOR and AND gates to execute the required SUM and CARRY logic functions, respectively. The performance of the half adder is evaluated through the quality factor (Q-factor), whose variation against the CR-SOA's critical operating parameters, including amplified spontaneous emission noise, is theoretically investigated. The simulation results show that MZIs with CR-SOAs can implement an AO half adder running at 120 Gb/s with a high Q-factor.

Keywords. All-optical half adder; carrier reservoir semiconductor optical amplifier; Mach–Zehnder interferometer; quality factor.

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1. Introduction

In digital electronics, the half adder is a fundamental combinational circuit that serves as the basis for building more complex processing circuits, such as full adders, binary decoders, binary counters and shift registers [1]. Its significance is also universal in the optical domain, in which the research path intensively followed to implement half adders utilising light, i.e. all-optically (AO), has relied on the technology of semiconductor optical amplifiers (SOAs), either stand-alone [2–5], or incorporated in interferometric architectures [6–8]. However, conventional SOAs suffer from the slow gain recovery time [9] that impedes their use for higher data rate applications intended to meet the expanded information needs of modern telecommunication networks and systems. Recently, the novel version of carrier reservoir (CR) SOAs has been proposed as a viable option for implementing basic AO logic gates at higher speeds and with better performance [10–12]. The presence of a CR layer near the active region (AR) enables these improvements by supplying the latter with carriers with transition durations as fast as 0.5–10 ps [13], considerably speeding up the CR-SOA gain dynamics. For the first time, an AO half adder with CR-SOAs-assisted Mach–Zehnder interferometers (MZIs) for 120 Gb/s return-to-zero (RZ) data is proposed and theoretically analysed in this study. One CR-SOA-MZI is utilised to form an AO XOR gate, which produces the SUM logic function, while another CR-SOAs-MZI is utilised to create an AO AND gate, which produces the CARRY logic function. The quality factor (Q-factor) is used as a performance metric to evaluate the operation of the AO half adder. Its change with the CR-SOA fundamental operating parameters is examined in the presence of the amplified spontaneous emission (ASE) noise to get more realistic findings. These findings show that by utilising MZIs with CR-SOAs, an AO half adder can be realised at 120 Gb/s having a high Q-factor and high-quality logic outcome. The work can enhance light-based technologies intended to support current and future photonic applications [14].

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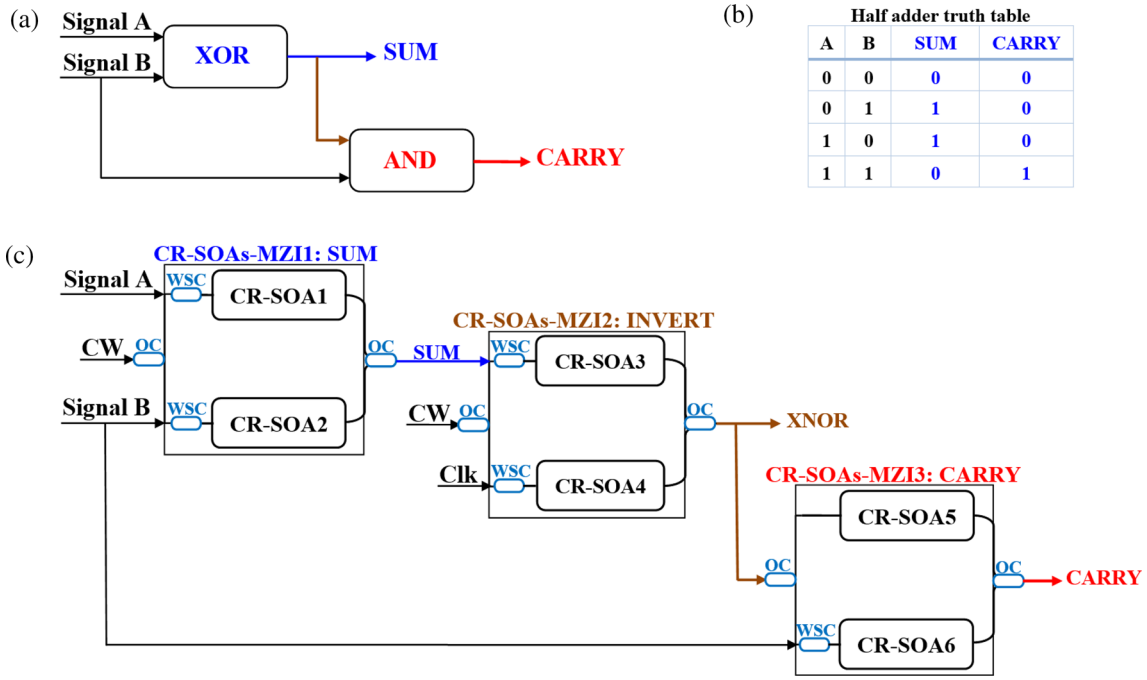

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Figure 1. (**a**) Block diagram of half adder with SUM and CARRY functions through XOR and AND gates, respectively, (**b**) truth table and (**c**) AO half adder circuit using CR-SOAs-MZIs.

2. Half adder using CR-SOAs

SUM and CARRY are two logic functions necessary to realise a binary half adder [1]. The logical outcome of the SUM function is '1' when only both inputs are '1' and '0', which is equivalent to the Boolean XOR operation. The logical outcome of the CARRY function is '1' when only both inputs are '1', which is equivalent to the Boolean AND gate. In this AO scheme, the SUM is generated by CR-SOAs-MZI1 and passed to CR-SOAs-MZI2 along with a clock signal (Clk) and a continuous wave (CW) light to achieve the XNOR gate. Then, the CR-SOAs-MZI2 output is coupled as an incoming probe signal with data signal B (or data signal A) into CR-SOAs-MZI3 to generate the CARRY. The block diagram, truth table and AO circuit of the half adder with SUM and CARRY functions implemented using CR-SOAs-based MZIs are shown in figures 1a–1c, respectively.

To produce the logic SUM, the upper and lower wavelength selective couplers (WSCs) inject the pulses of signals A and B serving as pumps into CR-SOA1 and CR-SOA2, respectively. A 3 dB optical coupler (OC) is also employed to inject a CW light as a probe into the CR-SOAs-MZI1 middle arm. The phases of the CW beams are shifted due to the nonlinear cross-phase modulation (XPM) effect caused by signals A and B in CR-SOAs. As a result, if the binary content of data signals A and B differs, the phase shift between the CW beams also varies, causing constructive interference at the CR-SOA-MZI1 output, producing a '1'. If signals A and B are the same, the phase shift of the halved CW beams interferes destructively at CR-SOA-MZI1 output, resulting in a '0'. In this manner, the logic SUM is obtained between signals A and B, as shown in the corresponding truth table.

The SUM output is sent to CR-SOA3 of CR-SOAs-MZI2 to perform the INVERT operation to implement the logic CARRY function. For this purpose, a Clk signal is launched via a 3 dB OC into CR-SOA4, while a CW light is injected via a WSC into the CR-SOAs-MZI2 middle arm. Consequently, the CR-SOAs-MZI2 output port implements the A XNOR B logic function. The XNOR result is then injected by a 3 dB OC into the CR-SOAs-MZI3 middle arm, where it is separated into two equal parts, while signal B is launched via a WSC into the CR-SOAs-MZI3 lower arm, i.e. CR-SOA6. Signal B opens a phase window via XPM on the XNOR input components. Thus, if signal B is '0', there is no such phase window, and so CR-SOAs-MZI3 output is '0' regardless of whether incoming XNOR is '1' or '0'. When B is '1' but the XNOR output is '0', there is no signal on which to map the incurred differential phase shift. Therefore, the CR-SOAs-MZI3 output is '0'. Because there is no signal on which to map the incurred differential phase shift when B is '1' but the XNOR output is '0', CR-SOAs-MZI3 output is '0'. If B and XNOR are both '1', the created phase window makes the XNOR

components interfere constructively at the CR-SOAs-MZI3 output, resulting in '1'. In this manner, the logic CARRY function between signals A and B is realised. The produced logic SUM and logic CARRY functions can also be combined to form the logic OR function [15], which is the operating advantage of the proposed scheme.

The time-dependent gain equations for CR-SOAs are shown below, and they incorporate carrier recombination between CR and AR, as well as the ultrafast intraband effects of carrier heating (CH) and spectral hole burning (SHB) [9–13]:

$$\frac{\mathrm{d}h_{\mathrm{AR}}(t)}{\mathrm{d}t} = \frac{h_{\mathrm{CR}}(t) - h_{\mathrm{AR}}(t)}{\tau_{\mathrm{t}}(1+\eta)} + \frac{\eta h_0}{\tau_c(1+\eta)} - \frac{h_{\mathrm{AR}}(t)}{\tau_c} - (\exp[h_{\mathrm{AR}}(t) + h_{\mathrm{CH}}(t) + h_{\mathrm{SHB}}(t)] - 1) \times \frac{P_{\mathrm{in,\,CR\text{-}SOA}}(t)}{E_{\mathrm{sat}}}, \tag{1}$$

$$\frac{\mathrm{d}h_{\mathrm{CR}}(t)}{\mathrm{d}t} = -\frac{\eta(h_{\mathrm{CR}}(t) - h_{\mathrm{AR}}(t)}{\tau_t(1+\eta)} + \frac{h_0 - h_{\mathrm{CR}}(t)}{\tau_c(1+\eta)} - \frac{h_{\mathrm{CR}}(t)}{\tau_c}, \tag{2}$$

$$\frac{\mathrm{d}h_{\mathrm{CH}}(t)}{\mathrm{d}t} = -\frac{h_{\mathrm{CH}}(t)}{\tau_{\mathrm{CH}}} - \frac{\varepsilon_{\mathrm{CH}}}{\tau_{\mathrm{CH}}}(\exp[h_{\mathrm{AR}}(t) + h_{\mathrm{CH}}(t) + h_{\mathrm{SHB}}(t)] - 1) P_{\mathrm{in,CR\text{-}SOA}}(t), \tag{3}$$

$$\frac{\mathrm{d}h_{\mathrm{SHB}}(t)}{\mathrm{d}t} = -\frac{h_{\mathrm{SHB}}(t)}{\tau_{\mathrm{SHB}}} - \frac{\varepsilon_{\mathrm{SHB}}}{\tau_{\mathrm{SHB}}}(\exp[h_{\mathrm{AR}}(t) + h_{\mathrm{CH}}(t) + h_{\mathrm{SHB}}(t)] - 1) P_{\mathrm{in,CR\text{-}SOA}}(t) - \frac{\mathrm{d}h_{\mathrm{AR}}(t)}{\mathrm{d}t} - \frac{\mathrm{d}h_{\mathrm{CH}}(t)}{\mathrm{d}t}, \tag{4}$$

where the overall integrated gain of the CR-SOA due to carrier recombination between AR and CR, CH and SHB is represented by functions h_{AR}, h_{CR}, h_{CH} and h_{SHB}, respectively. $\eta = N_{\mathrm{AR}}/N_{\mathrm{CR}}$ [9] defines the population inversion factor (η), the unsaturated power gain (G_0) is incorporated through $G_0 = \exp[h_0] = \Gamma a N_{\mathrm{tr}}(I\tau_c/eVN_{\mathrm{tr}} - 1)$ [9] and $E_{\mathrm{sat}} = P_{\mathrm{sat}}\tau_{\mathrm{c}} = wd\hbar\omega_0/a\Gamma$ [9] is the saturation energy (E_{sat}). Table 1 shows the definitions of all default parameters [2–8,10–13]. Adams' numerical approach is used to run the time-dependent equations using Wolfram Mathematica® software.

The input A, B and Clk signals are considered to carry Gaussian-shaped RZ pulses of energy E_0, pulse width τ_{FWHM} (FWHM: full-width at half-maximum) and bit period T, which is the operating data rate's inverse [10–12]:

$$P_{A,\,B,\,Clk}(t) \equiv P_{\mathrm{in,CR\text{-}SOA}}(t) = \sum_{n=1}^{N} a_{n(A,\,B,\,Clk)} \frac{2\sqrt{\ln[2]}E_0}{\sqrt{\pi}\,\tau_{\mathrm{FWHM}}} \times \exp\left[-\frac{4\ln[2](t-nT)^2}{\tau_{\mathrm{FWHM}}^2}\right], \tag{5}$$

Table 1. Simulation default parameters values [2–8,10–13].

Symbol	Definition	Value	Unit
E_0	Pulse energy	0.7	pJ
τ_{FWHM}	Pulse width	1	ps
T	Bit period	8.33	ps
N	PRBS length	127	–
λ_A	Wavelength of signal A	1545	nm
λ_B	Wavelength of signal B	1550	nm
λ_{CW}	Wavelength of CW light	1560	nm
I	Injection bias current	200	mA
P_{sat}	Material saturation power	30	mW
τ_c	Carrier lifetime	200	ps
τ_{t}	Transition lifetime from CR to AR	5	ps
η	Population inversion factor	0.3	–
α	α-factor	5	–
α_{CH}	Linewidth enhancement factor for CH	1	–
α_{SHB}	Linewidth enhancement factor for SHB	0	–
$\varepsilon_{\mathrm{CH}}$	Nonlinear gain suppression factor for CH	0.2	W^{-1}
$\varepsilon_{\mathrm{SHB}}$	Nonlinear gain suppression factor for SHB	0.2	W^{-1}
τ_{CH}	Temperature relaxation rate	0.3	ps
τ_{SHB}	Carrier–carrier scattering rate	0.1	ps
Γ	Confinement factor	0.3	–
a	Differential gain	10^{-20}	m^2
N_{tr}	Transparency carrier density	10^{24}	m^{-3}
L	Length of AR	500	μm
d	Thickness of AR	0.3	μm
w	Width of AR	3	μm
G_0	Unsaturated power gain	30	dB
ω_0	Central optical frequency	193.55	THz
N_{SP}	Spontaneous emission factor	2	–
B_0	Optical bandwidth	2	nm

where $\alpha_{n(A,B,Clk)}$ denotes the nth pulse along either $N = 2^7-1$ bit-long pseudorandom binary sequence (PRBS) data A, B, i.e. $\alpha_{n(A,B)} = 0$, 1, or a Clk stream, i.e. $\alpha_{n(Clk)} = 1$.

To model the logic SUM function, the input powers to CR-SOA1 and CR-SOA2 are formulated as follows [10]:

$$P_{\text{in,CR-SOA}_1}(t) = P_{\text{A}}(t) + 0.5P_{\text{CW}} \tag{6}$$

$$P_{\text{in,CR-SOA}_2}(t) = P_{\text{B}}(t) + 0.5P_{\text{CW}}. \tag{7}$$

The coefficient 0.5 signifies that CW light is divided by a 3 dB OC as it enters the CR-SOAs-MZI1 middle arm. The following interferometric equation gives the output power of the logic SUM function [10]:

$$P_{\text{SUM}}(t) = 0.25P_{\text{CW}}\left(\begin{matrix} G_{\text{CR-SOA}_1}(t) + G_{\text{CR-SOA}_2}(t) - 2\sqrt{G_{\text{CR-SOA}_1}(t)G_{\text{CR-SOA}_2}(t)} \\ \cos[\Phi_{\text{CR-SOA}_1}(t) - \Phi_{\text{CR-SOA}_2}(t)] \end{matrix}\right), \tag{8}$$

where the overall gains and phase shifts inside CR-SOA1 and CR-SOA2 are represented by $G_{\text{CR-SOA1,2}}(t)$ and $\Phi_{\text{CR-SOA1,2}}(t)$, respectively.

To model the logic CARRY function, the input powers going into CR-SOA5 and CR-SOA6, respectively, are expressed as [12]:

$$P_{\text{CR-SOA}_5}(t) = 0.5P_{\text{XNOR}}(t) \tag{9}$$

$$P_{\text{CR-SOA}_6}(t) = P_{Clk}(t) + 0.5P_{\text{XNOR}}(t), \tag{10}$$

where $P_{\text{XNOR}}(t)$ is the output power of the XNOR operation, which is given by [12]

$$P_{\text{XNOR}}(t) = 0.25P_{\text{CW}}\left(\begin{matrix} G_{\text{CR-SOA}_3}(t) + G_{\text{CR-SOA}_4}(t) - 2\sqrt{G_{\text{CR-SOA}_3}(t)G_{\text{CR-SOA}_4}(t)} \\ \cos[\Phi_{\text{CR-SOA}_3}(t) - \Phi_{\text{CR-SOA}_4}(t)] \end{matrix}\right). \tag{11}$$

Then, the output power of logic CARRY is given by [11]

$$P_{\text{CARRY}}(t) = 0.25P_{\text{XNOR}}(t)\left(\begin{matrix} G_{\text{CR-SOA}_5}(t) + G_{\text{CR-SOA}_6}(t) - 2\sqrt{G_{\text{CR-SOA}_5}(t)G_{\text{CR-SOA}_6}(t)} \\ \cos[\Phi_{\text{CR-SOA}_5}(t) - \Phi_{\text{CR-SOA}_6}(t)] \end{matrix}\right). \tag{12}$$

The overall gain of each ith CR-SOA is then calculated as follows [10–12]:

$$G_{\text{CR-SOA}_i}(t) = \exp[h_{\text{AR}}(t) + h_{\text{CH}}(t) + h_{\text{SHB}}(t)], \quad i = 1, 2, 3, 4. \tag{13}$$

The phase change induced in each ith CR-SOA is given by [10–12]

$$\Phi_{\text{CR-SOA}_i}(t) = -0.5(\alpha h_{\text{AR}}(t) + \alpha_{\text{CH}} h_{\text{CH}}(t)), \quad i = 1, 2, 3, 4, \tag{14}$$

where the SHB contribution to the above total phase is zero, i.e. $\alpha_{\text{SHB}} \sim 0$ [10–12], the normal linewidth enhancement factor is α and the linewidth enhancement factor associated with CH is α_{CH}.

3. Results

The Q-factor [10–12] is used in this study as the metric to assess the performance of the AO half adder. The Q-factor must be larger than 6 for acceptable performance so that the accompanying bit error rate is smaller than 10^{-9} [9–12]. Figures 2 and 3 show the pulse patterns and the corresponding eye diagrams for the logic SUM and logic CARRY functions employing CR-SOAs-based MZIs at 120 Gb/s. The Q-factor values attained for the logic SUM and CARRY functions are 24.5 and 19.6, respectively, and hence both are high and more than the acceptable value. Furthermore, the desired functions are performed in a logically valid and high-quality manner. This is checked by direct comparison to the corresponding truth tables in the first case and the uniform pulses profile and clear and open eye diagrams in the second case.

The CR-SOA's operation depends on the transition time from CR to AR (τ_t) and on the injection bias current (I). Therefore, it is essential to investigate how these parameters affect the half adder's performance. Figure 4 shows the influence of τ_t and I on the Q-factor of the SUM and CARRY functions using CR-SOAs-MZIs at 120 Gb/s. As illustrated in figure 4a, a shorter τ_t enables the CR-SOAs dynamics to recover faster and, as a result, to obtain a larger Q-factor. On the other hand, I is critical in the amplification and switching processes. At high I, more carriers are injected into the CR [9] due to the mobility of the quasi-Fermi level up over the CR edge band, thus allowing for faster recovery and refilling

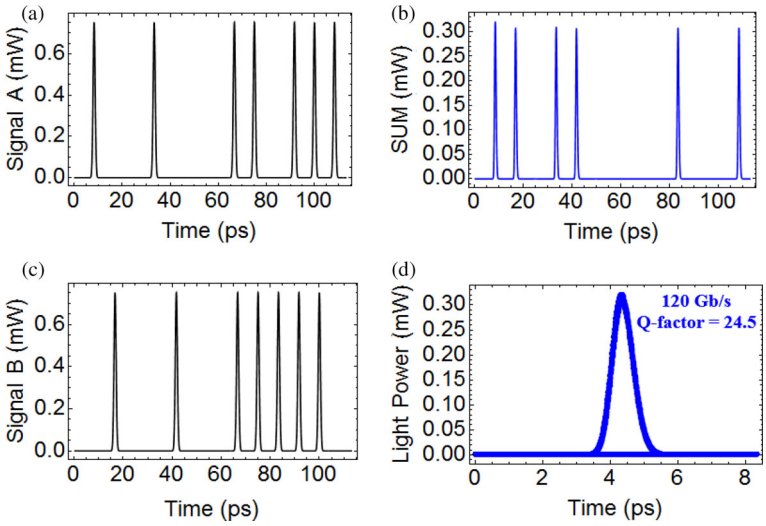

Figure 2. Logic SUM function numerical results using CR-SOAs at 120 Gb/s. (**a**) Data signal *A*, (**b**) data signal *B*, (**c**) logic output and (**d**) eye diagram.

of the AR layer after a strong input pulse has depleted it. As a result, the *Q*-factor increases, as depicted in figure 4b.

ASE noise is present in CR-SOAs, and so it is expected to affect the performance. Thus, the impact of ASE on logic SUM and CARRY functions utilising CR-SOAs-MZIs at 120 Gb/s is investigated, as shown in figure 5a. $P_{\mathrm{ASE}} = N_{\mathrm{SP}}(G_0 - 1)2hB_0$ [9] is used to calculate and add the ASE power to the output powers described by eqs (8) and (12). Although the *Q*-factor is decreased as the ASE power is augmented, the CR-SOAs allow acceptable performance even for higher ASE levels. This occurs because the CR-SOAs' inherently fast gain dynamics prevent ASE from having an irreversible effect on the AO half adder's performance.

On the other hand, it is helpful to know up to what speed the half adder can operate while maintaining acceptable performance. Figure 5b shows that this is possible up to 240 Gb/s, where the *Q*-factor remains over 6. Higher speeds, such as 320 Gb/s, would be feasible, provided the CR-SOAs were biased with higher I (~ 400 mA) and driven by lower energy data pulses (~ 0.3 pJ). These requirements are satisfied by authentic current sources and optical sources in combination

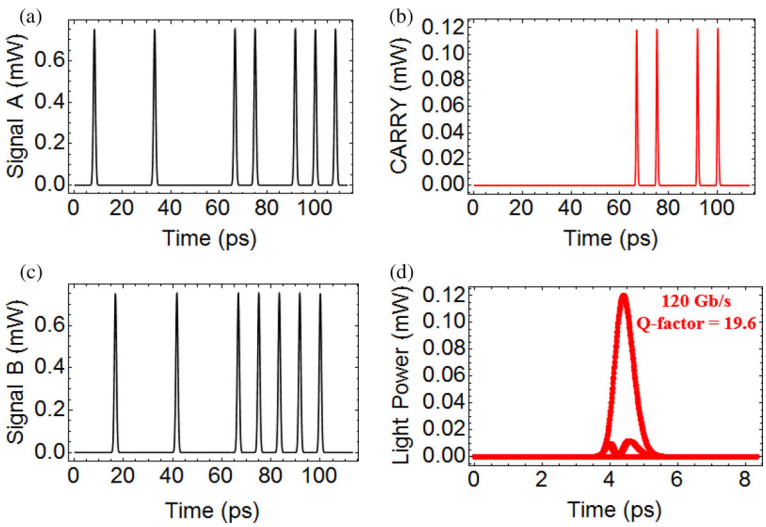

Figure 3. Logic CARRY function numerical results using CR-SOAs at 120 Gb/s. (**a**) Data signal *A*, (**b**) data signal *B*, (**c**) logic output and (**d**) eye diagram.

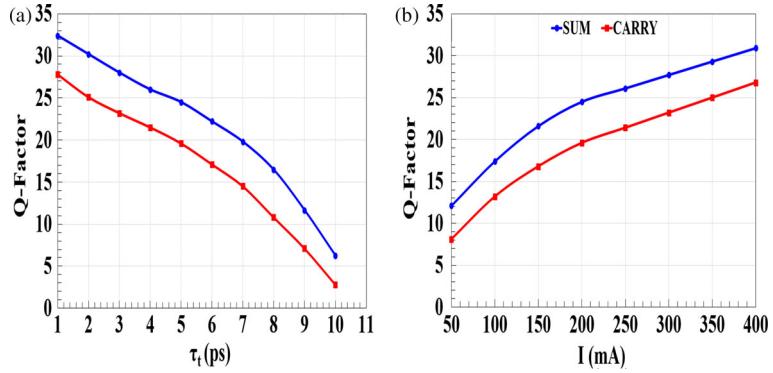

Figure 4. Q-factor of logic SUM and logic CARRY functions employing CR-SOAs-MZIs at 120 Gb/s vs. (**a**) transition time from CR to AR (τ_t) and (**b**) injection bias current (I).

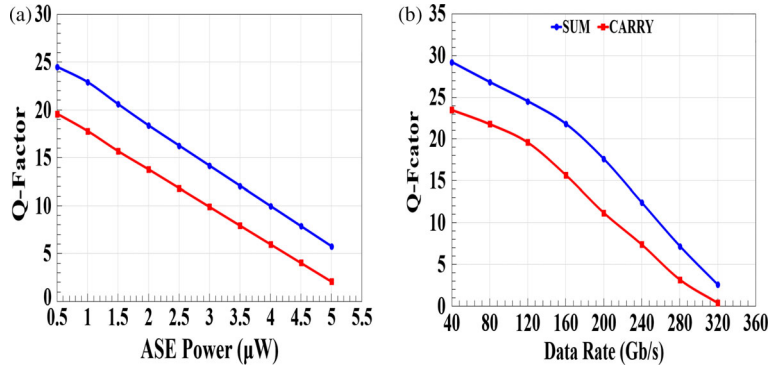

Figure 5. Q-factor of logic SUM and logic CARRY functions using CR-SOAs-MZIs at 120 Gb/s vs. (**a**) ASE power and (**b**) operating data rate.

with optical amplifiers. These findings demonstrate the CR-SOA's ability to realise the AO half adder despite the high ASE levels and data rates with acceptable performance.

4. Conclusion

In conclusion, we modelled and studied an AO half adder of 120 Gb/s RZ data employing properly configured and connected CR-SOAs-assisted MZIs. The Q-factor was used to evaluate the outcome of logic SUM and logic CARRY functions realised via XOR and AND logic gates, respectively, and subsequently the performance of the whole scheme. In the presence of ASE noise, the change of this metric vs. several important operating parameters was examined and assessed. The simulation findings suggest that using CR-SOAs, it is possible to achieve Q-factors well above their permissible limit for SUM and CARRY functions, which are executed with high quality. The AO half adder can be designed to exhibit high performance at ultrahigh speeds.

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