nature nanotechnology

ARTICLES

https://doi.org/10.1038/s41565-021-00966-5

Check for updates

Three-dimensional monolithic micro-LED display driven by atomically thin transistor matrix

Wanqing Meng[1,13], Feifan Xu[1,2,13], Zhihao Yu[1,3,13], Tao Tao[1,2,13], Liangwei Shao[1], Lei Liu[1], Taotao Li[1,4], Kaichuan Wen[5], Jianpu Wang[5], Longbing He[6], Litao Sun[6], Weisheng Li[1], Hongkai Ning[1], Ningxuan Dai[1], Feng Qin[1,7], Xuecou Tu[1,8], Danfeng Pan[1,8], Shuzhuan He[9], Dabing Li[10], Youdou Zheng[1,2], Yanqing Lu[4], Bin Liu[1,2] ✉, Rong Zhang[1,2,11,12] ✉, Yi Shi[1,2] ✉ and Xinran Wang[1,2] ✉

Two-dimensional materials are promising candidates for future electronics due to unmatched device performance at atomic limit and low-temperature heterogeneous integration. To adopt these emerging materials in computing and optoelectronic systems, back end of line (BEOL) integration with mainstream technologies is needed. Here, we show the integration of large-area MoS_2 thin-film transistors (TFTs) with nitride micro light-emitting diodes (LEDs) through a BEOL process and demonstrate high-resolution displays. The MoS_2 transistors exhibit median mobility of 54 $cm^2 V^{-1}s^{-1}$, 210 $\mu A \mu m^{-1}$ drive current and excellent uniformity. The TFTs can drive micrometre-sized LEDs to 7.1×10^7 $cd m^{-2}$ luminance under low voltage. Comprehensive analysis on driving capability, response time, power consumption and modulation scheme indicates that MoS_2 TFTs are suitable for a range of display applications up to the high resolution and brightness limit. We further demonstrate prototypical 32×32 active-matrix displays at 1,270 pixels-per-inch resolution. Moreover, our process is fully monolithic, low-temperature, scalable and compatible with microelectronic processing.

Since its debut in the early 1990s, the nitride semiconductor light-emitting diode (LED) has revolutionized solid-state lighting, and today has grown into a multi-billion-dollar industry[1–3]. In recent years, developments in miniaturized LED devices, the so-called micro-LED[4], have enabled many new applications such as the high-resolution self-emissive display for augmented and virtual reality (AR/VR), visible-light communication[5] and biomedical probes[6–12]. They can deliver extreme brightness $>10^7$ $cd m^{-2}$, a nanosecond response time, high efficiency ~60% and a wide operating temperature window, making micro-LEDs the ultimate display technology. To meet the future demands for the human–machine interface, individual pixels need to be of micrometre size and have unapparelled brightness. This requires monolithic three-dimensional (3D) integration of the high-performance thin-film transistor (TFT) backplane, beyond the driving capability of existing TFT technologies based on amorphous silicon and indium gallium zinc oxide (IGZO)[13,14].

To this end, two-dimensional (2D) semiconductors such as transition-metal dichalcogenides (TMDs) possess several remarkable features as a heterogeneous component[15–18]. First, being crystalline materials, they exhibit mobility greater than 100 $cm^2 V^{-1}s^{-1}$ (refs. [18,19]), which is much higher than that of amorphous TFT materials. Therefore, they can drive micro-LEDs at low voltage and reduce the power consumption of the backplane. The atomically thin channel also guarantees low leakage current at stand-by[20]. Second, many TMDs can be synthesized on a wafer scale by chemical vapour deposition (CVD)[21–24]. Currently, 4-inch MoS_2 films are batch-produced in laboratories[22], and there is no scientific barrier to going to a larger size. However, the technologically relevant CVD films generally have lower mobility than exfoliated flakes due to inferior material quality and surface contamination during the transfer and etching processes (Supplementary Table 1). Third, being van der Waals materials, they can be transferred to arbitrary substrates under room-temperature and non-vacuum conditions. This facilitates back end of line (BEOL) integration with mainstream semiconductor technologies[25–29]. Fourth, being atomically thin, they offer excellent flexibility and optical transparency[27,28]. These unique properties offer new opportunities to use TMDs in advanced display applications.

In this work, we report the monolithic 3D integration of large-area MoS_2 TFTs with GaN-based micro-LEDs and high-resolution displays. We develop a low-temperature, ultraclean BEOL process that eliminates the exposure of MoS_2 to any polymers, organic solvents and ion damage. This leads to improved transistor performance and uniformity compared to conventional fabrication processes. The MoS_2 transistors provide a large drive current of 210 $\mu A \mu m^{-1}$ and deliver 7×10^7 $cd m^{-2}$ luminance and a delay time of several hundred nanoseconds in micro-LEDs under 8 V. These metrics meet the

[1]National Laboratory of Solid State Microstructures, School of Electronic Science and Engineering and Collaborative Innovation Center of Advanced Microstructures, Nanjing University, Nanjing, China. [2]Jiangsu Provincial Key Laboratory of Advanced Photonic and Electronic Materials, Nanjing, China. [3]College of Electronic and Optical Engineering, Nanjing University of Posts and Telecommunications, Nanjing, China. [4]College of Engineering and Applied Sciences, Nanjing University, Nanjing, China. [5]Key Laboratory of Flexible Electronics (KLOFE) and Institution of Advanced Materials (IAM), Jiangsu National Synergetic Innovation Center for Advanced Materials (SICAM), Nanjing Tech University (NanjingTech), Nanjing, China. [6]SEU-FEI Nano-Pico Center, Key Lab of MEMS of Ministry of Education, Southeast University, Nanjing, China. [7]Tianma Microelectronics Co., Ltd, Shanghai, China. [8]Microfabrication and Integration Technology Center, Nanjing University, Nanjing, China. [9]Nanjing PureSemi Semiconductor Co., Ltd, Nanjing, China. [10]State Key Laboratory of Luminescence and Applications, Changchun Institute of Optics, Fine Mechanics and Physics, Chinese Academy of Sciences, Changchun, China. [11]Collaborative Innovation Center for Optoelectronic Semiconductors and Efficient Devices, Department of Physics, Xiamen University, Xiamen, China. [12]Institute of Future Display Technology, Tan Kah Kee Innovation Laboratory, Xiamen, China. [13]These authors contributed equally: Wanqing Meng, Feifan Xu, Zhihao Yu, Tao Tao. ✉e-mail: bliu@nju.edu.cn; rzhangxmu@xmu.edu.cn; yshi@nju.edu.cn; xrwang@nju.edu.cn

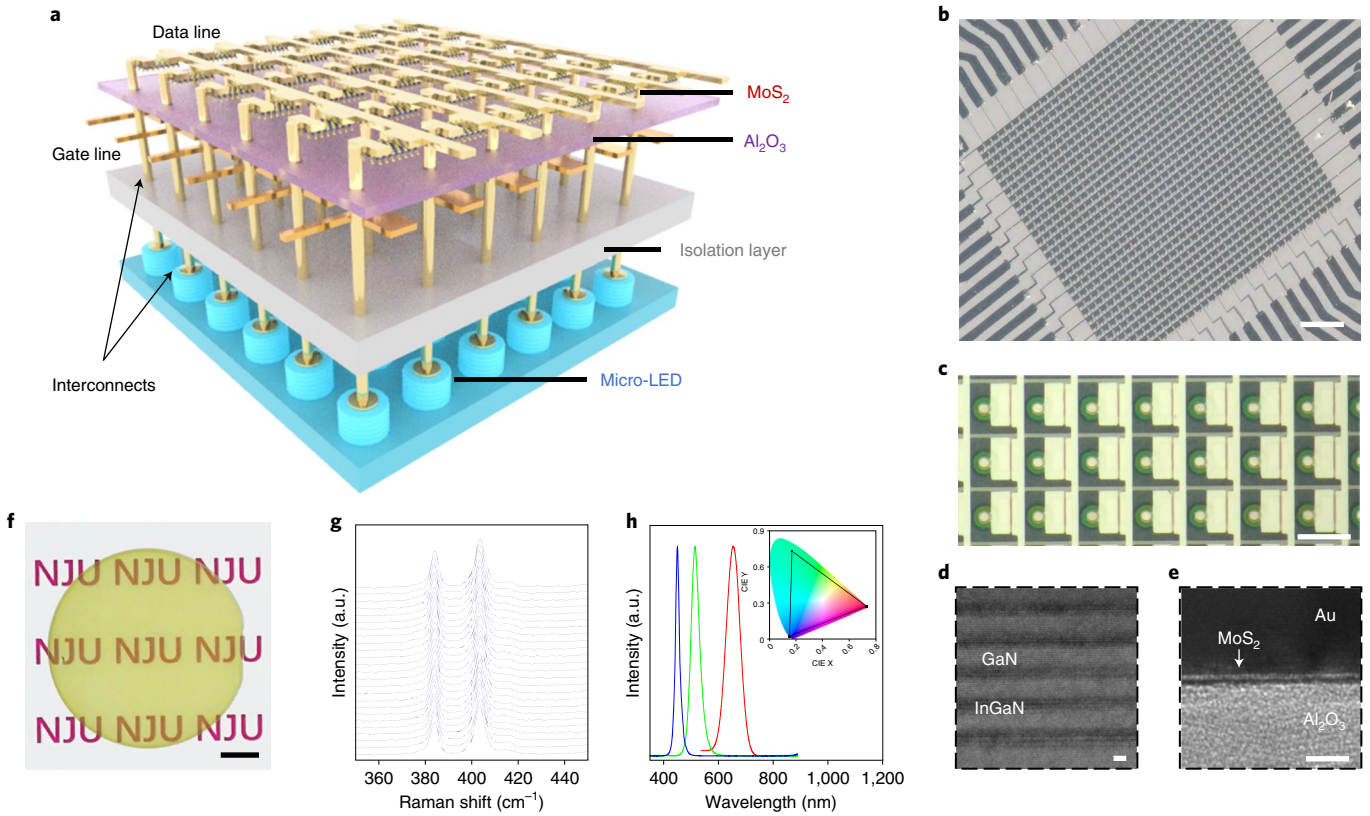

Fig. 1 | Monolithic integration of MoS_2 TFTs with micro-LEDs. a–**c**, Schematic illustration (**a**) and optical micrographs (**b**,**c**) of the AM micro-LED display. Scale bars, 100 μm and 20 μm for **b** and **c**, respectively. **d**,**e**, Cross-sectional TEM image of the InGaN/GaN multiple quantum well and the Au–MoS_2 contact interface, respectively. Scale bars, 4 nm. **f**, Wafer-scale MoS_2 single crystal grown on 2-inch sapphire by CVD. Scale bar, 1 cm. **g**, Raman line scans across the wafer diameter showing uniform monolayer MoS_2. **h**, The electroluminescence spectra and colour range of the RGB micro-LEDs. a.u., arbitrary units; CIE, International Commission on Illumination.

requirements of all the major display applications. Our process is fully monolithic, scalable and compatible with microelectronic processing. Finally, we fabricate 32 × 32 active-matrix (AM) displays at 1,270 pixels-per-inch (PPI) resolution, and demonstrate addressing of individual pixels and high-resolution QR code images.

Monolithic integration of MoS_2 TFTs with micro-LEDs

Figure 1a,b illustrates the schematics and optical micrograph of the AM micro-LED display. The stack consisted of three layers. The bottom layer was the standard GaN-based LED grown by metal-organic CVD on sapphire substrate. The circular mesa was fabricated by photolithography and dry etching. For blue and green LEDs, the emission colour was designed by controlling the indium composition in a InGaN/GaN multiple quantum well (Fig. 1d). The red colour emission was realized by depositing colour-converting CdSe/CdTe quantum dots on a blue LED[30]. This colour-converting approach is a more convenient method to realize full-colour displays by avoiding the problems of low external quantum efficiency (EQE) of the red LED and mass transfer[7]. The electroluminescence spectra of RGB LEDs were centred at 460 nm, 520 nm and 635 nm, respectively, covering 127% National Television Standards Committee (NTSC) and 95% Broadcasting Television (BT) 2020 (Fig. 1h). After photolithographic patterning into circular pixels (typically with one-to-one filling ratio) and deposition of the top contact on the p-GaN, a layer of spin-on-glass (SOG, ~1.3 μm thick) was added as a coating, which acted as both planarization and electrical isolation layer. The MoS_2 TFT matrix was monolithically fabricated on the SOG and connected to the underlying micro-LEDs through vertical vias. To minimize the blocking of the top emission, we designed the TFT and electrical wirings on the side of each LED pixel (Fig. 1c). The detailed fabrication processes are described in Methods and Supplementary Fig. 1.

To drive micro-LED displays, the MoS_2 transistors need to simultaneously have high performance and uniformity. To this end, we used high-quality MoS_2 single-crystalline films grown on a 2-inch sapphire wafer by CVD[31] (Fig. 1f and Supplementary Fig. 2). Figure 1g shows Raman scans across the wafer diameter. The $19.67 \pm 0.47\ cm^{-1}$ (the error represents s.d.) separation between the Raman E^1_{2g} and A_{1g} modes showed that the MoS_2 was a monolayer with good wafer-scale uniformity. The photoluminescence (PL) of MoS_2 exhibited a prominent A-exciton emission at 1.865 eV across a 2-inch wafer, further confirming the monolayer nature (Supplementary Fig. 3a). Furthermore, we performed high-resolution PL mapping experiments across a $100 \times 100\ \mu m^2$ area. The PL mapping results on the intensity, peak position and full-width at half-maximum (FWHM) show the high uniformity of the monolayer MoS_2 film (Supplementary Fig. 3b-d). Statistical analysis of the PL spectra shows that the average peak position is 1.865 eV with a s.d. of 1 meV, and the average FWHM is 72 meV with a s.d. of 0.7 meV (Supplementary Fig. 3e,f).

The performance of 2D transistors highly depends on contact and dielectric interfaces. Conventional polymer-based transfer, lithography and metal deposition inevitably introduce contamination and defects, which degrade the mobility and uniformity[32,33]. The situation is even worse for large-area CVD films due to the extra transfer step. To minimize extrinsic contamination, we developed an ultraclean and scalable fabrication process as illustrated in Fig. 2a (see Methods for details). Briefly, we used a poly(methyl methacrylate)/

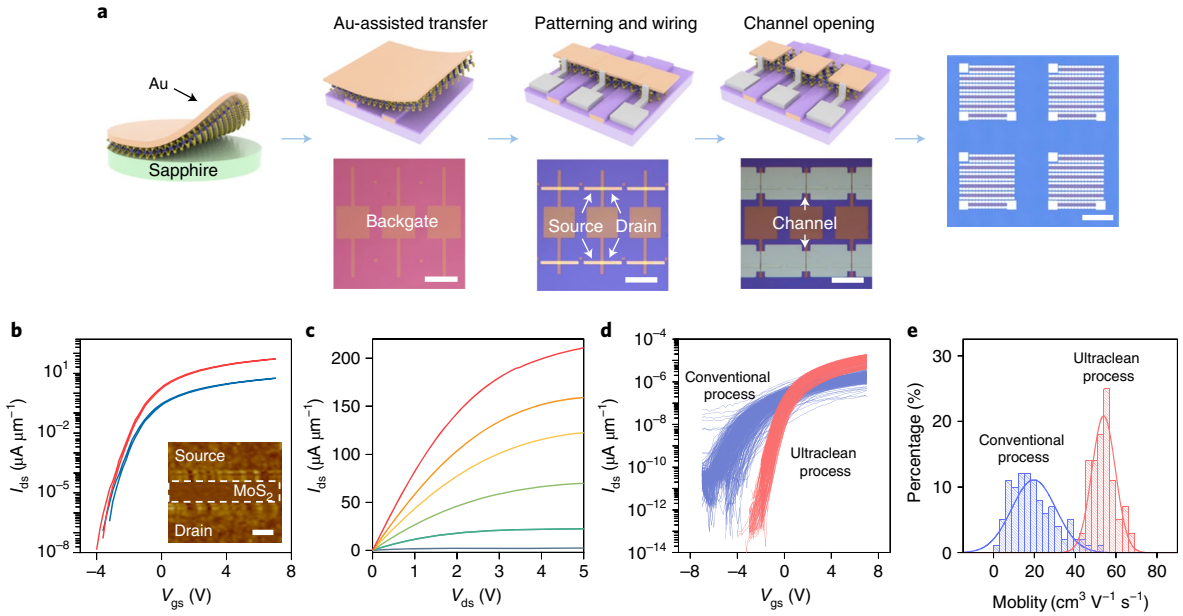

Fig. 2 | MoS_2 transistor performance. a, Fabrication process of MoS_2 transistors and the corresponding optical micrographs at each step. Scale bars, 40 μm. An optical micrograph of the finished MoS_2 field-effect transistor (FET) arrays is shown on the right. Scale bar, 500 μm. **b**, Double-sweep transfer characteristics of a MoS_2 FET (L = 1 μm, W = 10 μm) under the double-sweep voltage V_{ds} equal to 0.1 V (blue line) and 1 V (red line). Inset: atomic force microscopy image of the device. Scale bar, 1 μm. **c**, Output characteristics of the device in **b**. From top to bottom, V_{gs} equals 12 V to 0 V with 2 V steps. **d**, Comparison of 400 MoS_2 FET transfer characteristics (L = 1 μm, W = 10 μm, V_{ds} = 1 V) fabricated by our ultraclean process (red, 200 devices) and conventional polymer-based transfer and lithography process (blue, 200 devices). **e**, Mobility distribution of MoS_2 FETs. The solid lines are Gaussian fittings. The data are derived from long-channel devices (L = 50 μm) to minimize the effect of contact resistance.

polydimethylsiloxane (PMMA/PDMS) stamp to pick up Au film predeposited on a silicon wafer and laminated on the fresh as-grown MoS_2. After mild heating at 90 °C, the MoS_2 was dry-delaminated (without solvent) and transferred onto the micro-LED chip with prepatterned local backgate and 20-nm Al_2O_3 gate dielectrics. The dry delamination from sapphire indicated strong intrinsic bonding between Au and MoS_2, consistent with theoretical calculations[34]. The Au film was kept on the MoS_2 until the final step and it acted as protection layer from ambient absorption, dry etching mask and electrical contacts. Next, the unnecessary Au/MoS_2 was lithographically patterned and etched. It should be noted that, during this step, the channel and contact regions were still protected by the Au films (Fig. 2a, middle panel). Then, we etched the via holes and deposited metal interconnects onto the micro-LED. In the final step, a gap was opened on the Au film using water-based KI solution to define the MoS_2 channel. During the entire process, the MoS_2 was only briefly exposed to ambient before the Au lamination, and was not exposed to any polymer or organic solvent. Therefore, both the MoS_2 channel (Fig. 2b inset) and Au–MoS_2 contact interface (Fig. 1e) were extremely clean. We note that Au is a deep-level dopant and is incompatible with a complementary metal oxide semiconductor (CMOS) front end of line (FEOL) process. However, this issue is not a major concern in a low-temperature back end of line (BEOL) process as the dopant diffusion in semiconductors has an exponential dependence on temperature[35]. To further resolve the diffusion of Au and the potential combability issues with commercial foundries, we propose the use of a Cu/Au bi-layer, where Cu serves as the passivation layer to reduce the diffusion of Au (Supplementary Fig. 4).

MoS_2 transistor performance

Next, we evaluated the MoS_2 transistor performance. Figure 2b,c present transfer and output characteristics of a typical device with 1 μm channel length (L) and 10 μm channel width (W). The transistor exhibits n-type behaviour with a threshold voltage (V_{th}) of 0.2 V, a subthreshold slope (SS) of 200 mV dec^{-1} and on/off ratio greater than 10^9, and hysteresis-free transfer characteristics. The on-state current (I_{on}) reaches 2.1 mA (or 210 μA μm^{-1}), which exceeds the typical operation current in micro-LEDs by several orders of magnitude[36]. Consequently, the MoS_2 transistor could drive micro-LEDs at very low voltage as shown below. We note that relatively high gate voltage (V_{gs}) up to 12 V was needed to fully turn on the devices. However, both V_{gs} and SS can be readily reduced by using thinner or higherdielectric constant (κ) gate dielectrics (such as HfO_2). For example, using 15 nm HfO_2 as gate dielectrics, we achieved SS ~ 104 mV dec^{-1} and reduced gate drive voltage by about 2 V (Supplementary Fig. 5). Here, we used depletion mode transistors to achieve high drive current and demonstrated the potential of MoS_2 TFT, which leads to increased static power consumption at V_{gs} = 0 V. For low-power display applications (such as smart phone, watches and AR), we can engineer the V_{th} and static power consumption by using higher work-function gate metal and surface passivation, as detailed in Supplementary Figs. 6 and 7. For example, using Pt as the gate metal, the static leakage current was reduced by five orders of magnitude to 0.1 pA μm^{-1}, which was superior to commercial TFT technologies (Supplementary Table 2). We believe that by combining an appropriate gate metal and surface modification scheme, the V_{th} can be engineered on-demand to realize the balance between performance and static power consumption.

Micro-LED displays require millions of pixels being individually addressed, so the device variation is an important consideration. To this end, we measured a large number of devices. We also fabricated control devices using conventional processes, which exposed the surface of MoS_2 to PMMA and organic solvent repeatedly during transfer, etching and source/drain deposition (see Methods for details). Figure 2d plots the transfer curves of 200 devices in each group. After optimization, the device yield in a single batch could reach 95%, suggesting that our process is highly robust and potentially scalable for production using automated tools[15]. More

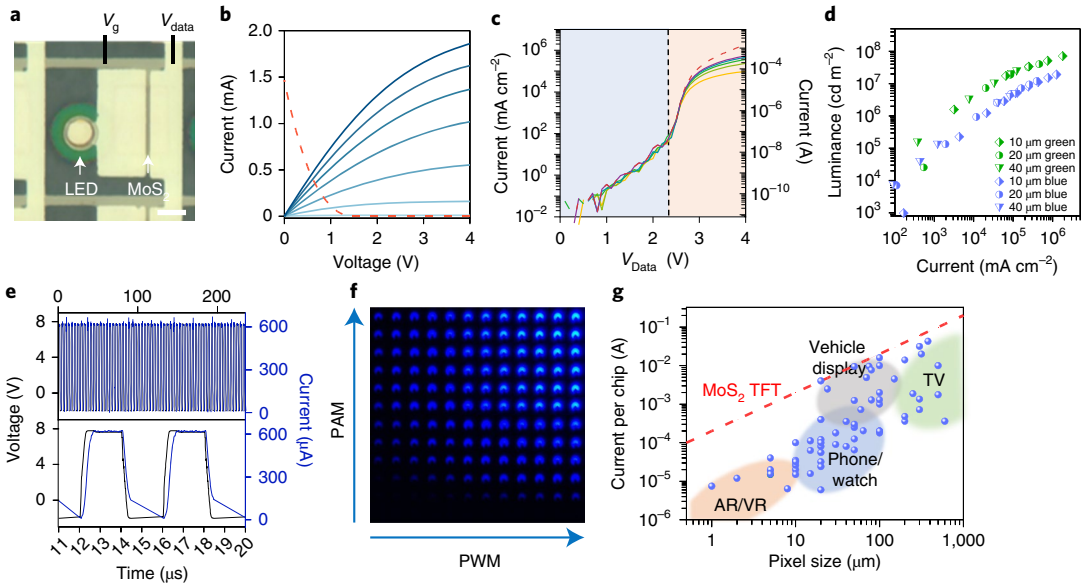

Fig. 3 | Driving individual micro-LEDs by MoS_2 TFTs. a, Optical micrograph of the 1T1D pixel. Scale bar, 5 μm. **b**, Gate-tunable operation points of the 1T1D, which is the intersection of the *I*–*V* characteristics of the MoS_2 FET (blue solid lines) and micro-LED (red dashed line). Here, both the transistor width and micro-LED diameter are 10 μm. **c**, *I*–*V* characteristics of the 1T1D under different V_{gs} (solid lines) and micro-LED only (red dashed line). **d**, The luminance of 10–40 μm blue and green micro-LEDs measured on the 1T1D structure. Both current and luminance are normalized by the area of the micro-LEDs. **e**, The stable operation of the 1T1D under 250-kHz voltage pulses. **f**, LED brightness modulated by PAM (V_{gs} from 0 V to 10 V) and PWM (V_{gs} from 500 kHz to 22 kHz) schemes in 1T1D, achieving a 12 × 12 level of continuous brightness tuning. **g**, Operating current as a function of pixel size for a wide range of LED dimensions (collected from the literature). Our MoS_2 TFT (dashed line) provides sufficient drive current for various display applications.

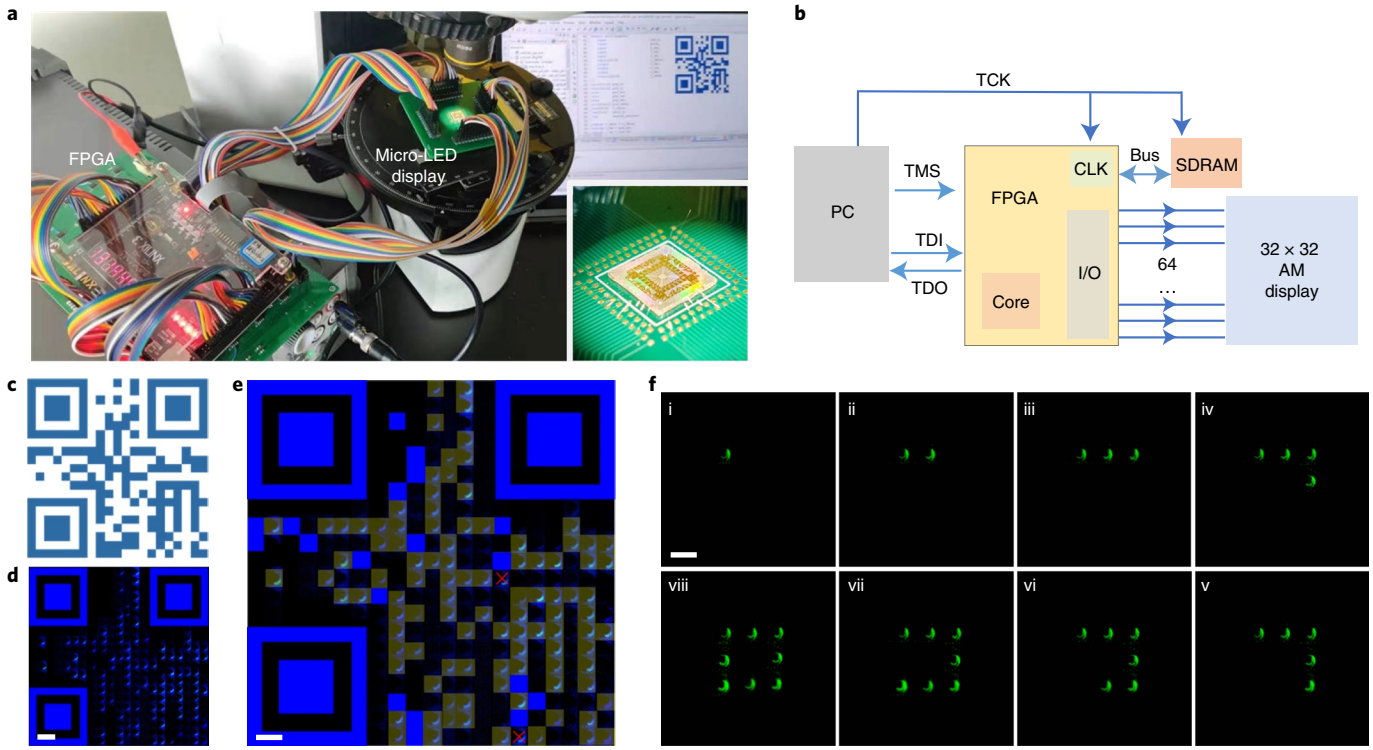

Fig. 4 | High-resolution AM micro-LED displays. a, Experimental setup for the AM displays. Inset: a wire-bonded chip mounted under optical microscope. **b**, Block diagram of the external circuitry. CLK, Clock; I/O, input/output; SDRAM, synchronous dynamic random-access memory; TCK, test clock; TMS, test mode select; TDI, test data in; TDO, test data out. **c**, QR code design corresponding to the phrase 'MoS2 LED NJU'. **d**,**e**, Microscopic images of the QR code displayed on a 1,270-PPI blue micro-LED display. In **e**, grey blocks indicate pixels that function properly, blue blocks indicate open pixels and red crosses indicate short pixels. **f**, Sequential frames of a green micro-LED display showing a square pattern. Scale bar, 20 μm.

importantly, the ultraclean process brought a significant boost in performance and uniformity. Compared to control devices, the median of on-state current and SS was improved by more than 475% (from 2 to 11.5 $\mu A\,\mu m^{-1}$) and 60% (from 775 to 310 $mV\,dec^{-1}$), respectively (Fig. 2d and Supplementary Fig. 8). Figure 2e depicts the statistical distribution of mobility. Our devices showed a median mobility of 54 $cm^2V^{-1}s^{-1}$ with FWHM (extracted from Gaussian fitting) of 6.6 $cm^2V^{-1}s^{-1}$. On the other hand, the control group showed much lower median mobility (17.9 $cm^2V^{-1}s^{-1}$) and greater variation (14.2 $cm^2V^{-1}s^{-1}$ FWHM). A similar trend was observed for SS and V_{th} (Supplementary Fig. 8).

We carried out further benchmarking with the literature on CVD MoS_2 devices reporting statistical results (Supplementary Fig. 9 and Table 1)[23,26,36–42]. Overall our devices exhibit good performance and variation (mobility, SS and V_{th}). The improvement suggests that our process indeed reduces the density of interface scattering centres, trap states and unintentional doping by protecting the MoS_2 from external contamination. These results also highlight the necessity for developing unconventional fabrication processes for surface-dominated 2D materials before they can achieve the level of performance and variation required by the industry[15].

Driving individual micro-LED

After monolithic integration of MoS_2 TFTs, we drive individual micro-LED pixels using a one-transistor-one-diode (1T1D) scheme (Fig. 3a, where V_g denotes the gate voltage of the MoS_2 TFT and V_{data} denotes the bias voltage of the 1T1D). The micro-LEDs show standard diode behaviour under forward bias with an ideality factor of $n = 1.45$ (Supplementary Text 1 and Supplementary Fig. 10). Figure 3b shows the gate-tunable operation points of the 1T1D (the interception points of the LED and TFT). At the on state of the TFT, the voltage drop on the transistor was only 0.57 V, corresponding to 14.3% of the total power consumption. Figure 3c shows the current–voltage (I–V) characteristics of the 1T1D. Below the LED turn-on voltage of 2.3 V, the current was limited by the LED. Above the turn-on voltage (light-emitting regime), the current through the LED was modulated by V_g. Using a 10-μm-wide MoS_2 TFT, we successfully lit 10–40-μm blue and green micro-LEDs. Under $V_{dd} = V_{data} = V_g = 8$ V (where V_{dd} denotes the total power supply of the circuit), the MoS_2 TFT was able to supply a drive current of more than 1.4 mA in all cases (Supplementary Fig. 11), corresponding to a current density of ~1.1–17.8 × 10^5 $mA\,cm^{-2}$ in these micro-LEDs. Under such conditions, the blue and green micro-LEDs showed extremely bright luminance of 1.9 × 10^7 and 7.1 × 10^7 $cd\,m^{-2}$, respectively (Fig. 3d). The high brightness of the 1T1D can support numerous types of display applications including AR/VR glasses, vehicle display under daylight and even visible-light communication. We note that the current per pixel in typical micro-LED displays is only in the microampere range[16,40], corresponding to $V_{data} < 3$ V in our 1T1D owing to the excellent driving capability of MoS_2 (Fig. 3c).

A GaN-based micro-LED has an intrinsically short response time on the nanosecond scale[36]. However, the parasitic resistance–capacitance from the TFT matrix may cause significant delays. We measured the response time of the 1T1D by applying a synchronized pulse of V_{data} and V_g. Figure 3e shows stable operation of the 1T1D under 250-kHz voltage pulses. The voltage rising and falling time (10–90%) was 330 ns, which was limited by the equipment. The current followed similar time constants but with a total resistance–capacitance delay of 410 ns (240 ns on the rising edge and 170 ns on the falling edge). This indicates that individual pixels can potentially operate at 2.4 MHz, which is four orders of magnitude faster than the refresh rate of the most advanced displays (~100 Hz). In addition, the current spikes in the transient response of micro-LEDs were reduced by the MoS_2 TFT (Supplementary Fig. 12), which could further increase stability and lifetime. The 1T1D structure showed excellent operating stability, with little degradation of current and brightness under continuous bias stress for 3 hours (Supplementary Fig. 13).

The brightness of the 1T1D was modulated by two schemes, namely pulse amplitude modulation (PAM) and pulse width modulation (PWM). The former is widely used in organic light-emitting diode, while the latter is suitable for micro-LEDs because they exhibit current-dependent efficiency and spectral shift. Figure 3f shows the LED brightness simultaneously modulated by both schemes in the 1T1D. Each row and column correspond to a constant V_g amplitude and pulse width, respectively. We can see that both PAM and PWM reliably achieved 12-level tuning of brightness. The large on/off ratio (10^9) and bandwidth (2.4 MHz) of MoS_2 transistors allow fine tuning of brightness to meet the requirement of high-dynamic-range displays.

Based on the 1T1D performance, we can evaluate MoS_2 TFT technology for various display applications. Figure 3g summarizes the operating current as a function of pixel size for a wide range of LED dimensions. The data points are broadly grouped into four categories (TV, vehicle display, phone/watch and AR/VR) according to the pixel size. The dashed line represents the driving capability of our MoS_2 TFT (210 $\mu A\,\mu m^{-1}$, assuming equal scaling of the transistor width with the micro-LED). We can see that MoS_2 provides sufficient drive current over the entire range. We also benchmark our MoS_2 TFTs with commercial high-performance TFT technologies, as summarized in Supplementary Table 2. Currently, IGZO is widely adopted in active-matrix organic light-emitting diode displays. However, a typical IGZO TFT has a mobility of ~10 $cm^2V^{-1}s^{-1}$, and the drive current is much lower than that for MoS_2 (ref. [43]). Low-temperature poly-Si (LTPS) is the most competitive commercial TFT technology in terms of mobility. However, LTPS requires high-temperature laser annealing and ion implantation[44], which is undesirable for a BEOL process. In addition, LTPS cannot achieve good flexibility and transparency, and it is therefore not compatible with wearable devices such as AR glasses. Besides, both V_{dd} and V_{gs} of our MoS_2 TFT are lower than the values for LTPS and IGZO. Compared to these existing TFT technologies, MoS_2 not only offers advantages in driving capability, low-power consumption and low-temperature integration, but it also enables new forms of flexible and transparent displays.

High-resolution AM display

To prove that the heterogeneous integration can work at a system level, we fabricated fully monolithic AM displays. The displays had 1,024 (32 × 32) pixels with 20-μm pitch, corresponding to 1,270 PPI. Each pixel comprised a 10-μm micro-LED and a MoS_2 driving transistor. All pixels shared a global ground (n-GaN contact) with independently addressable data and gate lines, which were wire-bonded to the input/output interface of a field-programable gate array (FPGA) for AM addressing (Fig. 4a,b, see Methods for details). The image was displayed by high-speed progressive scanning: in each frame, 32 gate lines were scanned sequentially and recorded by a synchronous dynamic random-access memory. Our FPGA circuit was designed with a minimal refresh time of 1 μs, corresponding to 31,250 frames per second.

Furthermore, we demonstrate two examples of AM addressing using our micro-LED displays. Figure 4c is a quick response (QR) image of the phrase 'MoS2 LED NJU' designed according to the international QR code standard (ISO/IEC 18004:2015). Figure 4d shows the QR code on a blue micro-LED display. In the magnified image in Fig. 4e, grey blocks mark the pixels that function properly (103 pixels), blue blocks mark the open pixels that should have been lit (128 pixels) and red crosses mark the short pixels that should have been dark (2 pixels). Most device failures were due to incomplete etching of thick SOG via holes, which resulted in open pixels. By fixing the failed pixels in the image, we successfully scanned the QR code by smart phone (Supplementary Video 1). Figure 4f

shows another example of AM addressing using a green micro-LED display, where a square pattern was drawn in sequential frames by lighting up individual pixels. Although these demonstrations were still primitive, they nevertheless proved that MoS_2 TFTs could drive micro-LED displays under very high resolution and at system level.

Conclusions

In conclusion, we report fully 3D monolithic, 1,270-PPI AM micro-LED displays driven by atomically thin MoS_2 TFTs. The MoS_2 was BEOL integrated by a low-temperature ultraclean process and exhibited excellent electrical performance and uniformity. Comprehensive analysis on the driving capability, luminance, response time, power consumption and modulation scheme show that MoS_2 TFTs are suitable for a range of micro-LED display applications up to the highest resolution and brightness limit. Furthermore, we envision that new forms of transparent and wearable displays will be enabled by the atomically thin semiconductors for biomedical applications and human–machine interfaces. We believe that heterogeneous BEOL integration with mature semiconductor technology, such as demonstrated here, will rapidly advance 2D materials technology in the near future.

Online content

Any methods, additional references, Nature Research reporting summaries, source data, extended data, supplementary information, acknowledgements, peer review information; details of author contributions and competing interests; and statements of data and code availability are available at https://doi.org/10.1038/s41565-021-00966-5.

Received: 19 February 2021; Accepted: 23 July 2021;
Published online: 9 September 2021

References

1. Nakamura, S., Senoh, M. & Mukai, T. High-power InGaN/GaN double-heterostructure violet light emitting diodes. *Appl. Phys. Lett.* **62**, 2390–2392 (1993).
2. Li, G. et al. GaN-based light-emitting diodes on various substrates: a critical review. *Rep. Prog. Phys.* **79**, 056501 (2016).
3. *Global Packaged GaN LED Market Report* (Market Reports World, 2019); https://www.marketreportsworld.com/-global-packaged-gan-led-market-14194592
4. Jin, S. X., Li, J., Li, J. Z., Lin, J. Y. & Jiang, H. X. GaN microdisk light emitting diodes. *Appl. Phys. Lett.* **76**, 631–633 (2000).
5. Yuan, Y. F. et al. Potential key technologies for 6G mobile communications. *Sci. China Inf. Sci.* **63**, 183301 (2020).
6. Lin, J. Y. & Jiang, H. X. Development of microLED. *Appl. Phys. Lett.* **116**, 100502 (2020).
7. Wong, M. S., Nakamura, S. & DenBaars, S. P. Review—progress in high performance III-nitride micro-light-emitting diodes. *ECS J. Solid State Sci. Technol.* **9**, 015012 (2019).
8. Huang, Y., Hsiang, E.-L., Deng, M.-Y. & Wu, S.-T. Mini-LED, micro-LED and OLED displays: present status and future perspectives. *Light Sci. Appl.* **9**, 105 (2020).
9. Liu, Z., Chong, W. C., Wong, K. M. & Lau, K. M. GaN-based LED micro-displays for wearable applications. *Microelectron. Eng.* **148**, 98–103 (2015).
10. Park, S.-I. et al. Printed assemblies of inorganic light-emitting diodes for deformable and semitransparent displays. *Science* **325**, 977–981 (2009).
11. Liu, Z. J., Chong, W. C., Wong, K. M. & Lau, K. M. 360 PPI flip-chip mounted active matrix addressable light emitting diode on silicon (LEDoS) micro-displays. *J. Disp. Technol.* **9**, 678–682 (2013).
12. Cok, R. S. et al. Inorganic light-emitting diode displays using micro-transfer printing. *J. Soc. Inf. Disp.* **25**, 589–609 (2017).
13. Zhang, L., Ou, F., Chong, W. C., Chen, Y. & Li, Q. Wafer-scale monolithic hybrid integration of Si-based IC and III–V epi-layers—a mass manufacturable approach for active matrix micro-LED micro-displays. *J. Soc. Inf. Disp.* **26**, 137–145 (2018).
14. Tull, B. R. et al. 26.2: Invited paper: high brightness, emissive microdisplay by integration of III-V LEDs with thin film silicon transistors. *SID Symp. Dig. Tech. Pap.* **46**, 375–377 (2015).
15. Akinwande, D. et al. Graphene and two-dimensional materials for silicon technology. *Nature* **573**, 507–518 (2019).
16. Liu, C. et al. Two-dimensional materials for next-generation computing technologies. *Nat. Nanotechnol.* **15**, 545–557 (2020).
17. Manzeli, S., Ovchinnikov, D., Pasquier, D., Yazyev, O. V. & Kis, A. 2D transition metal dichalcogenides. *Nat. Rev. Mater.* **2**, 17033 (2017).
18. Fiori, G. et al. Electronics based on two-dimensional materials. *Nat. Nanotechnol.* **9**, 768–779 (2014).
19. Yu, Z. et al. Realization of room-temperature phonon-limited carrier transport in monolayer MoS_2 by dielectric and carrier screening. *Adv. Mater.* **28**, 547–552 (2016).
20. Li, W. et al. Uniform and ultrathin high-κ gate dielectrics for two-dimensional electronic devices. *Nat. Electron.* **2**, 563–571 (2019).
21. Zhou, J. et al. A library of atomically thin metal chalcogenides. *Nature* **556**, 355–359 (2018).
22. Wang, Q. et al. Wafer-scale highly oriented monolayer MoS_2 with large domain sizes. *Nano Lett.* **20**, 7193–7199 (2020).
23. Kang, Kibum et al. High-mobility three-atom-thick semiconducting films with wafer-scale homogeneity. *Nature* **520**, 656–660 (2015).
24. Tang, H. W. et al. Recent progress in devices and circuits based on wafer-scale transition metal dichalcogenides. *Sci. China Inf. Sci.* **62**, 220401 (2019).
25. Goossens, S. et al. Broadband image sensor array based on graphene–CMOS integration. *Nat. Photonics* **11**, 366–371 (2017).
26. Choi, M. et al. Full-color active-matrix organic light-emitting diode display on human skin based on a large-area MoS_2 backplane. *Sci. Adv.* **6**, eabb5898 (2020).
27. Liu, Y., Huang, Y. & Duan, X. Van der Waals integration before and beyond two-dimensional materials. *Nature* **567**, 323–333 (2019).
28. Yu, J. et al. Van der Waals epitaxy of III-nitride semiconductors based on 2D materials for flexible applications. *Adv. Mater.* **32**, 1903407 (2020).
29. Akinwande, D., Petrone, N. & Hone, J. Two-dimensional flexible nanoelectronics. *Nat. Commun.* **5**, 5678 (2014).
30. Zhuang, Z. et al. High color rendering index hybrid III-nitride/nanocrystals white light-emitting diodes. *Adv. Funct. Mater.* **26**, 36–43 (2016).
31. Li, T. et al. Epitaxial growth of wafer-scale molybdenum disulfide semiconductor single crystals on sapphire. *Nat. Nanotechnol.* https://doi.org/10.1038/s41565-021-00963-8 (2021).
32. Pirkle, A. et al. The effect of chemical residues on the physical and electrical properties of chemical vapor deposited graphene transferred to SiO_2. *Appl. Phys. Lett.* **99**, 122108 (2011).
33. Liu, Y. et al. Approaching the Schottky–Mott limit in van der Waals metal–semiconductor junctions. *Nature* **557**, 696–700 (2016).
34. Huang, Y. et al. Universal mechanical exfoliation of large-area 2D crystals. *Nat. Commun.* **11**, 2453 (2020).
35. Struthers, J. D. Solubility and diffusivity of gold, iron, and copper in silicon. *J. Appl. Phys.* **27**, 1560 (1956).
36. Day, Jacob et al. III-Nitride full-scale high-resolution microdisplays. *Appl. Phys. Lett.* **99**, 031116 (2011).
37. Smets, Q. et al. Sources of variability in scaled MoS2 FETs. In *Proc. 2020 IEEE International Electron Devices Meeting (IEDM)* 3.1.1–3.1.4 (IEEE, 2020).
38. Smithe, K. K. H., Suryavanshi, S. V., Muñoz Rojo, M., Tedjarati, A. D. & Pop, E. Low variability in synthetic monolayer MoS_2 devices. *ACS Nano* **11**, 8456–8463 (2017).
39. Huo, N. et al. High carrier mobility in monolayer CVD-grown MoS_2 through phonon suppression. *Nanoscale* **10**, 15071–15077 (2018).
40. Yu, L. et al. Design, modeling, and fabrication of chemical vapor deposition grown MoS_2 circuits with E-mode FETs for large-area electronics. *Nano Lett.* **16**, 6349–6356 (2016).
41. Polyushkin, D. et al. Analogue two-dimensional semiconductor electronics. *Nat. Electron.* **3**, 486–491 (2020).
42. Sebastian, A. et al. Benchmarking monolayer MoS_2 and WS_2 field-effect transistors. *Nat. Commun.* **12**, 693 (2021).
43. Nomura, K. et al. Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. *Nature* **432**, 488–492 (2004).
44. Wager, J. F. TFT technology: advancements and opportunities for improvement. *Info Disp.* **36**, 9–13 (2020).

Methods

Fabrication of micro-LEDs. The GaN-based blue and green LEDs epi-wafers were grown on a 4-inch sapphire substrate by metal-organic CVD. Blue and green LEDs share the similar epi-structure, which consist of 3-μm undoped GaN buffer layer, a 2-μm Si doped n-type GaN layer, a 3-period InGaN/GaN stress buffer layer, a 15-period InGaN/GaN multi-quantum well layer, a thin AlGaN electron blocking layer and a 250-nm Mg doped p-type GaN layer. Indium content in InGaN multi-quantum wells for blue and green light emission was 13% and 21%, respectively. The circular micro-LED mesa was fabricated by photolithography and dry etching using Cl_2/BCl_3 plasma. The peak external quantum efficiency of 40-μm blue and green micro-LEDs was ~7% and 12%, respectively.

Heterogeneous integration of MoS_2 TFTs and micro-LEDs. For a micro-LED chip, a 240-nm Ti/Al/Ti/Au stack layer was evaporated onto the n-GaN and ITO as the n and p electrodes (Supplementary Fig. 1). Next, the micro-LED chips were spin coated with ~1.3 μm SOG (IC1-1000, FUTURREX) and baked at 200°C for 30 min. Then 20 nm Al_2O_3 was deposited by atomic layer deposition using trimethylaluminium and H_2O as precursors to serve as a passivation layer and TFT support layer.

To integrate MoS_2 TFT, we first used electron beam lithography to pattern backgate electrodes and gate lines on Al_2O_3/SOG, followed by the deposition of Ti/Pd metal and lift-off. Then 20 nm Al_2O_3 was deposited by atomic layer deposition as gate dielectric. Next, the vertical via holes were patterned by photolithography and etched by reactive ion etching (RIE) using CF_4 plasma. Then, we used a PMMA/PDMS stamp to pick up Au film predeposited on ultra-flat silicon wafer (roughness <0.1 nm) and laminated on the fresh as-grown MoS_2. The typical ambient exposure time of MoS_2 was of the order of a few minutes to minimize the surface contamination. After mild heating at 90 °C for 30 min, the MoS_2 was dry-delaminated and transferred to prepatterned chip. The unnecessary Au/MoS_2 was lithographically patterned and removed by sequential Au etching (using Transense TFA) and MoS_2 etching (using CF_4 plasma RIE). Next, metal interconnections between MoS_2 electrodes and the top contact metal of LEDs through the via holes, as well as the data lines, were lithographically patterned and deposited (5 nm Ti /55 nm Pd). In the final step, we opened the MoS_2 channel region by wet etching a gap on the Au film using Transense TFA, followed by thorough de-ionized water rinsing. The etching process was repeated several times to completely remove the Au particles, leading to a very clean exposed MoS_2 surface (Supplementary Fig. 14).

Fabrication of MoS_2 FETs using a conventional process. After CVD growth of monolayer MoS_2 on sapphire, we spin coated PMMA (AR-P 672.045, 2,000 r.p.m., baked at 150 °C for 10 min) and laminated thermal release tape. Next, the sample was immersed in de-ionized water, and the MoS_2 was delaminated from the sapphire and transferred onto chips with prepatterned backgate electrodes and dielectrics. Unnecessary MoS_2 was lithographically patterned and etched by CF_4 plasma RIE. Source/drain electrodes were patterned using electron beam lithography, followed by evaporation of 3 nm Ti/ 35 nm Pd and lift-off. Finally, the devices were annealed in vacuum at 200 °C to improve contacts. Other processes and device parameters were identical to the ultraclean process.

Material and device characterizations. Monolayer MoS_2 single-crystalline films were grown on custom-designed 2-inch C-plane sapphire wafers in a home-build CVD furnace. We used sulfur powder and MoO_3 as precursors, and the growth temperature was typically 1,000 °C. Detailed growth conditions can be found in ref. [31]. The atomic force microscopy characterization of monolayer MoS_2 was performed by an Asylum Cypher S system. Raman spectroscopy was measured with a laser wavelength of 488 nm and a Princeton Instruments SP-2500 spectrometer. Second harmonic generation was performed using an ultrafast laser 1,550 nm wavelength and collected by a photon-counting head. Low-energy electron diffraction (OCI, BDL600IR-MCP) were carried out at room temperature under ultrahigh vacuum and the electron acceleration voltage was 190 eV.

Cross-section scanning electron microscopy and transmission electron microscopy (TEM) samples were fabricated using a FEI Helios 600i dual-beam focused ion beam system. A Pt protection layer was predeposited on the top interface, followed by etching of the surrounding area to form the sample lamella and then direct transfer to a TEM half grid inside the focused ion beam chamber. The high-resolution TEM images were recorded on an image aberration corrected TEM (FEI Titan 80–300 at 300 kV) equipped with a charge-coupled device camera (GatanUltraScanTM 1000).

Electrical measurements of the MoS_2 TFT and 1T1D were carried out by a Keithley 4200 semiconductor parameter analyser in a probe station. Pulse measurements were performed on a Keithley 4225 PMU/RPM.

We used an Ocean Optics fibre integration sphere (FOIS-1) coupled with a QE65 Pro spectrometer for luminance measurements. The 1T1D devices were tested on top of the integration sphere and, as only forward light emission could be collected, the photons after diffuse reflection in the integrating sphere were captured by the optical fibre spectrometer to calculate the corresponding luminance value.

AM driving of the micro-LED display. We used the SPARTAN-6 FPGA from XILINX Co. as the microprocessor of the peripheral circuit, and controlled the shift register through the clock signal to perform voltage operations on the data lines and gate lines of the TFT matrix. The control code was designed by using Verilog Hardware Description Language. The microprocessor and the TFT matrix were bridged through a resistor divider board and the Keithley 2450 was used as voltage source to power the display circuit.

Data availability

The data that support the plots within this paper and other finding of this study are available from the corresponding author on reasonable request.

Code availability

All code used in this work is available from the corresponding author on reasonable request.

Acknowledgements

This work is supported by the Leading-edge Technology Programme of Jiangsu Natural Science Foundation (grant no. BK20202005); the National Natural Science Foundation of China (grant nos. 61927808, 61521001, 61734003, 61861166001, 61851401, 51861145202, 62004104, 61974062, 61921005, 91964202); the Strategic Priority Research Programme of Chinese Academy of Sciences (grant no. XDB30000000); the National Key Research and Development Programme of China (grant no. 2016YFB0404101); the Natural Science Foundation of Jiangsu Province (grant no. BK20202005); the Collaborative Innovation Center of Solid-State Lighting and Energy-Saving Electronics, Research Funds from NJU-Yangzhou Institute of Opto-electronics and the Fundamental Research Funds for the Central Universities, China.

Author contributions

X.W. conceived the research and supervised the project with B.L., R.Z. and Y.S. W.M, F.X., Z.Y., T.T. developed the MoS_2 TFT fabrication and monolithic integration process, fabricated micro-LED structures, conducted electrical measurements and demonstrated AM displays. L.S., W.L., H.N. and N.D. contributed to MoS_2 TFT fabrication. L.L. and T.L. performed MoS_2 CVD growth and characterizations. F.X., K.W. and J.W. performed LED brightness measurements. L.H. and L.S. performed TEM and data analysis. F.Q., X.T. and D.P. contributed to micro-LED fabrication. S.H. designed peripheral circuits and programs. D.L, Y.Z and Y.L. contributed to data analysis. W.M., Z.Y., B.L. and X.W. co-wrote the manuscript with input from other authors. All authors contributed to discussions.

Competing interests

The authors declare no competing interests.

Additional information

Supplementary information The online version contains supplementary material available at https://doi.org/10.1038/s41565-021-00966-5.

Correspondence and requests for materials should be addressed to Bin Liu, Rong Zhang, Yi Shi or Xinran Wang.

Peer review information *Nature Nanotechnology* thanks Deji Akinwande and Deep Jariwala for their contribution to the peer review of this work.

Reprints and permissions information is available at www.nature.com/reprints.