

LETTER

A pipeline row operation method of CMOS image sensors

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Abstract In this paper, we present a pixel array operation method of CMOS image sensor that enables pipeline processing of pixel operations. The sensor frame rate constraint from the delay of pixel array control lines is much relieved by manipulating control phases of adjacent pixel rows simultaneously. An analog frontend readout circuit is proposed to support the row pipeline operation pixel readout. A prototype image sensor was designed with its performance characterized and analyzed.

Keywords: CMOS image sensor, pixel array control, noise

Classification: Integrated circuits (memory, logic, analog, RF, sensor)

1. Introduction

Compared with charge coupled device (CCD), complementary metal oxide semiconductor (CMOS) image sensor has advantages of readout frame rate, cost, and power, which is now extensively used in consumer, surveillance, industrial applications. For scientific imaging, the image sensor needs to deliver high sensitivity [1, 2], high frame rate [3, 4, 5, 6, 7, 8, 9] and low noise [10, 11, 12, 13, 14, 15]. Scientific CMOS image sensors (sCMOS) can provide high sensitivity, high speed, and low noise simultaneously. sCMOS is replacing CCD in scientific applications. The sCMOS sensitivity is mainly improved by sensor fabrication like backside illumination [16], while the speed and noise are related to design improvements. In this paper, we are focusing on a technique to increase the sensor frame rate by pipeline operating the pixel row-level control, while also achieving low noise. The frame rate is normally limited by maximum output data bandwidth, column readout circuits such as amplifiers and ADCs. These limiting factors could be eliminated by designing a more parallelized high-speed interface and readout. The ultimate sensor frame rate limitation comes from physics, which are pixel array control line transmission delay [17] and charge transportation time in silicon [18]. By pipelining the pixel array control phases, it is possible to reduce the control line delay equivalently. In this paper, firstly a row pipeline operation is proposed, with a row-level 1-bit flag memory defining the row pixel exposure status to further shorten the pixel operation time. Secondly, an analog frontend programmable gain amplifier (PGA) struc-

ture suiting the row pipeline operation is designed. The extra noise introduced by this analog frontend is analyzed and simulated. Finally, an image sensor implementing the proposed pipeline row operation method and analog frontend is characterized. The proposed method can effectively eliminate the frame rate bottleneck caused by horizontal transmission delay of pixel control signals with a minimal noise penalty.

2. Traditional 4T rolling shutter pixel control

A typical CMOS image sensor (CIS) chip architecture is shown in Fig 1. The pixel control signals are accessed horizontally, and the pixel output voltage is output vertically to readout circuits located at the top and bottom.

A 4T rolling shutter pixel schematic is shown in Fig 2, the RST, TX, and SEL are pixel horizontal control signals, and the pixel output voltage PIX_OUT is vertically transmitted to readout circuits.

The conventional control timing of a 4T pixel is shown in Fig 3. There are three operations in one line-time: 1) reset floating diffusion (FD), readout circuit samples the reset voltage; 2) charge transfer, readout circuit samples

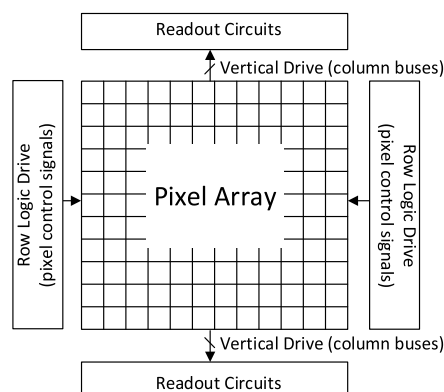


Fig. 1 Typical CIS chip architecture.

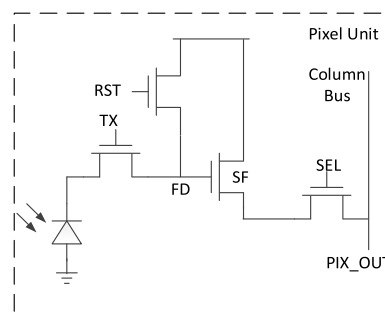


Fig. 2 4T rolling shutter pixel.

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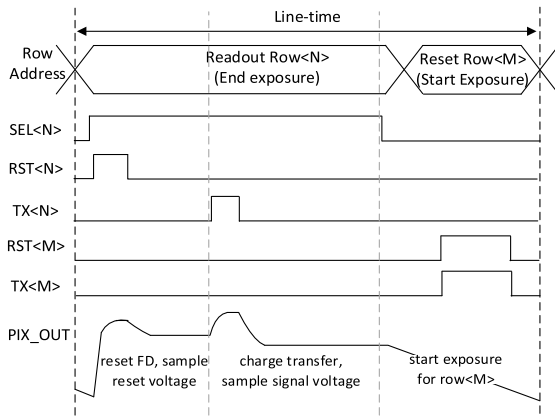


Fig. 3 Conventional 4T pixel control timing.

signal voltage; 3) start exposure for the next row. For the first part of line-time, the control operations end Row<N> exposure and enable pixel output PIX_OUT to readout chain via column bus. In the second part of the line-time, the Row<M> is accessed to start the exposure. As discussed in Section 1, the pixel horizontal control signals (RST, TX, SEL) settling time is one of the critical limiting factors for the sensor's ultimate frame rate. For the RST signal, the voltage on the RST transistor gate should settle to a relatively high voltage to fully turn on the reset transistor. For TX, which defines charge transfer time, is limited by TX signal horizontal settle time and the charge transportation time from the photodiode to FD. The charge transportation time is restricted by electron drift and diffusion, usually in the range of hundreds of nanoseconds [19, 20]. The TX coupling to FD also impacts readout chain PGA speed. The TX coupling will cause a PGA to flip in the opposite direction, which further increases settling time. This issue becomes severe in high sensitivity sensors, which are with minimal capacitance at FD [21, 22, 23]. As for start exposure operation, it is limited again by the horizontal settlement of TX and RST control signals.

To increase the frame rate, double-sided readout with multiple column bus architecture makes vertical settling in parallel [24]. The number of vertical column buses per pixel is normally limited by pixel size, number of metal layers, pixel fill factors. Extensive horizontal parallelism is not realistic. However, the pixel operations could be assigned in a pipeline way. It will significantly shorten the line-time as to be discussed in Section 3.

3. Pipeline pixel row control

The proposed pipeline pixel operation row logic block is shown in Fig. 4 (the N^{th} row logic as an example). There are two row decoders implemented. Address<1> is used for charge transfer, start exposure, and reset FD. Address<2> is for end exposure operation and SEL control. An exposure flag is implemented in the row logic part by a single bit static random-access memory (SRAM) to reduce the start and end exposure operation time. ROW_SET_IN and ROW_RESET_IN are input signals to set or reset the row-based exposure flag. They define the row in exposure or completed exposure, respectively. For rows in exposure, their

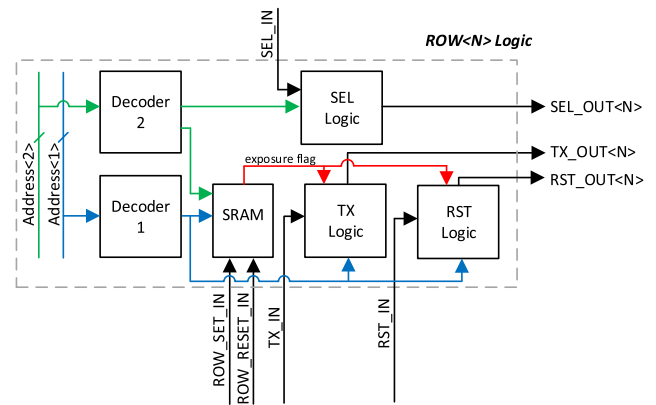


Fig. 4 Row control logic

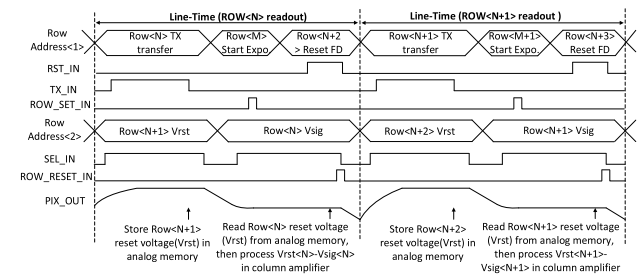


Fig. 5 Pipelined pixel row operation.

exposure state flags are set to logic high. Unless accessed by decoder Address<1>, TX_OUT and RST_OUT are kept continuously low for rows in exposure. If Address<1> access the N^{th} row, the TX_OUT<N> and RST_OUT<N> will follow input control signals. For rows that completed exposure and readout, their exposure flags are reset to logic low, which makes TX_OUT<N> and RST_OUT<N> are high to reset photodiodes constantly. By introducing the exposure flag, the start exposure operation duration equals to SRAM set/reset time. Compared to Fig. 3, the RST and TX pulse to start exposure is no longer needed, which reduces line-time effectively.

The pipelined row operation timing is illustrated in Fig. 5. The first line-time is explained as the following: while Address<1> is pointing to Row<N>, electrons transfer from photodiodes to FD nodes with TX_IN pulse. It should be noted that the FD nodes in Row<N> are reset in the previous line-time, making correlated double sampling (CDS) possible. In the middle of the line-time, Address<1> is pointing to ROW<M>, which starts the ROW<M> exposure by setting the exposure flag via ROW_SET_IN pulse. At the end of the line-time, ROW<N+2> FD nodes are reset then left floating. For the next line-time, the voltage on FD nodes directly output as ROW<N+2> pixel reset voltage. Therefore, compared to Fig. 3, the FD reset time at the beginning of a line-time is saved. Besides, the voltage bumps caused by RST and TX coupling to FD nodes will never show up on column buses. The PIX_OUT only has a pure FD reset voltage and then an exposure signal voltage, which relieves column buses and readout amplifier settling. Address<2> works together with SEL_IN to make ROW<N+1> reset voltage and ROW<N> signal voltage output to column buses. After ROW<N> finished readout, the ROW_RESET_IN pulse

makes ROW<N> in completed exposure state. In the next line-time, the operations repeat for ROW<N+1> readout.

4. Analog readout for pipeline pixel control

CIS column amplifier is widely realized by switch capacitor (SC) structure due to its low power consumption, high area efficiency, and high gain accuracy [25, 26, 27, 28]. As discussed in Section 3, the reset voltage and signal voltage in one line-time are from two rows. The analog readout frontend, which supports pipeline row readout, must have the ability to store and load reset voltage.

The proposed SC amplifier that supports pipeline pixel control is shown in Fig. 6(a). C_{in_a} and C_{in_b} are input capacitors. C_f is the feedback capacitor. The amplifier gain is:

$$Gain = \frac{C_{in_a}}{C_f} = \frac{C_{in_b}}{C_f} \quad (1)$$

Compared to conventional SC amplifier, two input capacitors are implemented in parallel. In the sample phase, these two capacitors are as pixel reset voltage sample and hold capacitors. In the amplification phase, the difference between the previously stored reset voltage and present exposure signal voltage on PIX_OUT will be amplified. S1 and S2 switches are interleaved controlled to sample and hold the reset voltage or signal voltage on PIX_OUT. INIT is the amplifier initialization switch to initialize the amplifier. S/H switch is the sample and hold switch for following column ADC processing.

The amplifier control timing is depicted in Fig 6(b). When PIX_OUT output ROW<N+1> reset voltage, the S1 switch is on. Once the pixel reset voltage is settled on the column bus, S1 is off to hold this voltage on C_{in_a} left node. During the S1 high period, INIT is off, leaving C_{in_a} right node and amplifier out with V_{ref} . Subsequently, the decoder address moves to ROW<N>, and switch S2 is on, to sample the Nth

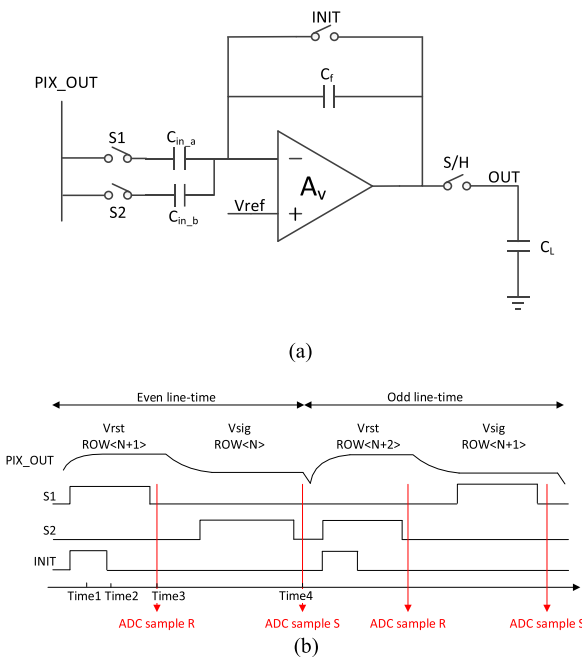


Fig. 6 Analog readout schematic and timing for pipeline pixel control.

row pixel exposed signal voltage. Since the C_{in_b} left node has already been stored with ROW<N> reset signal voltage in the previous line-time, the voltage difference between ROW<N> pixel reset and exposure signal will force charge in C_{in_b} transfer to C_f . The amplifier outputs the amplified CDS voltage, with KTC noise from pixel cancelled.

5. Noise analysis on pipeline row operation

To investigate the proposed SC PGA readout noise, the amplifier output resistance is assumed as infinity. The schematic in Fig. 6(a) is transferred to the small-signal equivalent circuit as shown in Fig. 7. $V_{n,pix1}$, $V_{n,pix2}$ are pixel noise including source follower flicker and thermal noise. $V_{n,s1}$, $V_{n,s2}$ and $V_{n,INIT}$ are switch thermal noise. R_{s1} and R_{s2} are resistance from S1 and S2 switches. $g_{m,sf}$ and $g_{m,ota}$ are the transconductance of source follower and amplifier. C_B and C_L are the pixel array column capacitance and PGA load capacitance respectively.

In Fig. 6(b), four time points (Time1 to Time4) are drawn in the even line-time. The even and odd line-time have the same noise result, as the operation are identical. Therefore, only even line-time noise is analyzed. At Time1, both S1 and INIT are on. At Time2, INIT is completely off, the noise from $V_{n,pix}$ and $V_{n,s1}$ is sampled as amplifier reset noise [29, 30]. The noise from $V_{n,INIT}$ will redistribute to V_{out} and V_C node when INIT off. The noise eventually at V_C is negligible due to the capacitive feedback and the high open-loop gain. Nevertheless, as the S1 is on, the noise from pixel and S1 still continuously transfers to V_{out} after INIT off. In between Time2 and Time3, the S1 switches off, the noise from pixel and resistor R_{s1} at V_{out} is frozen which will be quantized by ADC sample R, it will be cancelled by the ADC digital CDS (subtraction of ADC sample R and sample S). The noise on V_{out} node due to S1 off will be neglected in the following analysis.

The noise from PGA operational transconductance amplifier (OTA) and the OTA noise transfer function to V_{B1} node is:

$$V_{n,ota}^2 = \frac{4KT}{g_{m,ota}} \quad (2)$$

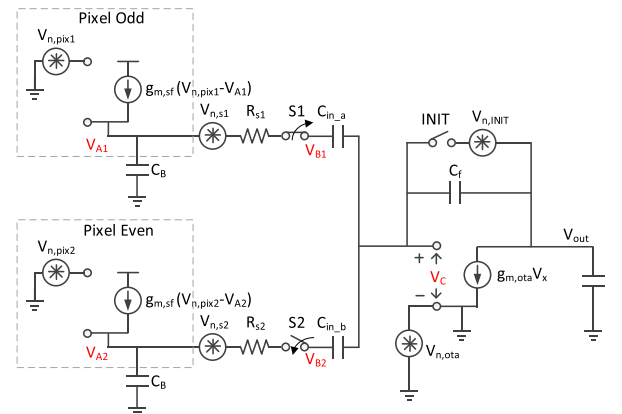


Fig. 7 Small signal equivalent of pipelined SC PGA

$$H_{ota}(s) \approx \frac{g_{m,ota}(C_{in_a} + C_f)C_f}{(C_L C_{in_a}(C_{in_a} + C_f) + C_{in_a}^2 C_f)s + C_{in_a} C_f g_{m,ota}} \quad (3)$$

The noise voltage at V_{B1} and V_C is sampled by S1 off, it will impact on the overall noise. As V_C node will be nearly noiseless due to capacitive feedback and open-loop gain, the noise will show up on V_{B1} node only. The noise on V_{B1} will add to final output noise when S1 is on for pixel exposure signal readout. The S1 switch thermal noise and its transfer function to V_{B1} node are in equation (4) and (5):

$$V_{n,s1}^2 = 4KTR_{s1} \quad (4)$$

$$H_{R,s1}(s) \approx \frac{(C_L C_B C_f)s^2 + (C_B g_{m,ota} C_f)s + g_{m,ota} g_{m,sf} C_f}{(C_{in_a} C_B C_L R_{s1})s^3 + [C_L C_B (C_{in_a} + C_f)]s^2 + (C_B C_f g_{m,ota})s + C_f g_{m,ota} g_{m,sf}} \quad (5)$$

The pixel noise and its transfer function to V_{B1} node are in (6) and (7), where K_f and γ are the flicker and thermal noise coefficients.

$$V_{n,pix1}^2 = \frac{K_f}{f} + \frac{4KT\gamma}{g_{m,sf}} \quad (6)$$

$$H_{pix}(s) \approx \frac{(C_L C_f g_{m,sf})s + C_f g_{m,sf} g_{m,ota}}{(C_L C_B C_f C_{in_a} R_{s1})s^3 + [C_L C_B (C_{in_a} + C_f)]s^2 + (C_f C_B g_{m,ota})s + g_{m,sf} g_{m,ota} C_f} \quad (7)$$

In the next line-time, the V_{B1} node will be connected to the odd pixel again. Since the amplifier will subtract the voltage difference, the noise on V_{B1} node will be filtered by CDS noise power transfer function as in (8), where T_s is sample interval.

$$H_{CDS}(f)^2 = 4\sin(\pi T_s f)^2 \quad (8)$$

The final total noise power is:

$$V_{n,tot}^2 = \int_0^\infty [(\|V_{n,ota}(f)\|^2 + V_{n,s1}^2 \|H_{R,s1}(f)\|^2 + V_{n,pix1}^2 \|H_{pix}(f)\|^2) H_{CDS}(f)^2] df \quad (9)$$

The pipeline row operation total noise discussed above and conventional operation (as in Fig. 3) total input referred noise are plotted in Fig. 8. The parameters are with C_{in_a} ranging from 40 fF to 640 fF, C_f fixed to 40 fF, R_{s1} and R_{s2} equal to 50 kOhm. The $g_{m,sf}$ and $g_{m,ota}$ is 100 uS and 22 uS respectively. K_f is $2.5nV^2/Hz$ and γ is 1. C_L is 200 fF, C_B is 5.5 pF. T_s is 1.25 us for pipeline row operation, 0.62 us for conventional.

Compared with conventional operation, the pipeline operation has higher noise due to the extra voltage sampling. However, as the PGA gain increases, the noise is attenuated to a relatively low level. The noise difference between conventional and pipelined operation is reduced as well.

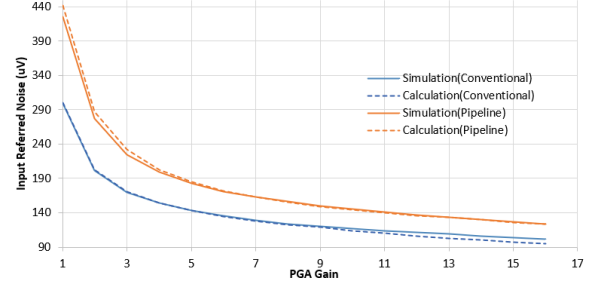


Fig. 8 Estimated noise versus different PGA gain

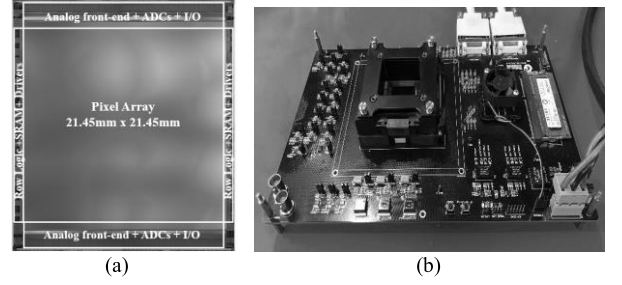


Fig. 9 Sensor chip photo (a) and test system (b)

Table I Sensor pixel array delay parameter summary

Signal Name	Signal Dir.	R_{tot} (k Ω)	C_{tot} (pF)	τ (ns)	Needed Settle times (conventional)	Needed Settle times (pipeline operation)
SEL	x-axis	4.7	12.3	14.5	2	4
TX	x-axis	3.2	21.2	17.2	4	0
RST	x-axis	4.3	11.4	12.3	4	0
PIX_OUT	y-axis	2.3+10 (SF)	5.5	67.7	4	2

6. Experimental results

The prototype sensor with pipelined row operation was developed and characterized with EVMA1288 standard. The die photo and test system are shown in Fig. 9.

The delay parameters of the prototype sensor pixel array are summarized in Table I. For horizontal signals, their time constant is $R_{tot}C_{tot}/4$ with consideration of distribution model and double side driving. For column bus output PIX_OUT, the time constant from bus wire is $R_{tot}C_{tot}/2$.

Supposing horizontal signals need 3τ settling time and vertical PIX_OUT requires 5τ settling time. For the conventional timing, minimum TX and RST pulse high period is 300 ns and 100 ns respectively, the timing depicted in Fig 3 needs 2.5 us line-time to fulfill pixel operation. For pipeline row operation, the RST and TX settle time and minimum logic high period constraint are removed, because 1) they operate in parallel with pixel output; 2) the start and end exposure operation are achieved by digital pulses. Beyond that, the time for PIX_OUT settle is relieved since RST and TX coupling on FD node is eliminated. With the pipeline row operation, the 1.25 us line-time can be realized.

The measurement of pixel output with conventional and pipelined row operation under 1.25 us line-time is shown in Fig. 10. The PIX_OUT waveform from pixel array rightmost column bus is plotted. For conventional operation,

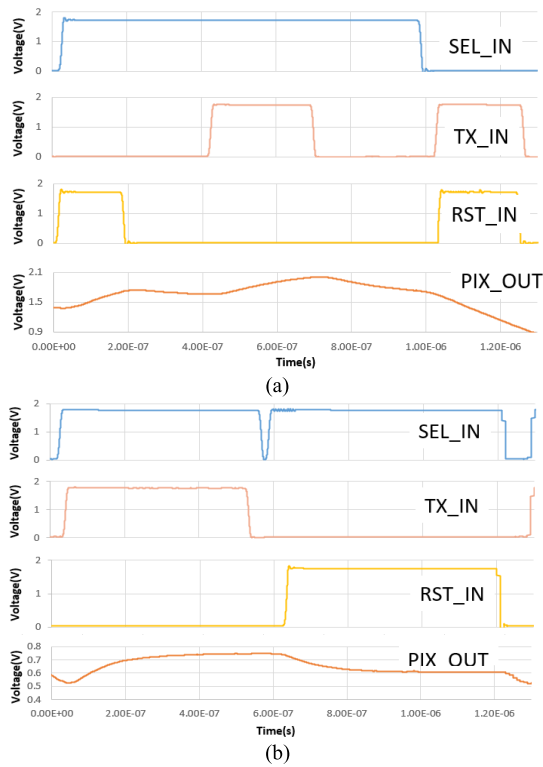


Fig. 10 Measured sensor input operation timing and PIX_OUT under 1.25 us (a) with conventional operation, (b) with pipeline row operation

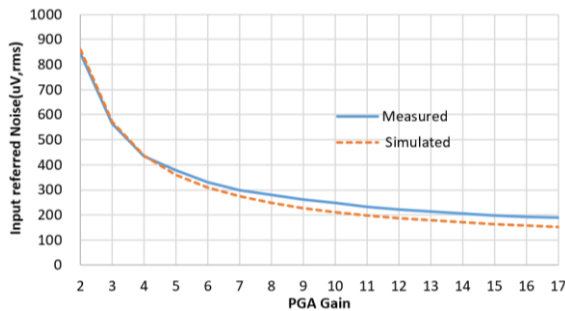


Fig. 11 Measured analog readout chain input referred noise

the PIX_OUT is not settled due to the limitations described above. The pipeline operation provides proper settling on PIX_OUT. In addition, for pipeline row operation, the logic high period for TX and RST can be further increased, making lower image lag and better image uniformity.

The sensor input referred noise (including pixel SF noise, PGA and ADC) with pipeline row operation under different PGA gain has been measured and is shown in Fig. 11. Due to the high-speed 8-bit column ADC quantization noise and ramp ADC comparator noise, the measurement results show higher noise than Fig. 8 which is not including the ADC noise. Under high PGA gain, the total input-referred noise is near 200 uV. In this sensor design, the pixel conversion gain is 100 uV/e, resulting $2e^-$ sensor input referred noise.

The sensor specifications and comparison with previous works are summarized in Table II. The proposed pipeline row operation has achieved a relatively high-speed readout in large array physical size, with the minimum input refer noise of $2e^-$. It shows that the proposed method has good performance if both speed and noise are required in large

Table II Sensor specifications and comparison with pervious works

Reference	This Work	[12]	[11]	[15]
Pixel Readout Technique	Pipelined row operation	Conventional	Conventional	Conventional
Process	180nm CIS	180nm CIS	180nm CIS	180nm CIS
Active array size	21.45mm x 21.45mm	13.3mm x 13.3mm	16.6mm x 14.0mm	7.7mm x 7.7mm
Pixel type	4T rolling	5T HDR rolling	5T global/rolling	4T rolling
Line-time	1.25us	2.56us	9.25us	250us ^a
Column Gain	x1 – x 17	x1 – x11	x1/x2/x10/x3 0	n/a ^b
Min. Input refer. Noise	$2e^-$	$2e^-$	$1.28e^-$	$1.2e^-$ ^a

a: 64 times of Correlated Multiple Sampling (CMS) is applied

b: no analog amplified implemented

array sensors.

7. Conclusion

This paper has presented a pipeline row operation method. The conventional pixel control timing is assigned in parallel, which breaks the physical settling time limitation for both horizontal and vertical signal transmission of the array. The analog frontend circuit that supports pipeline row operation is designed and measured. Compared with conventional operation timing, the sensor line-time is reduced from 2.5 us to 1.25 us. The proposed method is easy to be implemented and suitable for low noise, large format CMOS image sensors.

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