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Exploring Low Power and Ultrafast Memristor on p-Type van der Waals SnS

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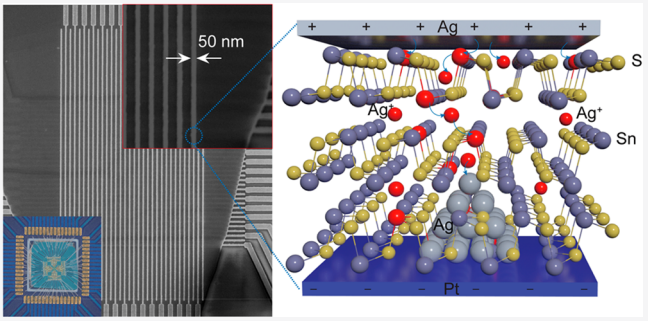
ABSTRACT: Memristor devices that exhibit high integration density, fast speed, and low power consumption are candidates for neuromorphic devices. Here, we demonstrate a filament-based memristor using p-type SnS as the resistive switching material, exhibiting superlative metrics such as a switching voltage ~0.2 V, a switching speed faster than 1.5 ns, high endurance switching cycles, and an ultralarge on/off ratio of 10^8. The device exhibits a power consumption as low as ~100 fJ per switch. Chip-level simulations of the memristor based on 32 × 32 high-density crossbar arrays with 50 nm feature size reveal on-chip learning accuracy of 87.76% (close to the ideal software accuracy 90%) for CIFAR-10 image classifications. The ultrafast and low energy switching of p-type SnS compared to n-type transition metal dichalcogenides is attributed to the presence of cation vacancies and van der Waals gap that lower the activation barrier for Ag ion migration.



KEYWORDS: *low power, ultrafast, SnS, memristor, neuromorphic computing*

INTRODUCTION

Two-dimensional (2D) materials have been researched extensively in memristor devices because they can form atomically thin tunneling barriers and exhibit readily tunable electrical properties.[1−5] By incorporation of 2D materials into a metal/insulator/metal (MIM) type memristive device, superior performance compared to the traditional metal-oxide-based memristor has been reported. For example, a low switching voltage of 0.25 V has been achieved in a Cu/MoS_2/Au memristor with bilayer MoS_2,[3] good thermal stability up to 340 °C was reported in a graphene/$MoS_{2-x}O_x$/graphene heterostructure,[4] and fast switching speed up to 10 ns and high reliability can be realized by inserting layered h-BN into the MIM structure.[6−8] Due to its excellent electrical performance, the 2D memristor is considered as one of the most promising candidates for neuromorphic computing.[1,9−11] As a brain-inspired information processing model, neuromorphic computing has been an important tool to realize artificial intelligence by mimicking the energy efficiency and versatility of the human brain.[12,13] To mimic the human brain, artificial synapses based memristor devices should possess fast speed, low power consumption, and high integration density and exhibit multiple levels of synapse strength for implementing synaptic learning processes. However, many of the above desirable metrics were achieved in isolation or coexisting with only a few other metrics. It is rare to have a material that can possess a combination of all these metrics.[13]

In the MIM structure memristor devices, the resistive switching is believed to originate from the occupation of vacancies by oxidized metal ions.[6,14,15] The chalcogen vacancies in transition metal dichalcogenides (TMDs) were demonstrated to be useful for electrochemical metallization memories, where migration of metal ions from active electrode leads to the formation of conductive filament.[14,15] Different from most TMDs, which are intrinsic n-type semiconductors due to the chalcogen vacancies,[16,17] SnS, a semiconductor with energy gap of ~1.1 eV,[18] is intrinsically p-type because of Sn vacancies.[19−21] In principle, Sn vacancies should be more energy favorable for the migration of metal ions than chalcogen vacancies.

In this work, we report a memristor device fabricated using SnS with thickness in the range of 10−40 nm. The vertical junction device shows low switching voltage (0.2 V), ultrafast switching speed (1.5 ns), large on/off ratio (10^8), and high reliability. The chip-level simulation of a convolutional neural network (CNN) on the CIFAR-10 data set based on 32 × 32 Ag/SnS/Pt arrays achieved a high recognition accuracy with

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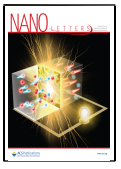

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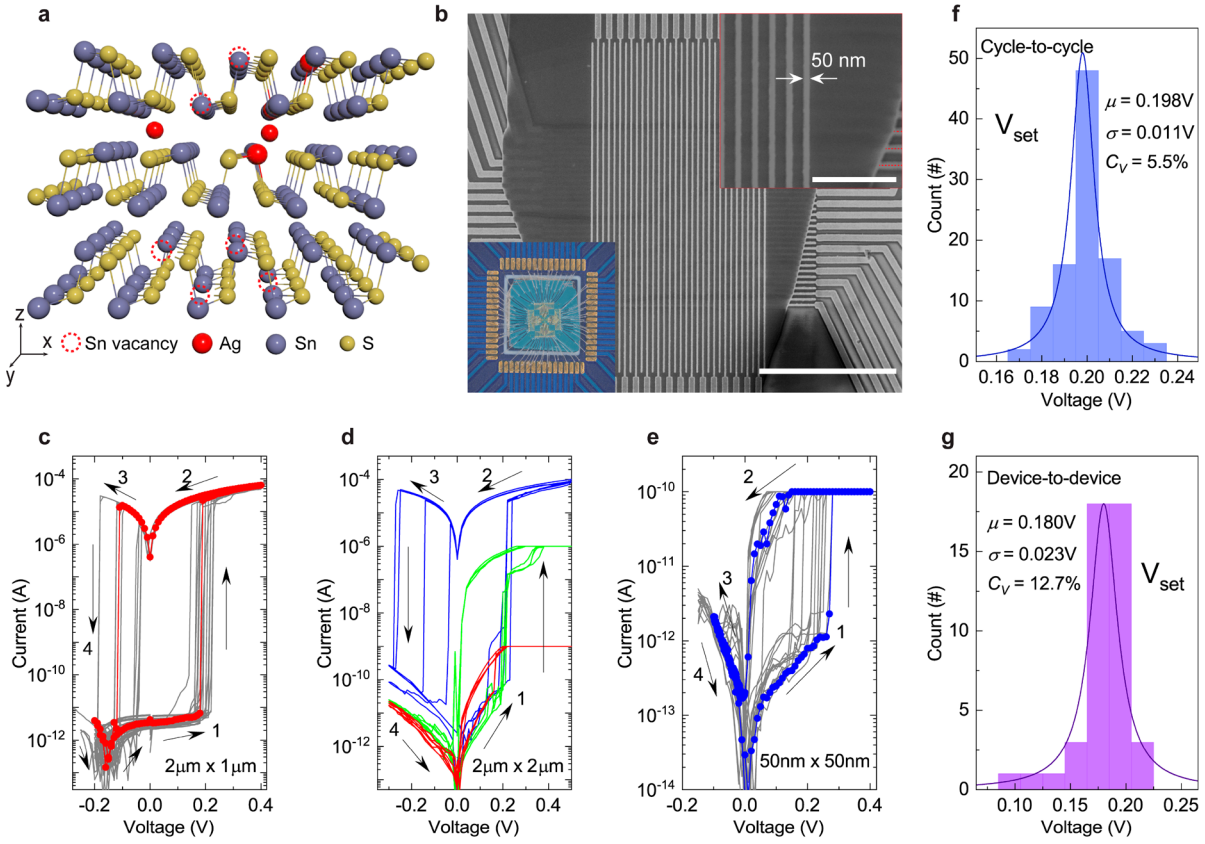

Figure 1. Crossbar array, repeatable threshold switching, and high reliability of Ag/SnS/Pt memristors. (a) Schematic crystal structure of SnS. Sn vacancies are highlighted and some Sn vacancy sites and van der Waals gap are occupied by Ag atoms. (b) SEM image of the 32 × 32 high-density memristive crossbar array with 50 nm feature size. Scale bar, 5 μm. The insets are the optical image of the array bonding to the measurement chip and the zoom in SEM image of the array. Scale bar, 1 μm. (c) Repeatable nonvolatile bipolar resistive switching of Ag/SnS/Pt device without current compliance (CC; see device array in Figure S1a, Supporting Information). (d) Resistive switching of Ag/SnS/Pt device with different CC. (e) Volatile resistive switching of 32 × 32 array with 50 nm × 50 nm feature size under 10^{-10} A CC. (f) Cumulative distribution of set voltages of 100 cycles measured on one single device. (g) Cumulative distribution of set voltages of 45 devices.

great energy efficiency. The outstanding performance of the SnS memristor device is attributed to facile and robust Ag filament formation due to the presence of Sn vacancies. Density functional theory (DFT) calculation reveals a low migration barrier for Ag^+ ion moving from interstitial sites in the van der Waals gap to Sn vacancies.

RESULTS AND DISCUSSION

Ag/SnS/Pt Device Switching Performance. Figure 1a shows the crystal structure of SnS. Cation vacancies are highlighted, which can be occupied by Ag atoms. Ag ions can also intercalate into the van der Waals gap. We used exfoliated SnS flakes of ~13 nm thickness for fabricating a 32 × 32 memristive crossbar array with 50 nm feature size, as shown in Figure 1b. Raman characterization (see Figure S2, Supporting Information) verifies that the exfoliated flakes show similar Raman fingerprint peaks to bulk SnS.[22,23] To construct the MIM crossbar structure, inert Pt electrodes were used as the bottom electrode while electrochemically active Ag serves as the top electrode. The $I-V$ curves of SnS devices show highly repeatable threshold switching (Figure 1c–e) between the high resistance state (HRS) and low resistance state (LRS) for multiple cycles. In addition, volatile and nonvolatile resistive switching could be achieved through control of compliance current (CC). Without using CC to limit the current, the $I-V$ curves show a nonvolatile switching behavior between 0.15 and 0.2 V with a high on/off ratio of ~10^8. The switching exhibits a sharp turn on with a slope of ~0.1 mV/decade. When applying CC $\leq$ 1 μA, the nonvolatile resistive switching changes to volatile switching, as shown in Figure 1d. In the volatile state, the SnS device spontaneously relaxes back to the HRS state, whereas a negative reset voltage is needed to switch the device back to HRS without CC. The volatile state can be explained by Rayleigh instability and spontaneous diffusion of Ag atoms that cause dissolution of the filament. The ability of SnS devices to operate in both volatile and nonvolatile modes enables the emulation of a wide range synaptic plasticity behaviors.[7] $I-V$ curves of the 32 × 32 array with 50 nm feature size are shown in Figure 1e. The resistive switching happens around 0.2 V and shows volatile behavior with 10^{-10} A CC. The high current capability (Figure S5) and large on/off ratio indicate that the SnS conductive filament devices can be used as selectors.[24]

To demonstrate the reliability of our SnS device, SnS crossbar arrays with a total of 45 devices were measured. The set voltages (V_{set}) of 1000 $I-V$ curves collected from 45 devices have been statistically analyzed, and the mean value (μ), standard deviation (σ), and coefficient of variation (C_v) are shown in Figure S1. The device yield is almost 100%, and V_{set} shows cycle-to-cycle variability in a single device down to 5.5% and device-to-device variability in 45 devices down to 12.7%, as shown in Figure. 1f,g. The optical images of the

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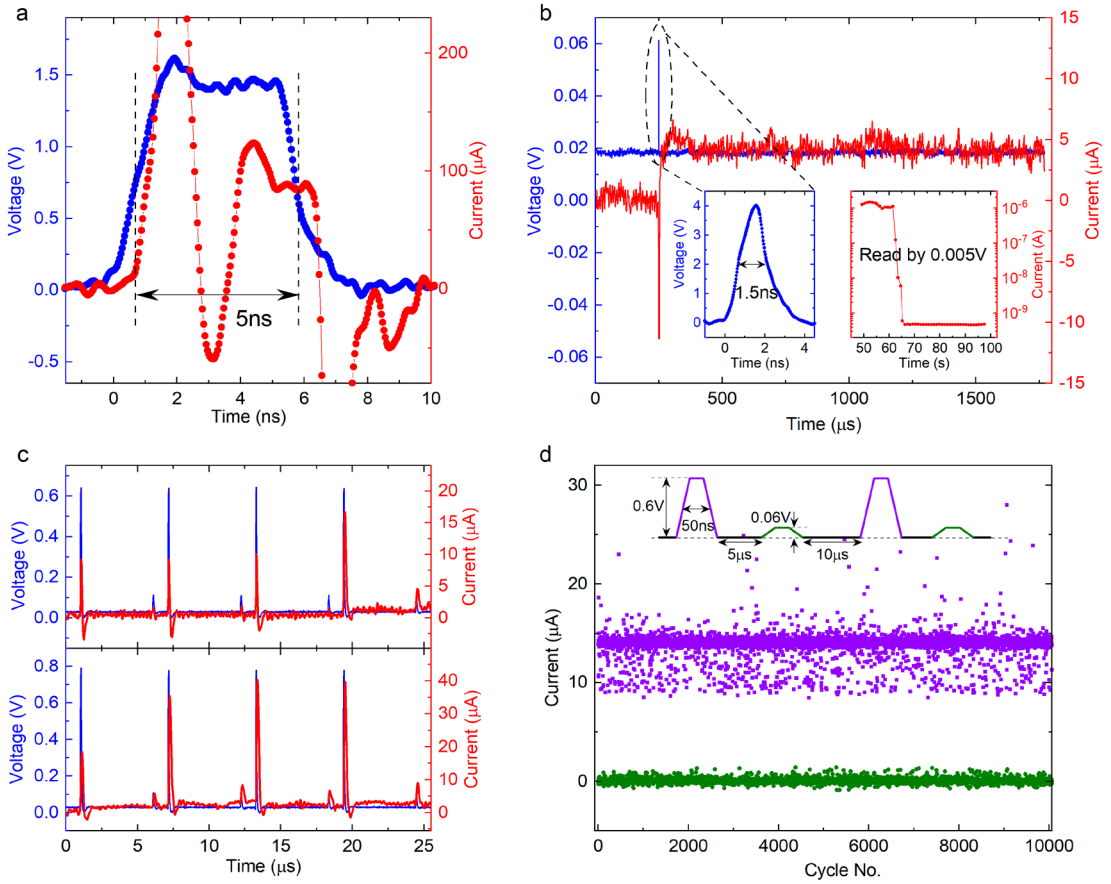

Figure 2. Ultrafast switching of Ag/SnS/Pt device. (a) Ultrafast switching curve of the device with 1.5 V/5 ns voltage set pulse. The voltage pulses are shown in blue, and the response current signal is shown in red. (b) Ultrafast switching curve of the device with 4 V/1.5 ns voltage pulse. Read voltage, 0.02 V. The inset at left is the pulse waveform of the 4 V/1.5 ns voltage pulse, and the inset at right is the DC measurement data of the SnS device with 0.005 V after this pulse measurement. (c) High-speed switching characteristics of SnS device with 0.6 V/50 ns and 0.8 V/50 ns pulse train, followed by 0.06 V/50 ns and 0.08 V/50 ns pulse to read the state within 5 μs 0.02 V bias interval after switch. (d) Endurance-cycling data of SnS device. The inset is the applied waveform, which consists of a 0.6 V/50 ns (shown in purple) set pulse followed by a 0.06 V/50 ns (green) read pulse. The interval between the set and read pulses is 5 μs, and the interval between adjacent cycles is 10 μs. The response currents for set and read pulses are plotted in the same color. High endurance switching achieved for 10 000 cycles.

arrays and the repeated $I-V$ curves of all devices are listed in Figure S1. Most of the devices do not need a forming process, which we attribute to the abundant Sn vacancies in SnS, ~1.5 × 10^{17} cm^{-3} (Figure S14), which aid the ion diffusion processes.

To measure the switching speed of the SnS device, high frequency pulse data were collected (see Figure S4, Supporting Information, for details). We demonstrate that conductive filament switching in the SnS device has a switching speed as fast as 1.5 ns, which is limited only by the high frequency pulse voltage source we used. As shown in Figure 2a, the SnS device could be switched to the LRS with a set pulse of 1.5 V/5 ns (pulse width is determined with full width at half-maximum (fwhm)). To reduce the capacitance effect in high frequency measurement, the resistance before and after the applied set pulse was measured to further characterize the switching speed of the SnS device (Figure 2b). A sharp current increase was recorded with a reading voltage of 0.02 V after a 4 V/1.5 ns set pulse, and the device relaxes back to the HRS spontaneously after 65 s (inset, Figure 2b), suggesting that the SnS device possesses an ultrafast switching speed of 1.5 ns.

Moreover, the relaxation time of the SnS device is dynamically configurable by the magnitude and width of the switching pulse, which is useful for a wide range of synaptic plasticity behaviors.[7] The tunable temporal response may be related to the ultrafast diffusion dynamics of Ag ions in SnS. In Figure 2c, 0.6 V/50 ns and 0.8 V/50 ns set pulses were followed by a read pulse of 0.06 V/50 ns or 0.08 V/50 ns, respectively, within 5 μs after switching to the LRS. For the 0.6 V/50 ns set pulse, the device switches to LRS and relaxes back to HRS within 5 μs, 0.02 V bias interval, until the fourth pulse. If the pulse amplitude is increased to 0.8 V, after only one pulse, the device cannot relax back to HRS. These results indicate that larger pulse amplitude results in thicker filament formation and requires a longer time to relax (see Figures S6–S9, Supporting Information, for the detailed control of relaxation time with pulse magnitude). The device develops a nonvolatile state with retention time larger than 10^5 seconds when pulse amplitude is increased to 1 V/1 μs (Figure S9). A 0.5 V/50 ns setting pulse produces ~5 μA switching current (Figure S7d); this gives a low power consumption down to ~100 fJ per switch, which is smaller than the reported minimum switching energy of ion migration based memristor devices.[10] The endurance was tested by subjecting one device to 10 000 switching cycles, which is competitive in 2D material-based memristors,[3,8,14] as shown in Figure 2d, where stable performance could be obtained throughout.

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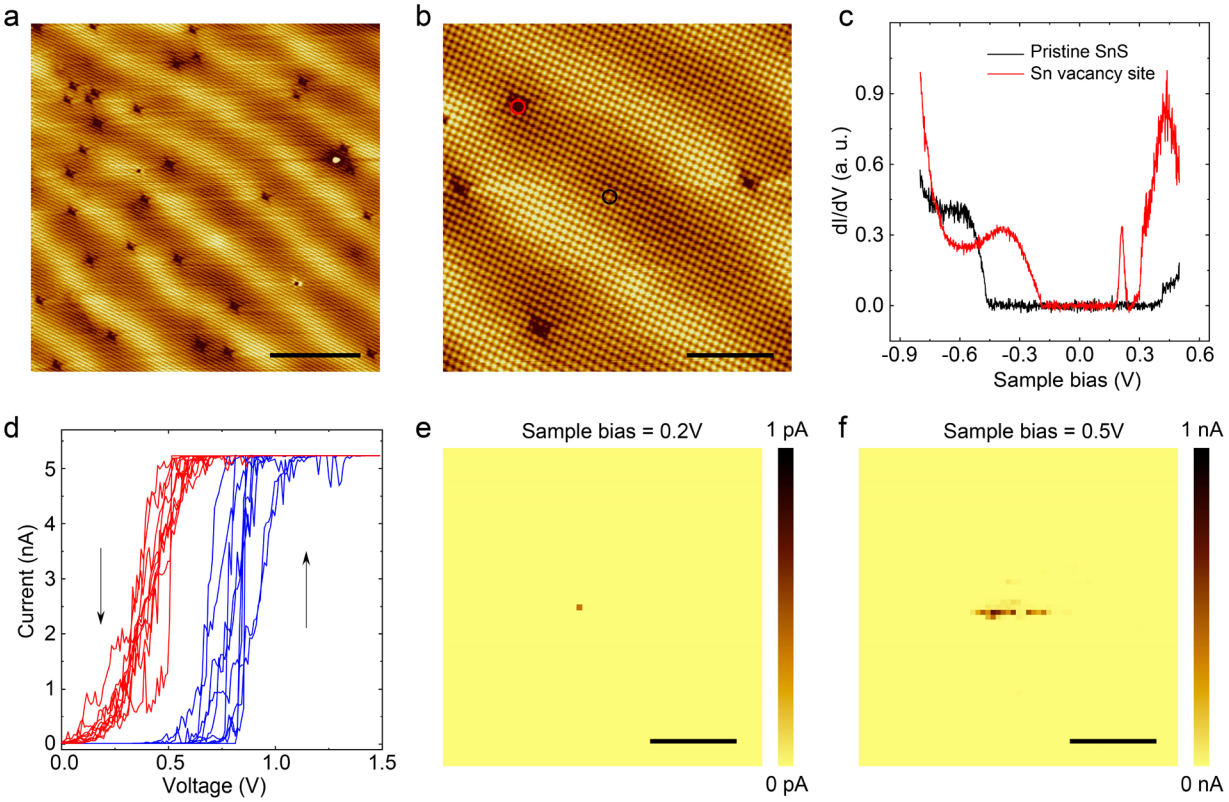

Figure 3. STM image of SnS surface and in situ observation of the threshold switching process and the formation of Ag conductive filament by CAFM. (a) Large area STM image. Scale bar, 10 nm. (b) Zoom-in showing defects identified as Sn vacancies. Scale bar, 5 nm. (c) dI/dV versus sample bias plot: black line denotes pristine area with a gapped region characteristic of SnS, while red line is collected on Sn vacancy sites, showing resonance peaks from charging of Sn vacancy. (d) In situ measurement of the $I-V$ curves of SnS flake with thickness of 10 nm in CAFM. (e, f) CAFM current mapping after repeated $I-V$ sweep with 0.2 and 0.5 V sample bias. Scale bar, 100 nm.

Ag/SnS/Pt Device Switching Mechanism. For some devices, the switching voltage is as low as 0.05 V (Figure S1), which is on the same order as biological neurons (50−120 mV).[25] To understand the exceptionally low activation barrier for filament formation, we analyzed the defect density on the surface of SnS using scanning tunneling microscopy (STM) (Figure 3a−c), where Sn vacancies as high as $\sim 1.0 \times 10^{18}$ cm^{-3} were observed after the growth of the crystal. It is well documented in the literature that Sn vacancies are major acceptor states in SnS;[19−21] thus acceptor-related resonance features originating from Rydberg-like bound hole states can be seen in the scanning tunneling spectra (STS) at both positive and negative sample biases. STS dI/dV spectra revealed a broad peak centered at around −0.4 eV, and a sharp peak at +0.2 eV in the gapped region, compared to a rather featureless gap of 0.9 eV on the pristine region. At positive sample bias of +0.2 eV, the acceptor states move above Fermi level and become deionized; this abruptly reduces the Coulomb repulsion for electrons that are injected into the conduction band, leading to a sharp resonance peak.[26] The apparent dimension of the Sn defects is 372 pm, which is much larger than the diameter of Ag^+ ions (252 pm), suggesting that Sn vacancies can serve as open channels for Ag ion migration in SnS.

To directly visualize the formation of the conductive filament channel, conductive atomic force microscopy (CAFM) was used to observe the switching process of SnS by interfacing it with a Ag substrate that serves as the bottom electrode. When the sample bias was swept between 0 to 1.5 V, an abrupt current increase can be detected in $I-V$ curves (Figure 3d). Following repeated resistive switching, a conductive channel can be clearly seen in the current map using 0.5 V sample bias (Figure 3f), which originates from the formation of a conductive Ag filament path. Since it is difficult to observe the vertical filament formation in the crossbar structure, we fabricated a planar Ag−SnS−Pt device to observe the Ag filament formation mechanism in real time using the scanning electron microscope (SEM). By application of +0.4 V bias to the Ag electrode (Pt ground), conductive filament formation in the Ag−Sn−Pt planar device was recorded in time sequence in Figure S12. We have also fabricated lateral devices on h-BN or MoS_2 using the same electrode configurations, but no conductive filament formation was observed under the same operating conditions.

To obtain insight into the migration pathways and energetics involved, DFT calculations were carried out in the bulk SnS system where Ag's migration process between various interstitial position and substitutional sites was investigated. The calculation method and results are listed in Figures S16−S20. According to our nudged-elastic-band (NEB) calculations, the migration energy barrier for Ag^+ hopping from an interstitial site at the van der Waals (vdW) gap to a Sn vacancy is only ∼0.05 eV, suggesting that the low activation energy for occupying Sn vacancies may originate from Ag ion migration through the interstitial sites within the vdW gap. It should be noted that almost all vdW 2D materials show a much higher switching voltage than SnS (See Table S3, Supporting Information, for the comparison of the DC characteristics

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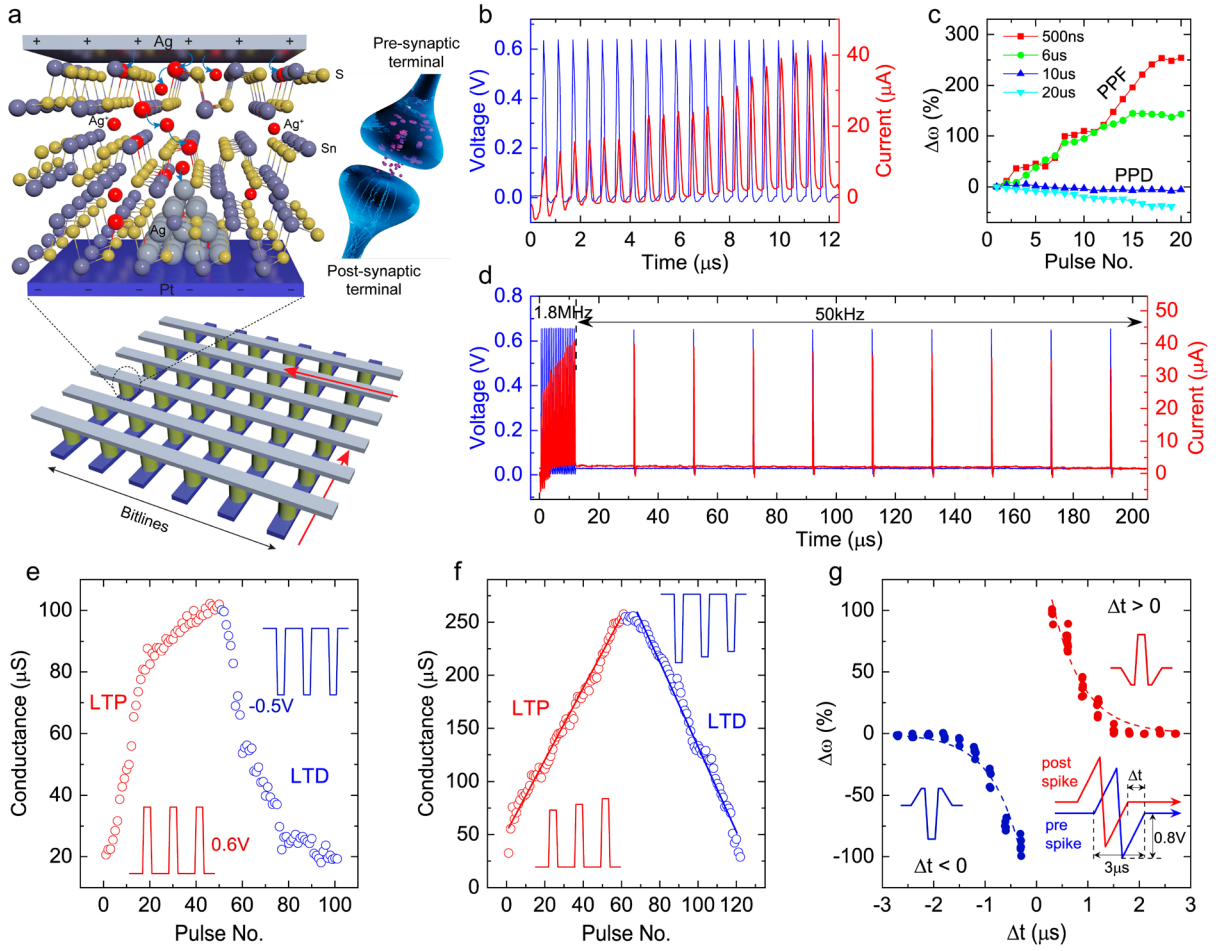

Figure 4. Short-term and long-term synaptic plasticity of Ag/SnS/Pt devices. (a) Schematic illustration of the ion dynamics of Ag/SnS/Pt based crossbar array. (b) Short-term PPF behavior demonstrated by experimental data with 0.65 V/50 ns pulse train (pulse interval 500 ns). (c) Conductance (weight) modulation with different pulse interval. (d) PPD following PPF behavior is realized by a train of voltage pulses with 0.65 V/50 ns but different frequencies. The device begins with PPF at high frequency pulse train (1.8 MHz), followed by PPD with low frequency pulses train (50 kHz). (e) LTP and LTD process measured with identical voltage pulses (pulse width/interval: 100 ns/2 μs). (f) LTP and LTD process measured with stepwise voltage pulses. For LTP, the pulse amplitude increases from 0.6 to 0.9 V with 5 mV steps; for LTD, the pulse amplitude decreases from −0.54 V to −0.42 V with 2 mV steps. Pulse width/interval, 100 ns/2 μs. (g) Conductance (weight) change of Ag/SnS/Pt device as a function of Δt. The time difference between prespike and postspike is denoted as Δt.

between SnS and reported devices).[3,6−8,14] Even at monolayer thickness, TMDs such as MoS_2, $MoSe_2$, WSe_2, and WS_2 typically required threshold voltages >1 V when used as resistive switching layers, which are much higher than that of SnS-based memristor devices using 10−40 nm thick SnS, suggesting that the low voltage filament activation is unique to p-type SnS with abundant cation vacancies.

Emulation of Synaptic Plasticity. Figure 4a illustrates the ion dynamics of the Ag/SnS/Pt based crossbar device next to a biological synapse. Ag^+ ions from the Ag electrode would occupy the Sn vacancies or interstitial sites in SnS and diffuse under the external electrical field and then be reduced to Ag atoms at the cathodes, causing the growth of the Ag filament. As shown in Figure 4b, the device exhibits paired-pulse facilitation (PPF) behavior when 0.65 V/50 ns pulse train with 500 ns pulse interval is applied. The conductance (referring to the weight of synapse) increases with the increase of pulse number. With the increase of pulse interval from 500 ns to 20 μs, the PPF behavior changes to paired-pulse depression (PPD) (as shown in Figure 4c). Figure 4d shows the frequency-controlled transition from PPF to PPD.

Long-term plasticity, including long-term-potentiation (LTP), long-term depression (LTD), and spike-timing-dependent plasticity (STDP), which are essential function for the memory and learning of human brain, can also be emulated by Ag/SnS/Pt devices. Figure 4e shows the LTP and LTD process measured with identical voltage pulse sequence, which suffers from nonlinearity due to the abrupt switching of conductive filament devices.[27] This has been an intrinsic limitation in filament-based switching devices. A linear weight change is needed to achieve high accuracy in artificial neural network (ANN) implementation. Applying stepwise voltage pulses was reported to increase the linearity of the LTP and LTD processes in conductive filament devices.[28−30] As shown in Figure 4f, with application of a consecutive stepwise voltage pulse sequence consisting of 60 positive and 60 negative pulses, the device exhibits approximately linear conductance potentiation (LTP) and conductance depression (LTD) processes. STDP is an important biological process regulating connection strengths between synapses based on the relative timing of the pre- and postsynaptic spikes. The pre- and postspike are applied to the same device, as shown in Figure 4g. The time difference, Δt determines the conductance

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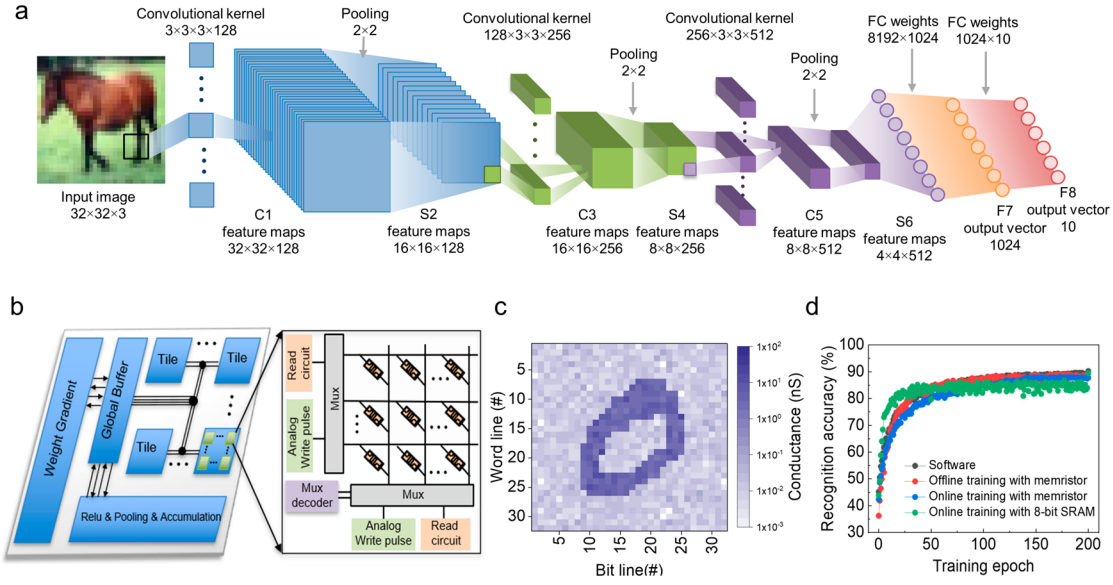

Figure 5. Chip-level implementation of DNN. (a) Architecture of 8 layers of VGG-8 convolutional neural network for CIFAR-10 image recognition. The horse image is reused with permission from ref 33. (b) Schematic diagram of hardware implementation for VGG-8 neural network. Left panel shows that the chip architecture contains tiles, global buffer, and functional peripheral circuits including pooling, accumulation, and activations. Inside tiles, it is further partitioned into multiple 32 × 32 subarrays with Ag/SnS/Pt synaptic devices at each cross-point. (c) Experimental demonstration of a handwritten digital code of "0" written in the fabricated 32 × 32 crossbar array. The code is written using write-verification scheme and conductance readout with 0.2 V. (d) Simulated classification accuracy results based on 8-bit SRAM and Ag/SnS/Pt devices for 10 categories of images such as dog, frog, truck, ship, and so on.

(weight) change of the Ag/SnS/Pt device. When $\Delta t > 0$, the appearance of prespike before postspike results in a positive voltage-dominated combined pulse (as plotted in the inset of Figure 4g), which gives a positive synaptic weight change, and vice versa for $\Delta t < 0$, obeying the asymmetric Hebbian learning rule.[31,32] The change of synaptic weight decreases with the increase of Δt magnitude and exhibits exponential dependence. Therefore, both short- and long-term synaptic plasticity behaviors could be well emulated using our Ag/SnS/Pt device. Importantly, synaptic plasticity was accomplished with a single Ag/SnS/Pt crossbar device without the help of additional supporting devices. As shown in Table S1, the performance of our Ag/SnS/Pt memristor is comparable to the best ones in the ion migration based RSM synaptic devices. However, unlike SnS, the metrics for the other materials are spread across different materials and seldom combined in one (see Table S2, Supporting Information). Therefore, SnS has great potential as materials hardware for neuromorphic computing.

We have demonstrated that our Ag/SnS/Pt memristive devices can mimic a series of essential synaptic behaviors with fast switching speed, small area, and high energy efficiency. It is also crucial to evaluate the chip-level performance using our Ag/SnS/Pt synaptic devices for hardware implementation of a deep neural network (DNN). An eight-layer convolutional neural network (CNN) was therefore built to recognize the CIFAR-10 images as shown in Figure 5a.[33,34] Based on the NeuroSim platform,[35,36] we did a chip-level simulation to evaluate the hardware performance of the CNN using our Ag/SnS/Pt memristive devices. Figure 5b depicts the chip architecture that contains a global buffer, peripheral functional circuits, and tiles, which can be further divided into multiple subarrays of 32 × 32. To verify the feasibility of mapping, a randomly chosen handwritten digital code "0" was successfully written on our fabricated 32 × 32 array with write-verification scheme in Figure 5c. The simulated recognition accuracy results of the ideal (software) and Ag/SnS/Pt memristive devices are summarized in Figure 5d. We investigated both online training (that is, both training and inference are done on chip) and offline training cases (that is, only inference is done on chip). The simulation of offline supervised learning using memristive devices and 32 nm node of CMOS technology achieves 89.3% recognition accuracy for 10 000 test images from the CIFAR-10 data set over 200 epochs, approaching the ideal software accuracy of 90.23%. Online training simulations based on Ag/SnS/Pt devices and 8-bit SRAM were also performed to give a high recognition rate of 87.76% and 89.5% after 200 epochs training with 50 000 images. Compared with the 8-bit SRAM based neuromorphic chip, it also shows 263% better energy efficiency and 4.3 times better performance density (see Methods and Tables S6 and S7).

CONCLUSION

We have fabricated a highly scalable memristor device based on Ag/SnS/Pt using SnS flake. The fast-switching speed of the SnS device combined with its low operation voltage allows for low power consumption. A wide range of synaptic plasticity behaviors, including PPF, PPD, LTP, LTD, and STDP, could be well emulated in SnS memristor devices based on the multilevel resistance states and the ability to operate in both volatile and nonvolatile modes. The chip-level simulation of a CNN on the CIFAR-10 data set reveals that the Ag/SnS/Pt device can achieve high recognition accuracy with great energy efficiency. The good performance is attributed to the low migration barrier of Ag^+ ions in SnS lattice due to presence of van der Waals gap and abundant Sn vacancies. The controllable conductive filament lifetime enables device engineering for nonvolatile memory for data storage and tunable short- and long-term memory for synaptic computing. Recently, Kwon et al. reported that wafer-scale SnS can be grown on arbitrary substrates,[37] which suggests that integration

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with silicon microelectronics may be achievable. Our findings suggest that p-type van der Waals semiconductors with cation vacancies exhibit great promise for electrochemical metallization type memory and neuromorphic devices.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.1c03169.

Methods and experimental details, $I-V$ characteristics for a total of 45 devices, control of the relaxation process with pulse magnitude, conductive AFM and in situ SEM data, computational methods and results, and comparison of the performance between reported data and this work (PDF)

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#X. F. L. and Y. Z. contributed equally. X. F. L. and Y. Z. conceived the research and wrote the initial draft. X. F. L. fabricated and tested the devices and analyzed the data. X. F. L., N. W., and W. B. G. conducted the ultrafast pulse measurement. Y. B. conducted the STM characterization and data analysis. X. F. L. and L. W. conducted the conductive AFM measurement. X. F. L. and Y. Z. perform the in situ SEM measurement. S. L. and G. L. performed the theoretical calculations. K. P. and X. H. C. grew the SnS crystal. X. F. L. and H. C. fabricated 32 × 32 arrays. Y. Z. conducted the CNN and DNN simulations. K. P. L. supervised the research and revised the manuscript with comments from all authors.

Notes

The authors declare no competing financial interest.

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