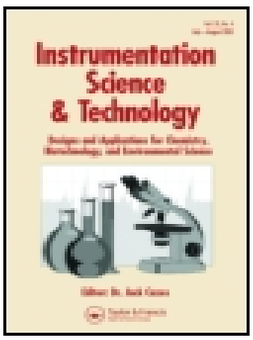

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Driving circuitry of a full-frame area array charge-coupled device (CCD) supporting multiple output modes and electronic image motion compensation

Hang Ren[a,b] and TaoTao Hu[c]

[a]Changchun Institute of Optics, Fine Mechanics and Physics, Chinese Academy of Sciences, Jilin, Changchun, China; [b]Changchun Institute of Optics, Fine Mechanics and Physics, Key Laboratory of Airborne Optical Imaging and Measurement, Chinese Academy of Sciences, Changchun; [c]School of Physics, Northeast Normal University, Changchun, China

ABSTRACT

In order to design a charge-coupled device (CCD) driving circuit with a high frame rate and a large area array which can support the electronic image motion compensation function, first a basic driving circuit of the large-array CCD is reported in this paper. Next, electronic image motion compensation is realized by adding an image motion compensation timing generator and a main timing generator, Saa8103. The internal design structure of the image motion compensation generator is provided and is characterized as follows. The data are first sent by the system controller, the main timing generator and the image motion compensation timing generator. The generator, the vertical driver, the horizontal driver and the full-frame charge-coupled device chip are then composed. During the exposure period, the image motion compensation transfer clock is generated by the image motion compensation timing generator, and the charge-coupled device charge packet is driven to track the image movement after being amplified by the vertical and horizontal drivers to carry out electronic image motion compensation in the vertical direction. During the output period, the vertical and horizontal rotations generated by the main timing generator are carried out by the image motion compensation timing generator. The shift clock is transmitted to the vertical and horizontal drivers to drive the charge-coupled device to produce the output. The phase relationship of the four corners of the charge-coupled device is independently controlled by the image motion compensation timing generator, which supports not only the electronic image motion compensation but also the flexible selection of the output channel number and output mode. A field-programable gate array (FPGA)/complex programable logic device (CPLD) has been selected to be the timing generator of image motion compensation, and timing simulation is carried out. Lastly, the design of the driving circuit was verified by an indoor image motion compensation experiment, and a good compensation effect has been achieved. In this system, the charge-coupled device adopts a separate driving technology, and the charge transfer direction of each block can be

KEYWORDS

Area array charge-coupled device (CCD); drive circuit; image motion compensation; timing-driven

CONTACT TaoTao Hu hutt262@nenu.edu.cn School of Physics, Northeast Normal University, No. 5268, People street, Changchun, Jilin, China.

established. Consequently, it is convenient to select the number of output channels and the output mode, which makes the camera suitable for different occasions, supports the charge-coupled device in terms of the output and electronic image motion compensation in various ways, and is capable of generating full-frame images. In order to meet the different requirements regarding the charge-coupled device frame frequency in different contexts, this proposed design overcomes the disadvantages of the complex structure and low reliability of traditional optical mechanical image motion compensation systems.

Introduction

Problem formulation

A high-frame-rate, large-area-array charge-coupled device (CCD) sensor is in high demand in the aerospace, digital photography, medical treatment, national defense, and high-resolution imaging fields. At home and abroad, high-frame-rate and high-resolution area array CCD ultrahigh-pixel digital cameras are used, there are many investigations in this very significant high demand area.[1]

A charge-coupled device is a type of sensor with mature technology and widespread applications. After more than 30 years of development, tens of millions or even hundreds of millions of pixels are utilized in ultrahigh-resolution large-area-array CCDs. In order to improve the image output rate, a large-area-array CCD often adopts a multioutput structure; that is, the CCD is divided into several blocks, and each block has independent drive signal input and output amplifiers, as adopted by the FTF series full-frame CCD of the Teledyne Dalsa.[2]

The charge-coupled device result is divided into four symmetrical images; each corner has an output amplifier, and the moving direction of the charge packet in each quadrant may be independently controlled to output in a variety of output modes and output channel numbers. When the charge-coupled device is used in low-speed situations, a single output is used to achieve better output consistency. When the charge-coupled device is used in high-speed situations, multiple outputs are used to achieve a higher output rate. Different output modes require different types of drive circuit support, and one drive circuit can meet only some needs. Therefore, there is a need to design many types of driving circuits to meet different application requirements with fewer designs and debugging cycles and with accompanying lower development costs.[3]

When a charge-coupled device aerial camera obtains an aerial photograph, due to the high speed of the aircraft, there is relative motion

between the camera and the target throughout the exposure time, which induces the image of the target on the focal plane to change, which induces image motion. Image motion results in the images of the objects to be aliased to each other, causing image degradation due to smearing of the objects with blurred edges, grayscale distortion, and reduced contrast and resolution.[1] For example, image motion may be separated into the forward image motion that is induced by the forward flight of the aircraft, the random image motion produced by variations in the attitude caused by pitch, yaw, and rolling of the aircraft, image motion due to various aircraft components that may include propellers and engine blocks, image motion due to camera platforms, vibrational image motion of the caused by the camera itself during its operation or impact, and vibrational image motion induced by fluctuations in the air flow. In a vertically photographed aerial image, the degree of the forward image motion is approximately one order of magnitude higher than all of the other types of image motion, and therefore the primary consideration with this type of camera is the compensation of the forward image motion.[4]

According to the compensation principles and the corresponding implementation methods, the internal model control image motion compensation (IMC) methods for the aerial camera hardware may be separated into four types: the mechanical image motion compensation method,[3] the optical image motion compensation method,[4] the electronic image motion compensation method, and the image-mode image motion compensation method.[5] Each method has its own characteristic advantages and limitations. The mechanical and optical image motion compensation methods require the use of complex and sophisticated optical and mechanical structures. Consequently, the complexity, volume, and weight of the camera are enhanced. The reliability of the camera is also reduced because of the presence of moving parts.

The image-mode image motion compensation method does not provide real-time results.[6] The advantage of the electronic IMC method lies in the use of the internal model control image motion compensation image motion compensation methods device itself. Because only the drive circuitry of the CCD requires modification; hence, a complicated optical system is not required which results in the simplification of the camera hardware. Therefore, the electronic method is often used in place of other IMC methods in an internal model control image motion compensation (IMC) method aerial camera.

Primary contributions of this article

Because the general traditional time sequence driving circuit of an area array charge-coupled device is designed with a special chip, taking the

Ftf5066m CCD driving circuit with a high frame rate and a large area array as an example, the traditional driving circuit uses a Saa8103 chip as the time sequence driving chip. However, SAA8103 has no on-chip central processing unit (CPU) and may only be controlled by an additional central processing unit. Generally, a microcontroller unit (MCU) is used.

Another method is to employ a FPGA instead of a Saa8103 chip. The combined single chip microcomputer may provide the whole driving circuit considerable versatility. However, if the driving circuit includes an image motion compensation function, the timing during the integration cannot be changed arbitrarily due to the use of a special timing generator (Saa8103) to generate a variety of timings. If an FPGA is used as the timing generator, the timing needed for image motion compensation integration can be generated. However, the hardware debugging is difficult.[7]

The technical problems that are resolved in this paper are as follows: (1) overcoming the shortcomings of the existing technology, (2) providing a full-frame CCD driving circuit that supports multiple output modes and electronic image motion compensation, (3) the development of the flexible selection of the CCD output mode and output channel number so that a driving circuit is able to meet the needs of multiple applications, (4) solving the problem of poor universality of a single driving circuit, and (5) realizing electronic image motion compensation. With the independent driving technology of quadrant grouping, the flexible selection of the charge-coupled device output mode and output channel number is realized, which can meet the requirements of the camera frame frequency in various applications and solves the problem of poor universality of a single driving circuit. At the same time, the electronic image motion compensation technology is performed by the use of an image motion compensation timing generator, which avoids the use of complex and precise optical structures and moving parts. Moreover, this approach overcomes the problem of the traditional optical mechanical image motion compensation camera whose disadvantages include a complex structure, large volume, heavy weight and low reliability, greatly enhancing development costs.

The structure of the paper is as follows. The Ftf5066m basic drive circuit is described, followed by structural characteristics and driving requirements of the Ftf5066m and the design of the Ftf5066m basic drive circuit. Next, we report the design of the driving circuit of a full-frame area array charge-coupled device that supports multiple output modes and an electronic image motion compensation function. The composition and overall design of the driving circuit is provided for a full-frame charge-coupled device supporting an image motion compensation function, followed by the introduction of the design of the image motion compensation sequence generator. The experimental results are presented, followed by a time-driven

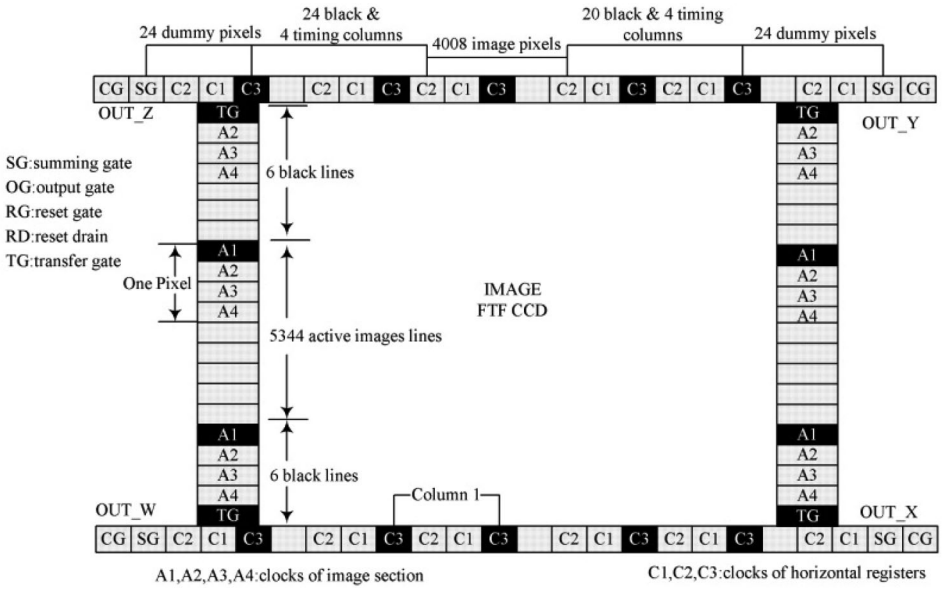

Figure 1. Internal structure diagram of the Ftf5066m.

simulation experiment. An image motion compensation imaging experiment is reported, followed by the actual imaging of the system reported in this paper. Lastly, conclusions regarding this study are provided.

Ftf5066m basic drive circuit

Structural characteristics and driving requirements of Ftf5066m

A Ftf5066m is a 22-million-pixel high-resolution, full-frame, large-area-array charge-coupled device image sensor with a vertical anti-halo structure. It has advantages such as a large area array (36 mm × 48 mm), high resolution (4992 × 6668), high fill factor (100%), large dynamic range (> 72 dB), fast pixel output speed (maximum 27 MHz), and high charge transfer efficiency (0.999999). The Ftf066m is very suitable for imaging by use of a scientific camera sensor, as shown in Figure 1.

The largest region of the chip is the photosensitive area, which adopts the four-phase electrode structure. Each pixel is composed of grids A1, A2, A3, and A4. There are six light-shielding lines at the upper and lower ends of the photosensitive area and 24 light-shielding columns at the left and right sides. There are horizontal output registers at the upper and lower ends of the chip, which adopt a three-phase electrode structure, and each pixel is composed of grids C1, C2, and C3. Between the horizontal output register and image area, there is a transfer gate (TG) that can be controlled independently. There is an output amplifier at both ends of each output register, adopting a floating diffusion output structure. In front of the

output amplifier is the output gate (OG) and the horizontal pixel merging gate (SG). The reset gate of the output amplifier is denoted by RG.

The most important feature of this device is that it has a four-quadrant symmetrical structure. The whole device may be regarded as being composed of four symmetrical parts, w, x, y and Z. Each section has a set of identical but independent driving clocks and bias voltage inputs. By changing the driving time sequence of each section, the signal charge of each quadrant may be transferred to different directions to realize flexible selection of the output channels and output modes. When a single output is used, the maximum frame rate is approximately 1 frame/second. When four channels are used for simultaneous output, the maximum frame rate may reach 3.6 frames/second.

The driving clocks of the Ftf5066m primarily include the following components: image area electrode driving clocks A1, A2, A3, A4 and TG; horizontal output register electrode driving clocks C1, C2, C3 and SG; the reset tube grid driving pulse RG and the full-frame reset pulse NSCR. The timing may be divided into frame transfer, row transfer and pixel transfer. The frame transfer timing is used to drive the charge-coupled device to complete the transfer output of a frame image, while the row transfer timing is used to drive the charge vertical transfer of a row in the charge-coupled device image area. The pixel transfer timing is used to drive the charge horizontal transfer of a pixel in the charge-coupled device horizontal output register.

The DC bias voltage includes the n substrate voltage VNS, P substrate voltage VPS, output amplifier voltage VSFD, reset transistor drain voltage VRD and output gate voltage VOG. Since the P substrate voltage is + 6 V, when the driving clock is 0 V, the electrode can be inverted, avoiding the use of a negative voltage for driving. The A1, A2, A3, A4 and TG drive clocks are 0 to 8 V during the optical integration period and 0 to 11 V during the charge transfer period for better output linearity. The C1, C2, and C3 drive clocks are 3 to 8 V, SG is 4.5 to 9.5 V, RG is 17 to 22 V, and NSCR is VNS-VPS + 5 V.

For optical integration, the mechanical shutter is opened. First, a positive-pulse NSCR is applied to the n substrate to realize full-frame reset as Ftf5066m has a vertical anti-halo structure. Next, a high level is applied to grids A2 and A3 and a low level is applied to A1/TG so that the photogenerated charge is collected into the potential well below A2 and A3. The optical integration time is from the end of the NSCR to the time when the shutter is completely closed.

After the end of optical integration, the charge-coupled device enters the stage of charge transfer output, alternating between vertical row transfer and horizontal pixel transfer. When vertical row transfer occurs, A1, A2,

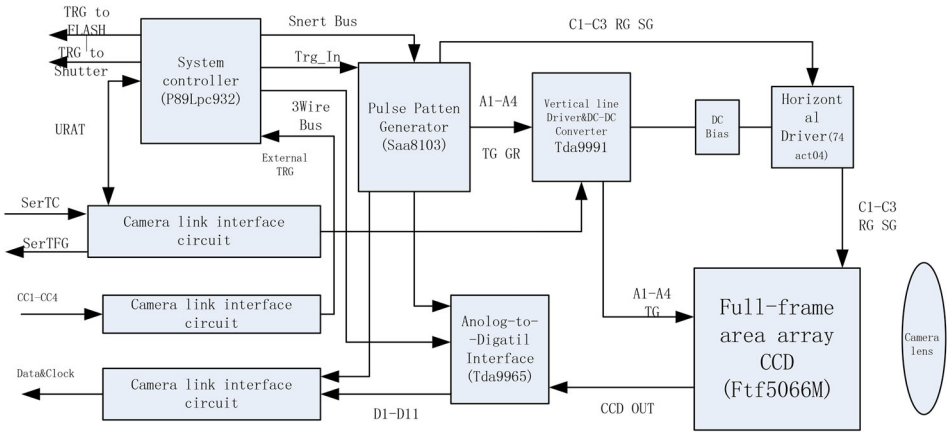

Figure 2. Ftf5066m basic drive circuit.

A3, A4 and TG overlap. When horizontal pixel transfer occurs, C1, C2, C3 and SG overlap. RG removes the charge on the detection gate before each charge packet is injected into the detection gate. After all of the charges are output, the charge-coupled device enters the idle stage and waits for the next frame to be collected.[5]

Design of the Ftf5066m basic drive circuit

For the Ftf5066m to work normally and optimize its performance, the design of the charge-coupled device driving circuit system becomes a key issue. Because the peripheral chip of the CCD is relatively mature, this device may greatly reduce the circuit complexity and cause the system to have a simple structure, high reliability, and excellent performance.

Figure 2 shows the basic driving circuit block diagram of the Ftf5066m circuit system, which consists of a vertical driver used to improve the vertical driving ability, a horizontal driver used to generate the charge-coupled device DC bias voltage and horizontal driving level, a DC bias circuit, front-end signal processing employed for black level clamp compensation, amplification, related double sampling and analog-to-digital conversion, and a system controller. Lastly, the image is transmitted to a personal computer through an image acquisition card.[6,8]

The timing pulse generator generates various types of timing pulse signals required by the system. The vertical driver amplifies the vertical transfer timing to the driving level signal with sufficient voltage and current driving ability and generates the main DC bias voltage required by the charge-coupled device. The horizontal driver amplifies the horizontal transfer timing to the driving level signal that meets the working requirements of the charge-coupled device.

The DC bias circuit drives the vertical drive. The main DC bias voltage generated by the actuator is divided to generate the other DC bias voltages required by the charge-coupled device.[9,10] The front-end signal processor carries out relevant double sampling, controllable gain amplification, dark level clamping compensation and analog-to-digital conversion of the analog signal output by the charge-coupled device. The camera link interface circuit is responsible for outputting the digital image signal generated by the analog-to-digital converter from the upper camera and providing it to the upper level. This process may be achieved by the Saa8103 or a programable logic controller (PLC). The system controller is realized by the MCU.[11,12]

Design of the driving circuit of a full-frame area array charge-coupled device that supports multiple output modes and an electronic image motion compensation function

Composition and overall design of the driving circuit for the full-frame charge-coupled device that supports the image motion compensation function

The technical problems to be solved in this paper include overcoming the shortcomings of the existing technology, providing a full-frame charge-coupled device driving circuit that supports multiple output modes and electronic image motion compensation, realizing the flexible selection of the charge-coupled device output mode and output channel number so that the driving circuit can meet the needs of multiple applications, solving the problem of poor universality of a single driving circuit, and realizing electronic image motion compensation.[13,14]

To develop the driving circuit of a full-frame charge-coupled device supporting image motion compensation, here is reported a charge-coupled device driving circuit structure called a double time sequence generator, which is based on the improved designed driving circuit. The system is composed of an image motion compensation sequence generator and the main sequence generator SAA8103 to realize electronic image motion compensation. The driving sequence generation method is shown in Figure 2, and its static product is shown in Figure 2. All of the time sequences are generated by Saa8103. The FPGA/CPLD is responsible for forwarding, while the vertical transfer time sequence in the image motion compensation integration time sequence is generated by the FPGA/CPLD, and other time sequences are generated by the Saa8103. The diagram of the driving time sequence is shown in Figure 3.[15,16]

In Figure 3, A1, A2, A3, and A4 are the vertical transfer drive clocks, VA high is the high-level transfer clock, and TG is the transfer clock. The CR

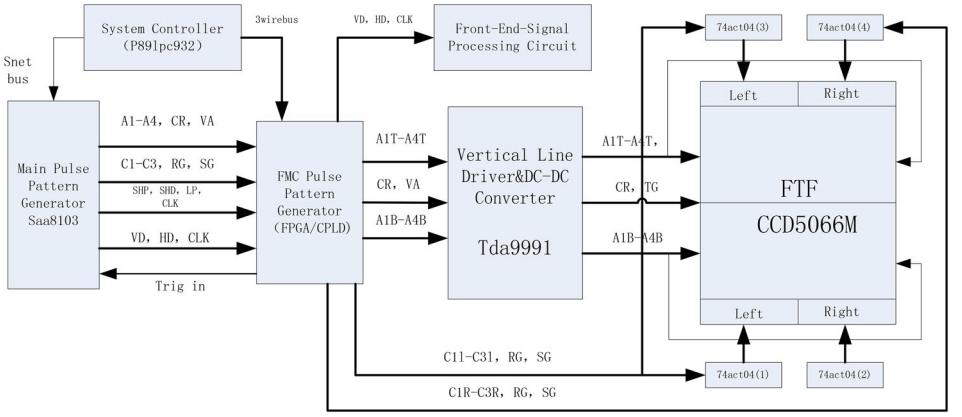

Figure 3. Structure of the driving circuit of the full-frame charge-coupled device supporting the image motion compensation function.

signal is the charge reset signal of the charge-coupled device photosensitive area whose function is to remove the residual charge of the charge-coupled device photosensitive area before integration starts. C1, C2, and C3 are the horizontal transfer drive clocks. RG, SG, SHP, SHD, and LP are high-frequency timing pulses closely related to the horizontal pixel shift.

CLK is the pixel clock. HD is the line clock signal. VD is the frame clock signal. The trigger in is the external trigger signal. RG is the output amplifier reset pulse, and SG is the horizontal pixel merge gate drive clock. As mentioned above, VNS is the voltage applied to the charge-coupled device n-type substrate, VPS is the voltage applied to the p-type substrate of the CCD, VSFD is the DC voltage applied to the CCD output amplifier, VRD is the voltage applied to the drain of the reset transistor of the CCD output amplifier, and VOG is the electricity added to the CCD OG.

A full-frame charge-coupled device driving circuit supporting multiple output modes and electronic image motion compensation is composed of a system controller, main timing generator, image motion compensation timing generator, vertical driver, full-frame charge-coupled device chip, horizontal driver 1, horizontal driver 2, horizontal driver 3, and horizontal driver 4 (Figure 4). The control bus output terminal of the system controller is composed of a main timing generator and an image motion compensation timing generator. The control bus inputs of the generator and the vertical driver are connected.

The horizontal transfer clock, the vertical transfer clock and the signal processing clock outputs of the main timing generator are connected to the horizontal transfer clock, the vertical transfer clock and the signal processing clock inputs of the image motion compensation timing generator, respectively. The upper and lower vertical transfer clock outputs of the image motion compensation timing generator are connected to the vertical

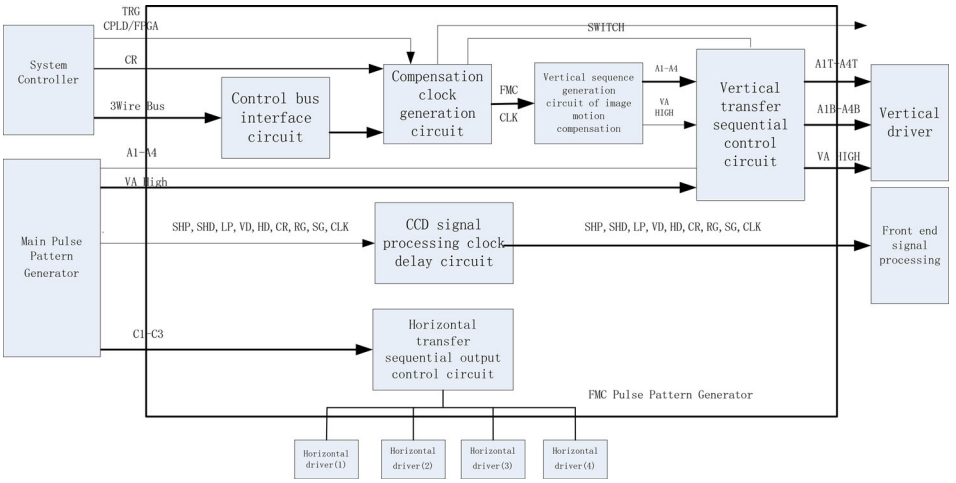

Figure 4. Internal function block diagram of the image motion compensation sequence generator.

transfer clock outputs. The upper and lower vertical transfer clock input terminals of the direct drive are connected, while the left horizontal transfer clock output terminal of the image motion compensation timing generator is connected to the horizontal transfer clock input terminals of horizontal driver 1 and horizontal driver 4. The right horizontal transfer clock output terminal of the image motion compensation timing generator is connected to the horizontal transfer clock input terminals of horizontal driver 2 and horizontal driver 3.

The upper vertical driver output terminal of the vertical driver is connected to the upper-left and upper-right vertical driver input terminals of the full-frame charge-coupled device chip, the lower vertical driver output terminal of the vertical driver is connected to the lower-left and lower-right vertical driver input terminals of the full-frame CCD chip; and horizontal driver 2, horizontal driver 3, and horizontal driver 4 are connected to horizontal driver 1. The moving level output terminal is connected to the lower-left, lower-right, upper-right and upper-left driver input terminals of the full-frame charge-coupled device chip, and the resulting signal processing clock of the image motion compensation timing generator is output to the signal processing circuit.[17,18]

The system controller controls all sections of the system through the control bus to coordinate the operation. When collecting data, the charge-coupled device first enters the exposure state. At this time, the camera shutter is opened. The image motion compensation timing generator produces a vertical transfer clock at specific instances according to the image motion speed information from the control bus output end of the system controller. The clock is amplified by the vertical driver into the charge-coupled device vertical transfer level drive C.

At the same time, the image motion compensation timing generator transmits the horizontal transfer clock generated by the main timing generator to horizontal driver 1, horizontal driver 2, horizontal driver 3, and horizontal driver 4 to drive the charge-coupled device to release the vertical image motion compensation when transferring. After the exposure period, the charge-coupled device enters the continuous output state, and the camera shutter is closed. The image motion compensation timing generator forwards the output vertical and horizontal transfer clocks generated by the main timing generator to the vertical driver and horizontal driver 1, horizontal driver 2, horizontal driver 3, and horizontal driver 4 to drive the charge-coupled device for charge output and the image motion compensation timing generator at the same time. The signal processing clock generated by the main timing generator is transmitted to the signal processing circuit for amplification, correlated double sampling, analog-to-digital conversion and output processing of the charge-coupled device output signal.[19,20]

The driving circuit of the full-frame charge-coupled device supporting multiple output modes and electronic image motion compensation is characterized as follows. The upper-left and upper-right vertical transfer level input terminals of full-frame charge-coupled device chip 5 are divided into one group, while the lower-left and lower-right vertical transfer level input terminals are divided into a second group, the upper-left and lower-left horizontal transfer level input terminals are divided into a third group, and the upper-right and lower-right horizontal transfer level input terminals are divided into a fourth group. The terminal is divided into groups; each group is driven independently so that the moving direction of each quadrant charge packet may be controlled, and the various output modes may be selected flexibly.

The system controller is P89lv51rd2, the main timing generator is Saa8103, the image motion compensation timing generator is the CPLD device Xc95144xl, the vertical driver is Tda9991, the full-frame charge-coupled device chip is Ftf2200m/3020m/4021m/4052m/5033m/5066m/6146m, and 74act04 is selected for horizontal driver 1, horizontal driver 2, horizontal driver 3, and horizontal driver 4.[21,22]

Design of the image motion compensation sequence generator

The image motion compensation timing generator is an FPGA/CPLD device, which consists of a control bus interface circuit, a compensation clock generation circuit, an image motion compensation vertical transfer timing generation circuit, a vertical transfer timing output control circuit, a horizontal transfer timing output control circuit, a charge-coupled device signal processing clock delay circuit, a control bus input end of the control bus interface circuit and a system controller. The control bus input end of

the control bus interface circuit is connected to the control bus output end of the system controller, while the parameter output terminal of the control bus interface circuit is connected to the parameter input terminal of the compensation clock generation circuit. The timing signal output terminal of the compensation clock generation circuit is connected to the timing signal input terminal of the image motion compensation vertical transfer timing generation circuit, while the selection signal output terminal of the compensation clock generation circuit is connected to the selection signal output of the vertical transfer timing output control circuit.

The vertical transfer clock input terminal 1 and vertical transfer clock input terminal 2 of the vertical transfer timing output control circuit are connected to the vertical transfer clock output terminal of the image motion compensation vertical transfer timing generation circuit and the vertical transfer clock output terminal of the main timing generator, respectively.[23,24] The upper and lower vertical transfer clock output terminals of the vertical transfer timing output control circuit are connected to the vertical transfer clock output terminal. The upper and lower vertical transfer clock input terminals of the driver are connected, with the left horizontal transfer clock output terminal of the horizontal transfer timing output control circuit connected to the horizontal transfer clock input terminals of horizontal driver 1 and horizontal driver 4, and the right horizontal transfer clock output terminal of horizontal transfer timing output control circuit 3 connected to the horizontal transfer of horizontal driver 2 and horizontal driver 3. The clock input is connected, and the charge-coupled device signal processing clock of the charge-coupled device signal processing clock delay circuit is output to the signal processing circuit.[25,26]

The division and functions of each section are as follows:

1. The control bus interface circuit provides a three-wire bus interface to receive the time interval information of image motion compensation from the system controller (timer setting).
2. During the exposure period, the compensation clock generation circuit generates a timing pulse with an interval of W/4 V according to the time interval information (timer setting), and a trigger signal and a timing switch signal (Saa8103) are generated according to the operational state.
3. The vertical sequence generation circuit of image motion compensation generates the image motion compensation driving sequence according to the timing pulse (A1, A2, A3, A4 and VA high signals).
4. The vertical transfer sequential control circuit selects the A1, A2, A3, A4 and VA high signals generated by the FMC V clock generator during exposure; selects the A1, A2, A3, A4 and VA high signals generated

by SAA8103 during the charge output and idle period; allocates the A1, A2, A3, A4 signals to A1T, A2T, A3T, and A4T and A1B, A2B, A3B, and A4B, and controls the phase relationship for each channel during the distribution process.[1–4,7]

5. The CCD signal processing clock delay circuit allocates the horizontal transfer sequence C1, C2, and C3 generated by SAA8103 into two channels, C1L, C2L, C3L and C1R, C2R, C3R, and controls the phase relationship of each channel in the allocation process.
6. The horizontal transfer sequential output control circuit forwards other sequential signals generated by the Saa8103.

According to the light integration start stop trigger signal of the TRG CPLD signal, the timing and control module is able to judge the start and end times of exposure to generate the corresponding timing pulse and control signal and make the whole timing generator work normally. The timing pulse is generated by counting the CPLD master clock by the counter, while the vertical transfer timing module is designed by the waveform subdivision method.

Advantages and disadvantages of the system

Notably, since the exposure time is arbitrary, the A1, A2, A3, A4 termination waveform may be in any possible state at the end of exposure, as shown at time T1 in the corresponding figure. If it is different from the waveform state at the end of Saa8103 exposure (A1 = 0, A2 and A3 = 1), the A1, A2, A3, A4 timing will suddenly jump after switching as shown at time T2 in Figure 5 so that it does not meet the overlapping principles of the charge-coupled device driving clock. It is possible to cause the charge packets of two adjacent lines to overlap, which greatly reduces the vertical resolution.

The approach to solve the time sequence jump before and after switching is to characterize the waveform state of A1, A2, A3, and A4 at the end of exposure. If the conditions of A1 = 0 and A2 and A3 = 1 are not met, the transfer driving time sequence, as shown in the gray interval in Figure 5b,

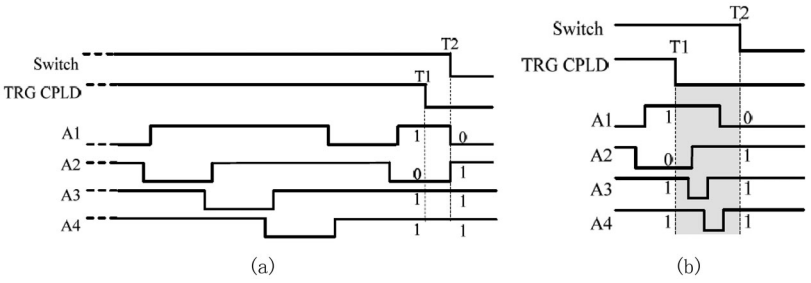

Figure 5. Schematic of the A1, A2, A3, A4 timing switching problem. (a) A sudden jump in A1-A4 sequence (b) The method of solving time sequence jump

is quickly generated several times until the condition is met, and then switching will be carried out as shown at T2 in Figure 5b. By the use of this approach, the A1, A2, A3, and A4 time sequence before and after switching naturally meets the charge-coupled device driver requirements.[27]

With the independent driving technology of quadrant grouping, the flexible selection of the charge-coupled device output mode and output channel number is realized, which can meet the requirements of the camera frame frequency in various applications and solve the problem of poor universality of a single driving circuit. At the same time, electronic image motion compensation technology is realized by using an image motion compensation timing generator, which avoids the use of complex and precise optical structures and moving parts and overcomes the problem of the traditional optical mechanical image motion compensation camera, which has the disadvantages of a complex structure, large volume, heavy weight and low reliability, greatly reducing the development cost.

In this system, the image motion compensation speed is set by the external controller, and an additional control system is needed. A process to obtain real-time image motion speed information and carry out automatic control actively is a problem that requires further study.

When the charge-coupled device uses four output channels, the output image has an obvious seam or strip effect, which is caused by the inconsistency of transmission characteristics between output channels, which is called channel nonuniformity. There are many factors that cause the nonuniformity of the output channel. The most important is that the on-chip amplifier and the off chip emitter triode of each channel have different gain, offset and nonlinear characteristics. These differences make the output channel somewhat asymmetrical. In this way, when uniform light is used to irradiate the entire charge-coupled device, the average gray value of the image obtained in each output channel is also different. To eliminate this type of joint, the nonuniformity between channels needs to be corrected.

Experimental measurements

Time-driven simulation experiments

Electronic image motion compensation is realized by modifying the vertical transfer driving clock during charge-coupled device optical integration. When the charge-coupled device performs normal optical integration, the driving clock of each electrode in the photosensitive region remains unchanged. Figure 6 shows the time of vertical transfer clock during exposure when ftf5066m performs traditional electronic image shift compensation Sequence diagram, wherein shut is the trigger signal of shutter, when it is high current, the shutter is opened; A1–A4, TG, VA high are the high

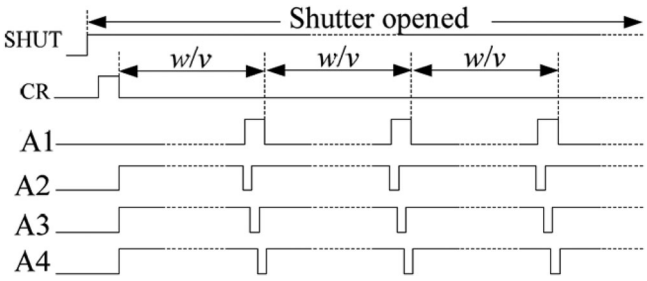

Figure 6. Driving time sequence of vertical transfer during electronic image motion compensation exposure.

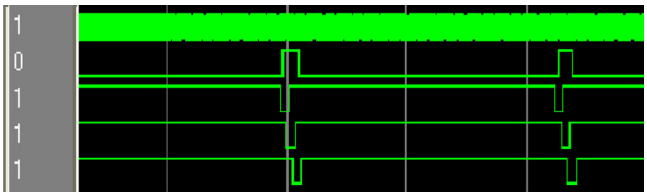

Figure 7. Waveform simulation of the vertical transfer sequence diagram.

level control signals of vertical transfer drive clock and transfer clock. During the exposure period, the driving clocks A1–A4 drive the charge packet to transfer in behavioral steps according to the image moving speed, and track the image moving; after each transfer, the horizontal transfer drives the charge in the output register to read out. After the exposure, it works according to the normal reading sequence. However, when electronic image motion compensation is performed, the driving clock is changed at certain points in time, and the driving electric bag is transferred along the image motion direction. The time interval is calculated by the following relationship:[28]

$$\Delta t = \frac{w}{v_{FM}}$$

where w is the pixel size in the column direction (mm), and v_{FM} is the image speed (mm/s).

The sequence diagram after the system simulation of the program is shown in Figure 7. The simulation results of the image motion compensation timing software Modelsim are shown in this figure, and the timing meets the requirements. After downloading the program to the FPGA through the Modelsim software, the wave simulation diagram of vertical transfer and horizontal transfer and the driving sequence diagram meet the imaging requirements.[29]

After the completion of software debugging and simulation, the designed software driver was downloaded to the main control chip for the characterization of the driving system. At the beginning of the measurement, an

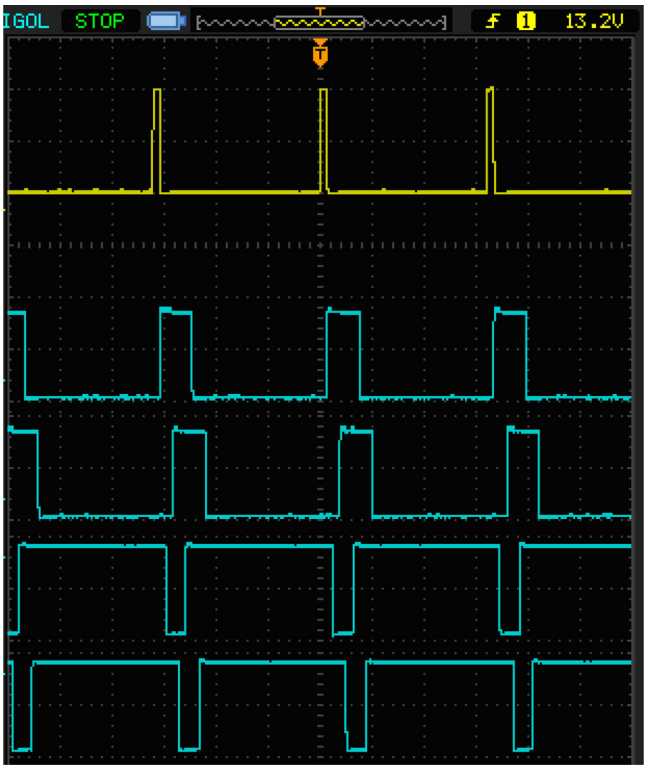

Figure 8. Vertical transfer timing and simulation waveform diagram.

oscilloscope was used to observe the signal output of the circuit to determine whether the function of the circuit and the software program were designed correctly. Figure 8 shows the subsignal and vertical driver pulse output observed by the oscilloscope, which meet the vertical transfer drive timing, demonstrating the feasibility of the drive circuit reported in this paper.[30]

Image motion compensation imaging measurements

Comparison of the effects of different image motion compensation methods

To verify the feasibility of the image motion compensation method, compensation experiments were carried out. In these measurements, a camera with a focal length of 80 mm was used to provide a high-definition image of the Water Cube of the Bird's Nest at rest. The letters and a torch were selected from the high-definition image as the specified experimental objects.

The input image is the initial estimate of the point spread function, and the restored image is the final estimate of the function. Through the application function of the blind deconvolution method mentioned above, the software compensation is programed with Matlab. The compensation results are shown in Table 1.

Table 1. Comparison of the results of the software compensation methods.

Target	Stillness	Exercise (uncompensated)	Software (after compensation)	Mechanical method (after compensation)	Optical method (after compensation)	Electronic method (after compensation)
Letter						
Torch						

Table 2. Number of pixels in the charge-coupled device target of the image formed by the letter B in Table 2 (unit: number).

Target	Stillness	Exercise (uncompensated)	Software (after compensation)	Mechanical method (after compensation)	Optical method (after compensation)	Electronic method (after compensation)
Letter	2160	3050	2598	2520	2430	2340

Taking letter B as an example, the pixel values of letter B in three cases are calculated by importing images into Envi software, and whether the compensated image motion residual satisfies the requirement of image motion compensation (less than 1/3 pixels) is shown in Table 2.

Table 2 shows that the number of image pixels following mechanical compensation is 360 pixels greater than for the still image, so the compensation ratio is approximately 1/7. Similarly, the software compensation method adds 438 pixels compared with the still image, thereby accounting for approximately 1/6 of the number of pixels in the still image. The optical method compensation method adds 270 pixels, which accounts for approximately 1/8 of the number of pixels in the still image. The electronic method compensation method adds 270 pixels, which accounts for approximately 1/12.5 of the number of pixels in the still image.

The results of the above four methods indicate that the electronic compensation method is superior to the other compensation methods.

The image quality evaluation is primarily divided into subjective quality evaluation and objective quality evaluation. This paper carries out objective quality evaluation and evaluates the image by calculating the clarity of the image.

Image sharpness refers to the obvious difference in the gray value near the edge of the image or the two sides of the shadow line, that is, the gray change rate is large. The image sharpness represents the relative clarity of the image. Usually, the sharper the image, the clearer the image. The definition for the clarity of the image is as follows:

$$GMG = \frac{1}{(M-1)(N-1)} \sum_{i=1}^{M-1} \sum_{j=1}^{N-1} \sqrt{\frac{\left[g(i,j+1) - g(i,j)\right]^2 + \left[g(i+1,j) - g(i,j)\right]^2}{2}}$$

where $g(i,j)$ is the gray value of the first row and j column of the image and M and N are the total numbers of rows and columns of the image, respectively.

In the Matlab environment, the principal formula is used to calculate the image sharpness. The comparison results in Table 3 show that the sharpness value after electronic compensation is higher than those obtained by the use of other compensation methods. Therefore, the image following

Table 3. Image sharpness evaluation results of two compensation methods.

Target	Before compensation	After mechanical method compensation	After software compensation	After optical compensation	After electronic compensation
Torch	0.8263	1.6020	1.5151	1.6728	1.7212
Letter	1.1713	1.9106	1.9017	1.9213	1.9315

Figure 9. Diagram of the experimental verification device.

electronic compensation is clearer than those obtained with the other compensation methods.

Actual imaging of the system reported in this paper

The driving circuit of the charge-coupled device is simulated and photographed. The experimental device consists of a charge-coupled device camera, a three-axis swing table and a personal computer. As shown in Figure 9, the charge-coupled device camera is composed of the designed driving circuit system plus an adjustable lens. The computer is used to control the camera for shooting, to change the rotation speed of the motor and to send the rotation speed information to the camera. The computer was equipped with the CAMRA link image acquisition card to collect the captured images. The focal length of the camera is 90 mm, and the pixel size of the area array charge-coupled device camera is 9 μm.

The charge-coupled device driving circuit is connected to the personal and operates through Rs232 interface control. The image acquisition card is responsible for collecting the images, and the camera circuit generates the image motion compensation timing signal. The serial port software is compiled by Microsoft Visual C++ software to collect the images, and the data collected from the images are analyzed by Matlab.[31,32]

Figure 10. Comparison of image motion compensation experimental photographs: (a) without image motion compensation and (b) with image motion compensation.

According to the above design scheme, the schematic diagram and printed circuit board (PCB) design of the circuit system are generated so that the actual circuit debugging is completed. The designed system operates normally, is stable and reliable, and has been shown to obtain clear images. When the exposure time is 10 ms, the frame rate reaches 3.4 f/s. The camera was installed, placed era horizontally, on the three-axis swing platform and rotated the pitch axis at a constant of 5°/s to simulate the forward flight of an aircraft, wherein the line transfer frequency of the charge-coupled device was equal to 872 Hz.

The forward image compensation was performed by controlling the charge-coupled device transfer frequency, as shown in Figure 10.[33,34] The left image was obtained without image motion compensation, and the right was collected with image motion compensation. The image motion is effectively eliminated, which demonstrates the effectiveness of this system.[35]

Based on the basic driving circuit of the CCD Ftf5066m array, this paper proposes a charge-coupled device driving circuit structure called a double time sequence generator and designs its image motion compensation generator using an FPGA as the core of image motion compensation to realize the driving circuit of a full-frame CCD supporting image motion compensation. At the end of this work, a simulation was carried out, and a specific experiment is presented. The experiment shows that the method has favorable compensation properties.

The double time sequence generator structure is able to make full use of the hardware resources of the original time sequence generator of the system and retain the advantages of the original circuit technology that include its maturity, stability, reliability, and convenience in debugging, to

the greatest extent. The added time sequence generator of image motion compensation is only used during the exposure period. Several vertical transfer driving timings and transmitting timing signals generated by Saa8103 are needed; thus, the development difficulty is relatively low. With the redesigned timing generator, the development difficulty is greatly reduced and the development cycle is shortened.

The designed circuit system adopts block-independent driving technology. Moreover, the charge transfer direction of each block may be established. Thus, it is convenient to select the number and output mode of the output channels. When the charge-coupled device is used in a low-speed situation, a single output is used to achieve better output consistency. On the other hand, when the charge-coupled device is used in a high-speed situation, a multichannel output is used to achieve a higher output rate.

The method described in this paper supports the charge-coupled device output and electronic image motion compensation in many ways. These approaches are able to meet the different requirements of the charge-coupled device frame frequency for different scenarios and overcome the disadvantages of traditional optical mechanical image motion compensation that include a complex structure and low reliability. We compared the effects of different image motion compensation methods.

The results from the four methods indicate that the electronic compensation method is superior to the other compensation approaches.[36,37] Here is provided the actual imaging effect of the system designed in this paper. The image motion is effectively eliminated, which demonstrates the effectiveness of this system.

An actual flight verification of electronic image motion compensation and the realization of automatic compensation have been achieved.[38] Due to the limitations of experimental conditions, only the electronic image motion compensation method and the designed hardware circuit have been used. The indoor experiment results indicate good compensation. However, the compensation effect for the actual flight shooting has yet to be verified. In the system, the image motion compensation speed is set by the external controller, and an additional control system is needed. The method to obtain real-time image motion speed information and carry out automatic control actively is a problem that needs further study.

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