Journal of Alloys and Compounds 814 (2020) 152293

Contents lists available at ScienceDirect

Journal of Alloys and Compounds

journal homepage: http://www.elsevier.com/locate/jalcom

# Analysis of the back-barrier effect in AlGaN/GaN high electron mobility transistor on free-standing GaN substrates

Xinke Liu [a], Hao-Yu Wang [b], Hsien-Chin Chiu [b, c, d, *], Yuxuan Chen [a], Dabing Li [a], Chong-Rong Huang [b], Hsuan-Ling Kao [b, d], Hao-Chung Kuo [e], Sung-Wen Huang Chen [e]

[a] State Key Laboratory of Luminescence and Applications, Changchun Institute of Optics, Fine Mechanics and Physics, Chinese Academy of Sciences, Changchun, 130033, People's Republic of China

[b] Department of Electronics Engineering, Chang Gung University, Taoyuan, 333, Taiwan

[c] Departments of Radiation Oncology, Chang Gung Memorial Hospital, Taoyuan, 333, Taiwan

[d] The College of Engineering, Ming Chi University of Technology, Taishan, 243, Taiwan

[e] Photonic and Institute of Electro-Optical Engineering, National Chiao Tung University, Hsinchu, 300, Taiwan

A R T I C L E I N F O

*Article history:*
Received 19 March 2019
Received in revised form
8 September 2019
Accepted 13 September 2019
Available online 14 September 2019

*Keywords:*
GaN on GaN
Microwave
HEMT
Back barrier
Raman

A B S T R A C T

The effect of AlGaN back-barrier on AlGaN/GaN high electron mobility transistors (HEMTs) using free-standing GaN wafer has been investigated in this work. With the introducing back-barrier structure, the leakage path underneath the buffer (native nitrogen-vacancies and $GaO_x$ compounds of the HVPE-grown free-standing GaN surface) layer can be suppressed by lift-up the conduction band. As compared with AlGaN/GaN HEMTs on SiC wafer, AlGaN/GaN HEMTs on free-standing GaN wafer show enhanced drain current (700 mA/mm), improved transconductance (143 mS/mm), less current collapse (12%), higher current gain cut-off frequency (13 GHz), and maximum stable gain cut-off frequency (24 GHz), which is attributed to the higher epi quality layer on free-standing GaN wafer.

© 2019 Elsevier B.V. All rights reserved.

## 1. Introduction

In recent years, GaN-based high electron mobility transistors (HEMTs) have been comprehensively demonstrated and adopted as high-frequency power amplifiers in long-distance and high output power communication applications, such as macro-cell base-station (BS) and radars infrastructure. It is also expected to be widely used in millimeter-wave wireless communications for the macro-cell and micro-cell BS of fifth-generation mobile communications (5G). For 5G communication systems, a higher peak power density is required for the power amplifiers (PAs), since the back-off operation from the peak power of PAs was generally used to increase their linearity [1–3]. However, the dominated substrate material for traditional GaN high electron mobility transistor (HEMT) epitaxy is silicon carbide (SiC). The 3.5% lattice mismatch between GaN and SiC is relatively small but still leads to a considerable source of lattice defects caused by the threading dislocations and these defects also result in the traps inducing nonlinearity during high power operation. If huge amount of the traps were found in the buffer region, they end up suppressing the density of two dimensional electron gas (2-DEG), thereby increasing the dynamic on-resistance [4,5].

In the past several years, ammonothermal-grown or hydride vapor phase epitaxy (HVPE)-grown free-standing semi-insulating GaN bulks, with a low threading dislocation density ($TDD < 10^6$ $cm^{-2}$), provided a highly potential method to demonstrate high reliability AlGaN/GaN microwave HEMT on latticed matched GaN substrates [6,7]. Based on the industrial production point of view, HVPE-grown GaN bulk exhibits a higher growth rate and high volume production ability. However, huge amount of the native nitrogen-vacancies and $GaO_x$ compounds, or surface Si contamination of the HVPE-grown free-standing GaN substrate formed a trapping center beneath the buffer for HEMT structure and this trapping center storages the spillover electron of 2-DEG at high current and high voltage operation. In this study, the $Al_{0.08}Ga_{0.92}N$ back-barrier was first employed and investigated in AlGaN/GaN HEMT on free-standing HVPE GaN substrates to minimize the device interface traps and thermal effects.

* Corresponding author. Department of Electronics Engineering, Chang Gung University, Taoyuan, 333, Taiwan.hcchiu@mail.cgu.edu.tw

https://doi.org/10.1016/j.jallcom.2019.152293
0925-8388/© 2019 Elsevier B.V. All rights reserved.

## 2. Experiment details

Fig. 1(a) displays the layer structure of in-situ $SiN_x$/AlGaN/AlN/GaN HEMT with AlGaN back barrier design on a 2-inch semi-insulating Fe-doped free-standing GaN substrate (350 μm thick) with (0001) orientation, and the wafer was grown by HVPE method. The epitaxial layers were grown by metal organic chemical vapor deposition, starting with a thin AlN nucleation layer and a highly Fe-doped GaN buffer where Fe ions act as the deep acceptor above the midgap to minimize the parasitic channel effect caused by native nitrogen-vacancies and $GaO_x$ compounds or the Si contamination layer of GaN bulk surface. In addition, recent study [8] also indicated that the high resistivity GaN substrate was found a pit halo structure revealing the leakage current path in V-shaped pits. The resistance in a pit halo edge is much lower than that in the normal area, resulting in a leakage current path [9]. Therefore, the back barrier and Fe-doped GaN buffer designs were proposed in this study. Above the AlN nucleation and Fe-doped buffer layer, the vertical structure of the wafer consists of a 3- μm-thick buffer layer, a 50-nm $Al_{0.08}Ga_{0.92}N$ back barrier, 500-nm GaN layer, 1-nm AlN spacer layer, and an 18-nm $Al_{0.24}GaN$ barrier layer. In order to avoid the oxidation of AlGaN barrier layer, the wafer was passivated by a 3 nm in-situ $SiN_x$ layer in the MOCVD and this thin $SiN_x$ was also adopted as gate insulator. The identical structure was also grown on a 2-inch 4H–SiC substrate for electrical characteristic comparisons. The 2-DEG sheet charge density and mobility for both wafers were determined using the Hall effect measurement. Room temperature (RT) Hall measurements revealed a 2-DEG density of $9.1 \times 10^{12}/cm^2$ and a mobility of 1524 $cm^2/V \cdot s$, corresponding to a sheet resistance of 310 Ω/□ for GaN on GaN device and these values were $9.82 \times 10^{12}/cm^2$, 1676 $cm^2/V \cdot s$, 292 Ω/□ for GaN on SiC device, respectively. Fig. 1 (b) shows a band diagram for the in-situ $SiN_x$/AlGaN/AlN/GaN HEMT with AlGaN back barrier calculated using a self-consistent one-dimensional Schrödinger–Poisson equation solver. A deep 2-DEG channel was formed by $Al_{0.24}Ga_{0.76}N$/AlN/GaN heterostructure for high sheet charge density and high carrier confinement consideration. The AlN spacer layer was designed to further improve channel mobility and to suppress channel-to-gate leakage current under high input power swing. The thicknesses of the $Al_{0.08}Ga_{0.92}N$ back barrier is 50 nm and an obvious raise of band diagram to minimize the carrier injecting into buffer layer at high drain voltage. In addition, low Al mole fraction of $Al_{0.08}Ga_{0.92}N$ back barrier also avoid back barrier induced sub-channel effect and disorder scattering between GaN channel/$Al_{0.08}Ga_{0.92}N$ back barrier. Fig. 1 (c) and (d) show the transmission electron microscopy (TEM) image and Fast Fourier transform (FFT) image of $Al_{0.08}Ga_{0.92}N$ back barrier layer, respectively. Based on the clear crystal structure of TEM and FFT diffractogram, high single crystalline quality of the epitaxial AlGaN back barrier layer is obtained, and no phase separation of AlN and GaN is observed [10–12].

Device fabrication began with mesa isolation of the active HEMT areas through a reactive ion etcher by using a gas mixture of $BCl_3$, $Cl_2$, and Ar. Then, ohmic contacts were prepared by the electron beam evaporation of a multilayered Ti/Al/Ni/Au (30/125/50/200 nm) sequence, followed by rapid thermal annealing at 850 °C for 30 s in a nitrogen-rich ambient. For the gate process, 0.8-μm-long gate metal (Ni/Au = 30/300 nm) was evaporated onto the in-situ SiNx layer and the gate was located in the middle place of 6 μm drain-to-source spacing. Finally, interconnection metals were deposited (Ti/Au = 50/300 nm), and a 150-nm thick $SiO_2$ final passivation layer was deposited.

## 3. Results and discussion

Fig. 2(a) shows the high resolution X-ray diffraction (HR-XRD) $\omega$-$2\theta$ scans rocking curves for (002) reflection of AlGaN/GaN structures grown on bulk GaN and SiC substrates to confirm the Al composition and the crystal quality. A sharp peak is resolved at 17.2° corresponding to the known equilibrium GaN lattice constant. Rocking curve measurements on GaN films revealed the full-width hall maximum (FWHM) of 146 arcsec and 237 arcsec for the HEMT on GaN and SiC substrates, respectively. The narrower GaN peak signal was obtained on free-standing GaN substrate because of its ultralow dislocation density and lattice matched buffer and substrate materials. As to the AlGaN quality, the AlGaN signal was separated to $Al_{0.24}Ga_{0.76}N$ Schottky layer and $Al_{0.08}Ga_{0.92}N$ back barrier layer. The fitting $Al_{0.24}Ga_{0.76}N$ FWHM and $Al_{0.08}Ga_{0.92}N$ FWHM signals were 221 arcsec, 210 arcsec of GaN on GaN device

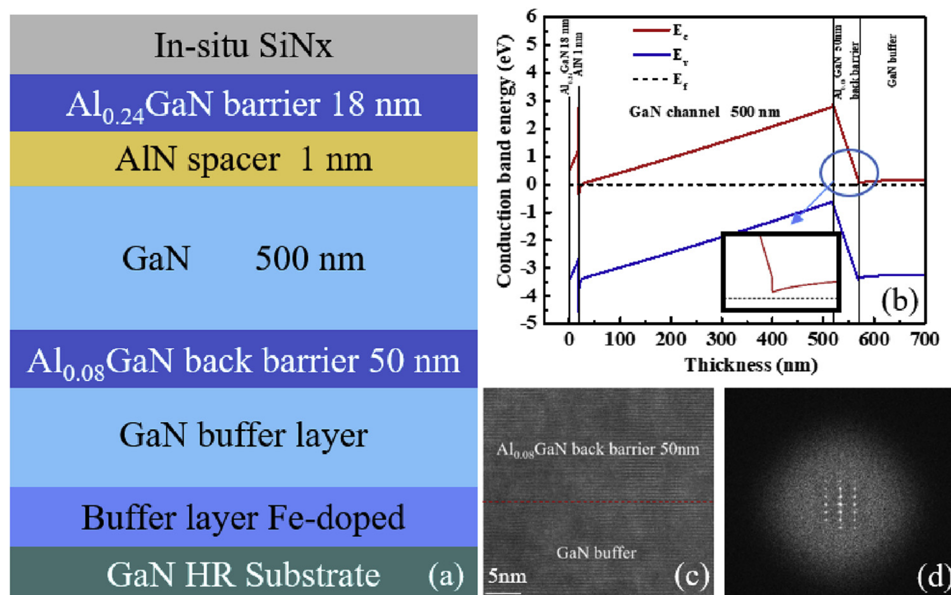



Fig. 1. (a) Cross-sections of in-situ $SiN_x$/AlGaN/AlN/GaN HEMT, (b) simulated band diagram (c) TEM image of $Al_{0.08}Ga_{0.92}N$ back barrier layer (d) FFT diffractogram of the $Al_{0.08}Ga_{0.92}N$ back barrier layer.

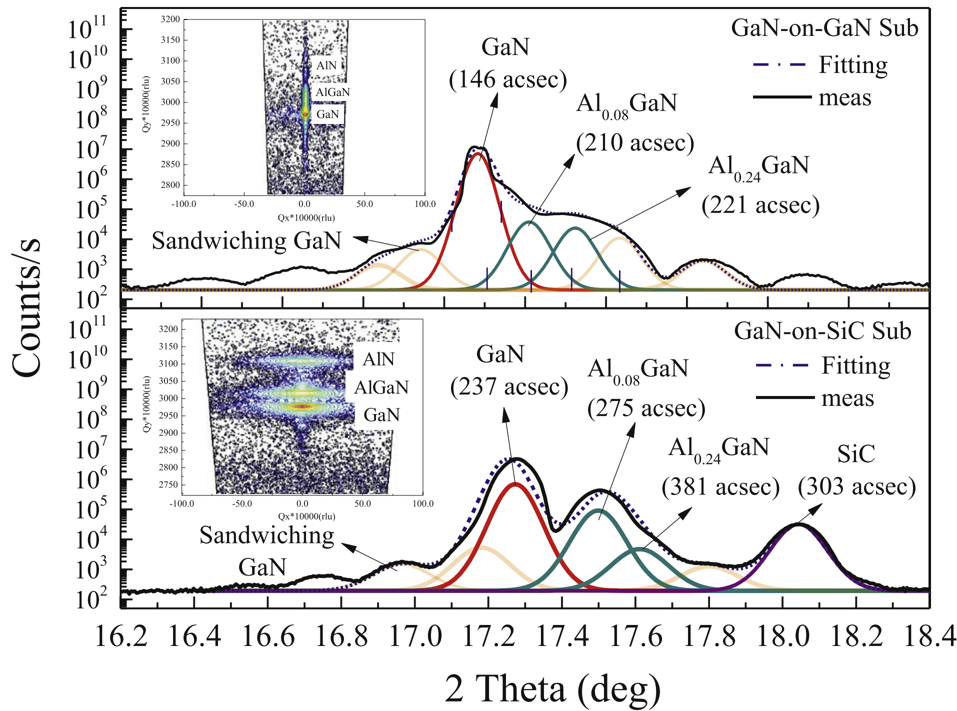



**Fig. 2.** X-ray-diffraction profiles of GaN HEMT structure on GaN and SiC substrates.

and these values were 381 arcsec, 275 arcsec of GaN on SiC device. In order to further evaluate the heterostructure quality for both devices, the reciprocal space maps (RSMs) of the in-situ $SiN_x$/AlGaN/AlN/GaN HEMTs on the bulk GaN and SiC substrates were obtained by using high-resolution X-ray diffraction (HR-XRD). The inset figure of Fig. 2 illustrated that the difference in the mosaic spread, particularly for AlN, AlGaN and GaN, is significant. The RSM centers of AlN and AlGaN performed the obvious splits in GaN on GaN device, indicating that misorientations were influenced by the lattice mismatch between GaN and SiC. Compared to this novel GaN on GaN structure, broadening in the RSM of the GaN on SiC device indicates an increase in either mosaicity or the density of dislocations.

The Micro-Raman spectrums for both samples were shown in Fig. 3 to investigate the heterostructure stress. For the GaN on SiC samples, the folded transverse acoustic (FTA) and longitudinal optical (LO) mode were both observed and these signals showed a highly agreement with published paper [13]. The $E_2$ (high) phonon peak was generally used to characterize the in-plane strain state of the GaN epilayer. The $E_2$ peak of GaN on GaN device was found to be 567.12 $cm^{-1}$ and the standard freestanding GaN film value is 567.1 $cm^{-1}$ [14]. As compared to the device on SiC substrate (566.65 $cm^{-1}$), an obvious epitaxial tensile stress was built in GaN on SiC device owing to lattice mismatched GaN/SiC interface. The value of the stress could be calculated according to the formula: $\sigma = \Delta\omega/4.2\ (cm^{-1}Gp^{-1})$, where $\sigma$ is the stress and $\Delta\omega$is the $E_2$ (high) mode shift. Thus, the calculative stresses were determined to be 0.107 GPa for GaN on SiC device.

Fig. 4 displays the drain-to-source current ($I_{DS}$) and output transconductance ($g_m$) versus gate-to-source voltage ($V_{GS}$) of the in-situ $SiN_x$/AlGaN/AlN/GaN HEMT with AlGaN back barrier design on the two substrates at $V_{DS} = 10$ V and 300 and 400 K, respectively. The devices dimension for electrical characterization is 0.8 μm gate length together with a drain-to-source distance of 6 μm. For devices on the GaN and SiC substrates, the maximum $I_{DS}$ at $V_{GS} = 2$ V were 700 and 582 mA/mm, respectively, and the peak $g_m$ values were 143 and 85 mS/mm appeared at $V_{DS} = -2$ V, respectively. The output current and $g_m$ improvement was thus observed for the bulk GaN substrate HEMT owing to its less lattice strain. In addition, previous study has reported that this thermal boundary resistance (TBR) in traditional GaN HEMT on SiC substrates can reach higher value than $6 \times 10^{-4}$ $cm^2K/W$, which leads to the device's maximum temperature increasing by up to 40%–50% [15]. The room temperature thermal conductivity of 250–300 $W\,m^{-1}\,K^{-1}$ was also measured for bulk GaN and this value is in the range of the highest GaN thermal conductivities demonstrated for MOCVD-growth epi wafers. For traditional buffer without back barrier design, the buffer/substrate induced current collapse is related to the injection of hot electrons into the buffer layer traps at high drain voltage. The energy of hot electrons would be reduced at higher lattice temperature due to the increased scattering of optical phonons. In addition, the emission of the trapped electrons would be enhanced at elevated temperature. Thus, the degree of measured buffer-induced current collapse drops sharply with increased temperature. At the device of GaN on SiC device, there is comparatively high characteristics drop in temperature indicating a thermal boundary resistance at this interface. Adding to the existing heat in the device, this difference heat is reflected back into the device, further increasing the temperatures in the active region. Therefore, the output current and the $g_m$ of the GaN HEMT on GaN substrate showed a better thermal stability which can be easily observed in Fig. 4 owing to its lattice matched epitaxy/substrate interface.

The pulsed $I$–$V$ test was performed with an AMCAD AM241 pulsed $I$–$V$ system at 300 and 400 K environments. In Fig. 5(a), the $I_{DS}$-$V_{DS}$ pulsed characteristics were also measured from different quiescent bias points at $V_{GS} = 2$ V to investigate the influence of OFF-state drain bias stress on dynamic $R_{ON}$ and $I_{DS}$. The reference bias was set as ($V_{GSQ}$, $V_{DSQ}$) = (0 V, 0 V), which does not induce any relevant trapping. The device is switched with 2 μs pulse width and 200 μs pulse period, respectively. The quiescent drain bias ($V_{DSQ}$) was swept from 0 to 100 V with 20 V increments and the quiescent gate bias was swept to -6V. The current collapse characteristics [$V_Q$

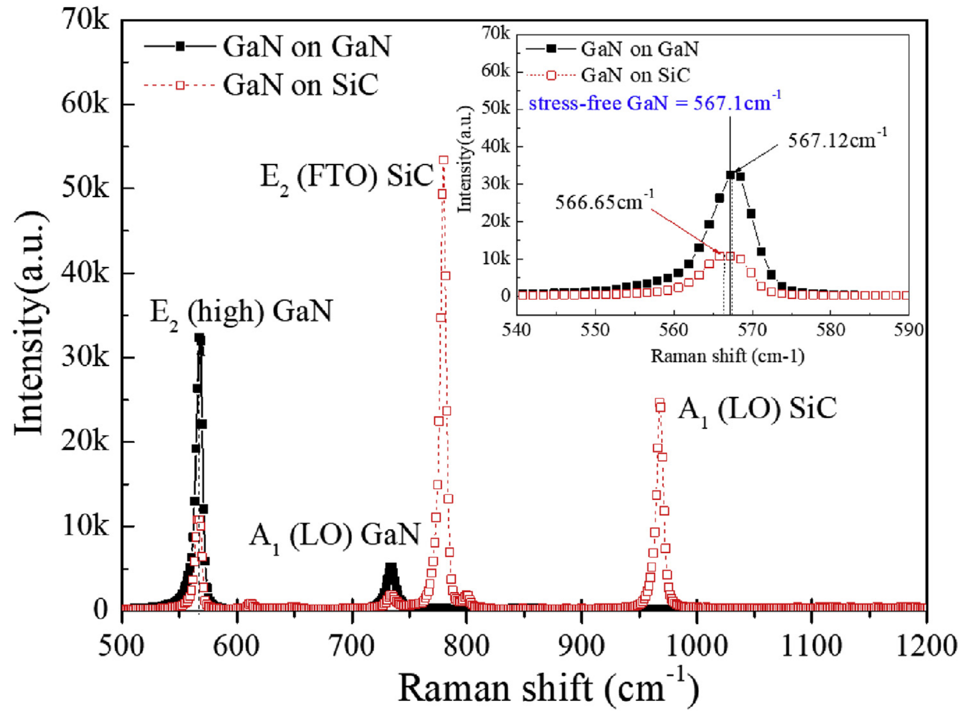



**Fig. 3.** The typical Raman spectra for both samples.

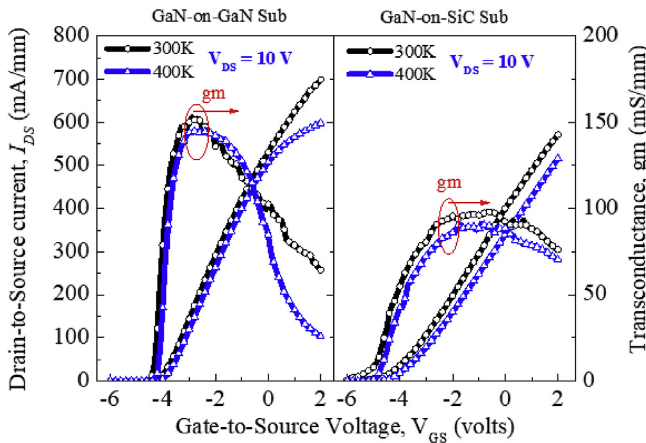



**Fig. 4.** Measured $I_{DS}$–$V_{GS}$ and $g_m$–$V_{GS}$ curves at $V_{DS} = 10$ V for both devices.

(0, 0) to $V_Q$ (−6100)] were 12% and 24% for bulk GaN and SiC substrate devices and these values were increased to 16% and 33% at 400 K environment. Apparently, the current collapse of GaN on SiC device is worse than that of GaN on GaN device, and the high drain lag of the GaN on SiC device under relatively high drain voltage OFF-state stress result in I–V slope decreases, indicating its buffer trap density is higher than that of the GaN on GaN device. As Fig. 5(b) shown at room temperature (300K), the dynamic $R_{ON}$ ($R_{ON,D}/R_{ON,Q}$) of GaN on GaN device slightly increased to 1.22 (1.28 @400 K) with higher drain bias stress from 0 V to 100 V because of low electron injection into the buffer trap states from the gate electrode, and the dynamic $R_{ON}$ ratio was increased to 1.43 (1.54 @400 K) at the OFF-state drain bias stress of 100 V for the GaN on SiC device. These results have shown highly agreements to the XRD, Raman, and DC measurement results.

To examine traps in the buffer/substrate interfacial layers of both devices, low-frequency noise (LFN) spectra were measured at various gate overdrive voltages. The drain current power spectral density $S_{ID}$ was measured and normalized to the square of the drain current versus frequency at a frequency of 100 Hz. If the slope of $S_{ID}/I_D^2$ is close to −1, the spectral fluctuation is dominated by the mobility fluctuation model, but if it approaches −2, it is dominated by fluctuation in the carrier numbers [16]. A value between −1 and −2 indicates that the noise is attributable to the correlation between the number of carriers and mobility fluctuation. The slopes at 300 K for the AlGaN/GaN HEMT on the GaN and SiC substrates are −1.91 and −1.66, respectively. These measured results were −2.24 and −2.75, respectively measured at 400 K for both devices. Therefore, the mobility fluctuation theory considers that 1/f noise is a result of the fluctuation in mobility based on Hooge's empirical relation for $S_{ID}/I_D^2$, as follows:

$$\alpha_H = \frac{S_{ID} f W L C_b (V_{GS} - V_{th})}{q I^2} \quad (1)$$

where $\alpha_H$ is the Hooge parameter. As illustrated in Fig. 6, the average $\alpha_H$ values at 300 and 400 K were $1.15 \times 10^{-5}$ and $5.02 \times 10^{-5}$, respectively, for the HEMTs on the GaN substrate. The results for the HEMTs on the SiC substrate were $6.55 \times 10^{-5}$ and $2.89 \times 10^{-4}$, indicating the matched buffer/substrate interface are beneficial to improve the device interface noise.

To determine the effect of substrate isolation on both devices on RF performance, the microwave S-parameters of both devices were evaluated using a common-source configuration and a PNA network analyzer in conjunction with Cascade direct probes. The S-parameters measurement frequency range is from 100 MHz to 28 GHz with the operating condition $V_{DS} = 10$V. Based on the optimal RF operation for both devices, the $V_{GS}$ were defined at the appearance of their peak $g_m$ and the $V_{GS}$ bias voltages were −2.8V and −2V for the device on GaN substrate and SiC substrate, respectively. As shown in Fig. 7, the current gain cut-off frequency ($f_T$) and maximum stable gain cut-off frequency ($f_{max}$) were 13 GHz

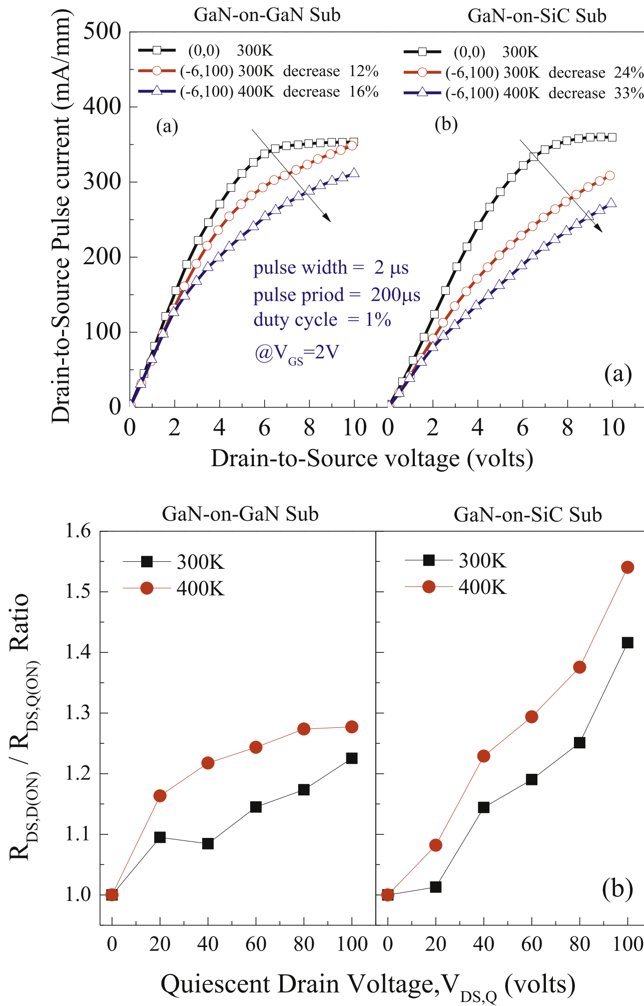



**Fig. 5.** (a)Pulse $I$–$V$; (b) Dynamic $R_{ON}$ measurement for the two devices.

and 24 GHz for GaN on GaN device. Owing to the GaN/SiC mismatch induced strain, these values were 8.7 GHz and 19.8 GHz for GaN on SiC one. These microwave gain cut-off frequencies were strongly influenced by the device mobility fluctuation caused by the trapping effect. These two cut-off frequencies are important indexes to evaluate the RF bandwidth of a transistor. Generally, following well-known equations are shown [17]:

$$f_T = \frac{f_C}{\left(1+\frac{C_{gd}}{C_{gs}}\right) + (R_S+R_d)\left[\frac{C_{gd}}{C_{gs}}(g_m+g_{dS})+g_{dS}\right]} \quad (2)$$

$$f_{MAX} = \frac{f_C}{2\left(1+\frac{C_{gd}}{C_{gs}}\right)\sqrt{g_{dS}(R_S+R_d)+\frac{1}{2}\frac{C_{gd}}{C_{gs}}\left(R_S g_m+\frac{C_{gd}}{C_{gs}}\right)}} \quad (3)$$

$R_g$, $R_s$, $R_d$ are gate resistance, source resistance, and drain resistance, respectively. $G_{ds}$ is the AC drain conductance and $G_m$ is the AC transconductance. $C_{ds}$, $C_{gs}$ and $C_{gd}$ are the drain-to-source capacitance, gate-to-source capacitance and gate-to-drain capacitance, respectively. By extracting the small signal model, GaN on GaN device obviously performed a small output conductance ($g_{ds}$) and a small gate-to-drain feedback capacitance ($C_{gd}$) which are beneficial to increase device bandwidth as compared with GaN on SiC device. The detailed small-signal parameters comparison was also shown in Fig. 7. Therefore, the reduction of gate-to-drain feedback capacitance can be concluded to the contribution of 50-nm $Al_{0.08}Ga_{0.92}N$ back barrier which showed a highly agreement and discussion in previous study with p-GaN back barrier design [18].

## 4. Conclusion

In this work, AlGaN back-barrier has been introduced in AlGaN/GaN HEMTs. Due to the higher HEMT epi quality layer on free-standing GaN wafer, the devices on free-standing wafer show higher drain current, improved transconductance, less current collapse, higher current gain cut-off frequency, and higher

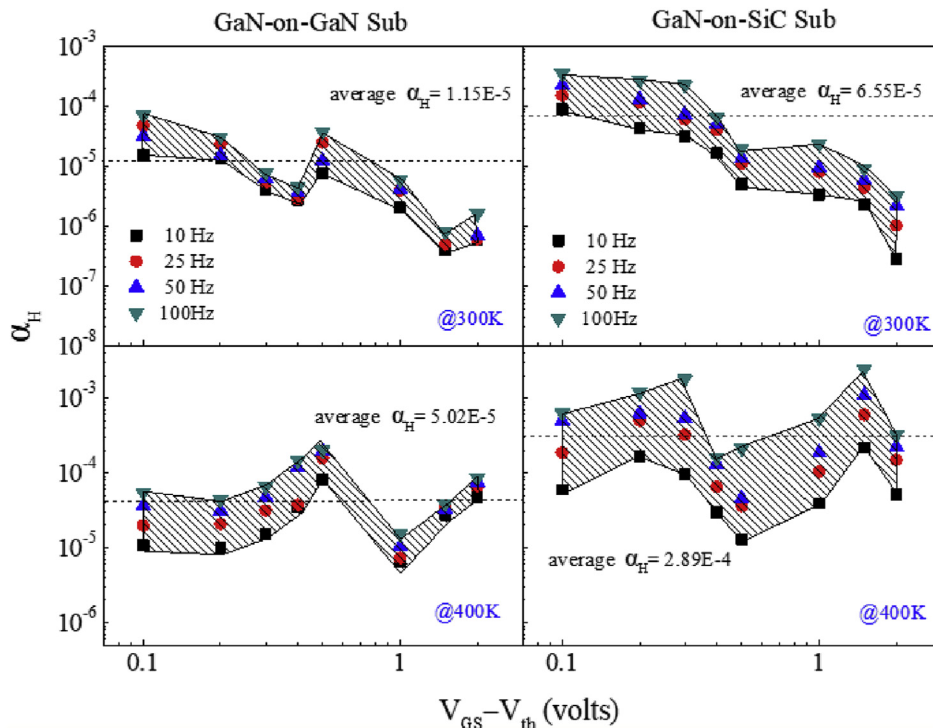
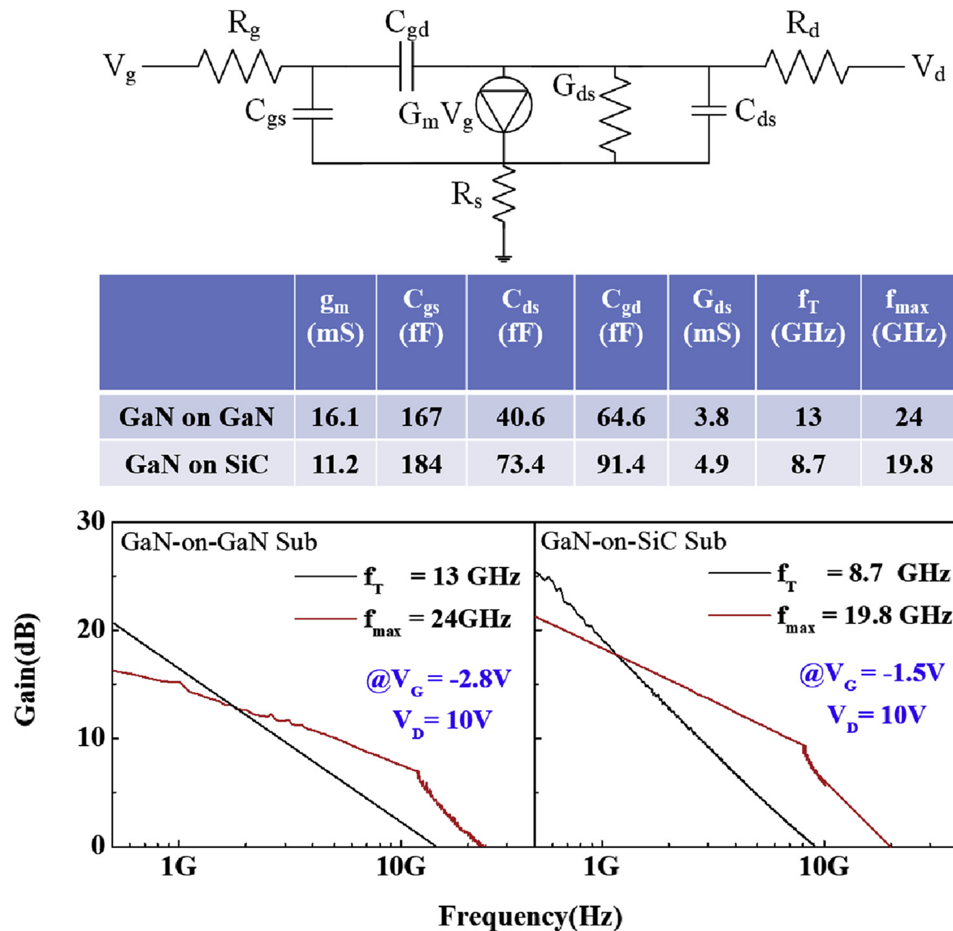



**Fig. 6.** Temperature dependent Hooge parameters distributions for the two devices.



| | $g_m$ (mS) | $C_{gs}$ (fF) | $C_{ds}$ (fF) | $C_{gd}$ (fF) | $G_{ds}$ (mS) | $f_T$ (GHz) | $f_{max}$ (GHz) |
|---|---|---|---|---|---|---|---|
| GaN on GaN | 16.1 | 167 | 40.6 | 64.6 | 3.8 | 13 | 24 |
| GaN on SiC | 11.2 | 184 | 73.4 | 91.4 | 4.9 | 8.7 | 19.8 |



**Fig. 7.** $f_T$ and $f_{max}$ for both devices.

maximum stable gain cut-off frequency. In addition, traps caused by the native nitrogen-vacancies and $GaO_x$ compounds of the HVPE-grown free-standing GaN substrate was overcome by this back barrier design. The lattice matched substrate/epilayer showed a low thermal boundary interface resulting a thermally stable electrical characteristics. AlGaN/GaN HEMTs on free-standing wafer is a promising technology option for high frequency and high power application.

## Acknowledgments

This study was funded by National Key Research and Development Plan (2017YFB0404100, 2017YFB0403000), the Ministry of Science and Technology, Taiwan (MOST 108-2218-E-182-006), National Science Fund for Distinguished Young Scholars (61725403), National Natural Science Foundation of China (61974144), CAS Pioneer Hundred Talents Program,and in part by the Institute for Radiological Research Center, CGU under Grant CIRPD2F0021.

## References


[1] Y.F. Wu, D. Kapolnek, J.P. Ibbetson, P. Parikh, B.K. Keller, U.K. Mishra, IEEE Trans. Electron Devices 48 (2001) 586–590.
[2] T. Kuwabara, N. Tawa, Y. Tone, T. Kaneko, in: 2017 IEEE Compound Semiconductor Integrated Circuit Symposium, CSICS), 2017, pp. 1–4.
[3] S. Nakajima, in: 2018 IEEE International Electron Devices Meeting, 2018, pp. 14.2.1–14.2.4.
[4] J.L. Jimenez, U. Chowdhury, in: 2009 Reliability of Compound Semiconductors Digest, ROCS), 2009, pp. 57–58.
[5] S. Mukherjee, E.E. Patrick, M.E. Law, ECS Journal of Solid State Science and Technology 6 (2017) S3093–S3098.
[6] D.F. Storm, D.S. Katzera, J.A. Roussos, J.A. Mittereder, R. Bass, S.C. Binari, D. Hanser, E.A. Preble, K.R. Evans, J. Cryst. Growth 301 (2007) 429–433.
[7] Anna Barbara Piotrowska, Eliana Anetka Kaminska, Wojciech Wojtasiak, Wojciech Gwarek, Robert Kucharski, Marcin Zajac, Pawel Prystawkod, Piotr Kruszewskid, Marek Ekielski, Jakub Kaczmarski, Maciej Kozubal, Artur Trajnerowicz, Andrzej Taubef, Manufacturing microwave AlGaN/GaN high electron mobility transistors (HEMTs) on truly bulk semi-insulating GaN substrates", ECS Transactions 75 (2016) 77–84.
[8] S. Porowski, Materials Research Society Internet Journal of Nitride Semiconductor Research 4 (1999) 27–37.
[9] Y. Zhang, J. Wang, S. Zheng, D. Cai, Y. Xu, M. Wang, X. Hu, M. Zhao, K. Xu, APEX 12 (2019), 074002.
[10] R. Doradziński, M. Zając, and R. Kucharski, International Patent Application, PCT/EP2014/055876.
[11] Y. Kawada, H. Hanawa, K. Horio, Jpn. J. Appl. Phys. 56 (2017) 108003.
[12] E.B. Treidel, F. Brunner, O. Hilt, E. Cho, J. Würfl, G. Tränkle, IEEE Trans. Electron Devices 57 (2010) 3050–3058.
[13] Y. Peng, X. Hu, X. Xu, X. Chen, J. Peng, J. Han, S. Dimitrihev, Opt. Mater. Express 6 (2016) 2725–2733.
[14] L. Zhang, J. Yu, X. Hao, Y. Wu, Y. Dai, Y. Shao, H. Zhang, Y. Tian, Sci. Rep. 4 (2014) 4179.
[15] A. Manoi, J.W. Pomeroy, N. Killat, M. Kuball, IEEE Electron. Device Lett. 31 (2010) 1395–1397.
[16] P. Magnone, F. Crupi, G. Giusi, C. Pace, E. Simoen, C. Claeys, L. Pantisano, D. Maji, V. Ramgopal Rao, P. Srinivasan, IEEE Trans. Device Mater. Reliab. 9 (2009) 180–189.
[17] H.-C. Chiu, C.-W. Yang, H.-C. Wang, F.-H. Huang, H.-L. Kao, F.-T. Chien, IEEE Trans. Electron Devices 60 (2013) 3877–3882.
[18] Sarosij Adak, Arghyadeep Sarkar, Sanjit Swain, Hemant Pardeshi, Sudhansu Kumar Pati, Chandan Kumar Sarkar, Superlattice Microstruct. 75 (2014) 347–357.