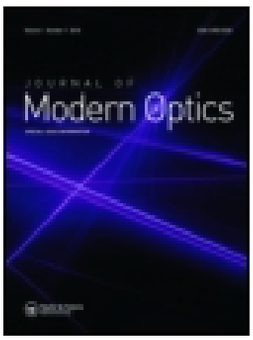

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120 Gb/s all-optical NAND logic gate using reflective semiconductor optical amplifiers

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ABSTRACT

In this paper, the unique features of the reflective semiconductor optical amplifiers (RSOAs) are exploited to numerically simulate the ultrafast performance of an all-optical NOT-AND (NAND) logic gate for the first time using a return-to-zero modulation format at a data rate of 120 Gb/s. A comparison is made between RSOAs and conventional SOAs through studying the dependence of the gate's quality factor (QF) on the critical operational parameters, including the effects of both amplified spontaneous emission and operating temperature to get more realistic results. The results show that the all-optical NAND logic gate can be executed at 120 Gb/s using the RSOAs scheme with a higher QF than when using conventional SOAs.

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KEYWORDS
All-optical NAND logic gate; reflective semiconductor optical amplifiers; quality factor

Introduction

Recently, semiconductor optical amplifiers (SOAs) and quantum-dot SOAs (QDSOAs) have attracted a huge amount of attention not only for amplification but also for optical signal processing. SOAs and QDSOAs offer considerable advantages over optical fibres in optical signal processing applications; these advantages are not limited to the compact size, low energy requirement, and ability of monolithic integration [1–3]. However, SOAs have infinite gain and phase recovery times, which limit the SOAs' operational data rates do not exceed $\sim$ 100 Gb/s and QDSOAs also face a big challenge in real applications due to some practical issues. On the other hand, reflective SOAs (RSOAs) have waveguide structures similar to conventional SOAs but have more advantages over SOAs, such as higher optical gain and lower noise figure at low injection currents with energy-efficient [1]. RSOAs are very important devices as colourless upstream transmitters for optical network units in a wavelength division multiplexed passive optical network [1]. RSOAs utilize an anti-reflective (AR) coating on the front fact and a high reflectivity (HR) coating on the rear fact (Figure 1). Based on the RSOAs' unique structure, the travelling signal is amplified twice over the active region. This feedback processing due to the forward and backward travelling waves through ROSAs provides high optical gain and addition to that obviates the need for extra optical hardware. Therefore, it is a priority to use the RSOAs' technology in designing optical logic gates at high data rates. Thus, in this article, all-optical NOT-AND (NAND) logic gate is numerically simulated for the first time to the best of our knowledge using a return-to-zero modulation format based on the dual-RSOAs-based scheme at 120 Gb/s to complete and extend our previous work based on RSOAs' technology [4]. The quality of the considered operation is examined and assessed using the quality factor (QF) metric for both RSOAs and conventional SOAs schemes, including the effects of the amplified spontaneous emission (ASE) and operating temperature (T_{OP}) to get more realistic results. The outcomes of Wolfram Mathematica show that the NAND logic gate can be executed at 120 Gb/s with higher QF using RSOAs than when using conventional SOAs.

All-optical NAND logic gate at 120 Gb/s

A Gaussian pulse has been widely used in optical networks due to its properties of maximum transition steepness with no overshoot and minimum group delay. The input optical pulses ($P_{in}(t)$) used herein are assumed to be

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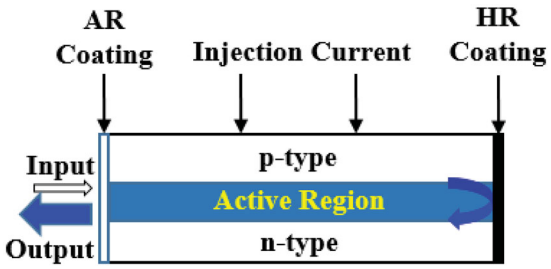

Figure 1. Schematic of RSOA device.

Gaussian-shaped pulses having energy (E_0), full-width at half maximum (FWHM) pulse width (τ_{FWHM}), and bit period (T), which is defined as the inverse of the operating data rate ($T = 1000/\text{data rate} = 8.33$ ps @ 120 Gb/s), i.e. [1,2,4]:

$$P_{A,B,Clk}(t) \equiv P_{in}(t) = \sum_{n=1}^{N} a_{n(A,B,Clk)} \frac{2\sqrt{\ln[2]}\ E_0}{\sqrt{\pi}\ \tau_{FWHM}} \times \exp\left[-\frac{4\ln[2](t-nT)^2}{\tau_{FWHM}^2}\right] \quad (1)$$

where $P_{A,B,Clk}(t)$ are the input powers of the signals A, B, and the clock signal (Clk). $a_{n(A,B,Clk)}$ is the n-th pulse, which can take '1's for Clk and '1' or '0' for signals A and B. $N = 2^7$-1 [4–7] is the length of the pseudorandom binary sequence (PRBS).

The operation of the RSOAs can be numerically studied based on the computational accurate models mentioned in Refs. [8–10]. The model used herein allows examining the RSOA response to an optical excitation by solving a couple of standard differential equations in the time domain, and hence reduction in the computational complexity. The interband nonlinear effect of the carrier depletion (CD) takes into account only the transition process from the conduction band to the valence band. However, the intraband nonlinear effects of the carrier heating (CH) and spectral hole burning (SHB) cause a redistribution of carriers in the conduction band, and therefore they contribute to the gain process. For higher energy, carrier heating (CH) is generated inside each RSOA when the carriers' temperature became higher than the lattice temperature. Also, higher energy burns a hole in the gain spectrum, resulting in a SHB effect [1]. These two nonlinear processes occur in a short time of subpicosecond and should not be neglected when providing an accurate theoretical model of RSOAs behaviour. Therefore, the time domain differential equations of the RSOA, including the effects of CH and SHB as well as the effect of the CD, are given by [4]:

$$\frac{dh_{CD}(t)}{dt} = \frac{h_0 - h_{CD}(t)}{\tau_C} - \frac{h_{CD}(t)}{h_{CD}(t) - \alpha_{loss}L} \times (\exp[h_{CD}(t) + h_{CH}(t) + h_{SHB}(t) - \alpha_{loss}L] - 1) \times (1 + R\exp[h_{CD}(t) + h_{CH}(t) + h_{SHB}(t) - \alpha_{loss}L])\frac{P_{in}(t)}{E_{sat}} \quad (2)$$

$$\frac{dh_{CH}(t)}{dt} = -\frac{h_{CH}(t)}{\tau_{CH}} - \frac{\varepsilon_{CH}}{\tau_{CH}}(\exp[h_{CD}(t) + h_{CH}(t) + h_{SHB}(t) - \alpha_{loss}L] - 1) \times (1 + R\exp[h_{CD}(t) + h_{CH}(t) + h_{SHB}(t) - \alpha_{loss}L])\, P_{in}(t) \quad (3)$$

$$\frac{dh_{SHB}(t)}{dt} = -\frac{h_{SHB}(t)}{\tau_{SHB}} - \frac{\varepsilon_{SHB}}{\tau_{SHB}}(\exp[h_{CD}(t) + h_{CH}(t) + h_{SHB}(t) - \alpha_{loss}L] - 1) \times (1 + R\exp[h_{CD}(t) + h_{CH}(t) + h_{SHB}(t) - \alpha_{loss}L])\, P_{in}(t) - \frac{dh_{CD}(t)}{dt} - \frac{dh_{CH}(t)}{dt} \quad (4)$$

where functions 'h' represent the RSOAs' gain integrated over the RSOAs' length induced due to CD (h_{CD}), CH (h_{CH}), and SHB (h_{SHB}). R is the rear-facet reflectivity, which is ~ 0 for conventional SOAs, α_{loss} is the internal loss coefficient, and L is the length of the active layer. $G_0 = \exp[2h_0]$ [4,11], taking into account the double pass of the signal propagating inside the RSOAs active layer, where G_0 is the unsaturated power gain with the need to note that $G_0 = \exp[h_0]$ [5–7] is used for conventional SOAs. G_0 is related to the key operational parameters through [1]:

$$G_0 = \alpha\Gamma\left(\frac{I\tau_c}{eV} - N_{tr}\right)L \quad (5)$$

where α is the differential gain, Γ is the optical confinement factor, I is the injection current, τ_c is the carrier lifetime, e is the electron charge, V is the active layer volume, and N_{tr} is the transparency carrier density. E_{sat} is the saturation energy defined as [1]:

$$E_{sat} = P_{sat}\tau_c = \frac{wd\hbar\omega_0}{\alpha\Gamma} \quad (6)$$

where P_{sat} is the saturation power, w & d are the width and thickens of the active layer, respectively, $\hbar$ is Planck's

constant divided by 2π, and ω_0 is the central frequency. τ_{CH} and τ_{SHB} are the temperature relaxation rate and carrier-carrier scattering rate, respectively. ϵ_{CH} and ϵ_{SHB} are the CH and SHB nonlinear gain suppression factors, respectively. The SOAs time-dependent differential equations are described in detail in Refs [1,2].

The input signal passes twice inside the active layer, which doubles the resulting gain, i.e. [4]:

$$G_{RSOA_i}(t) = R\exp[2(h_{CD}(t) + h_{CH}(t) + h_{SHB}(t) - \alpha_{\text{loss}}L)], \quad i = 1,2,3,4 \tag{7}$$

While the phase change incurred on the input probe signal propagating through each RSOA as a result of its gain perturbation is given by [4]:

$$\Phi_{RSOA_i}(t) = -(\alpha h_{CD}(t) + \alpha_{CH}h_{CH}(t) + \alpha_{SHB}h_{SHB}(t)), \quad i = 1,2,3,4 \tag{8}$$

where α is the traditional linewidth enhancement factor known as α-factor, α_{CH} is the CH linewidth enhancement factor, and α_{SHB} is the SHB linewidth enhancement factor. The contribution value of the α_{SHB} is null because the SHB effect produces a nearly symmetrical spectral hole centred at the input signal wavelength [4,12].

The NAND logic gate produces '1' output only if any of its inputs are '0'; thus NAND gate is the invert of an AND gate. The NAND schematic diagram and its corresponding truth table using the dual-RSOAs-based scheme are shown in Figure 2.

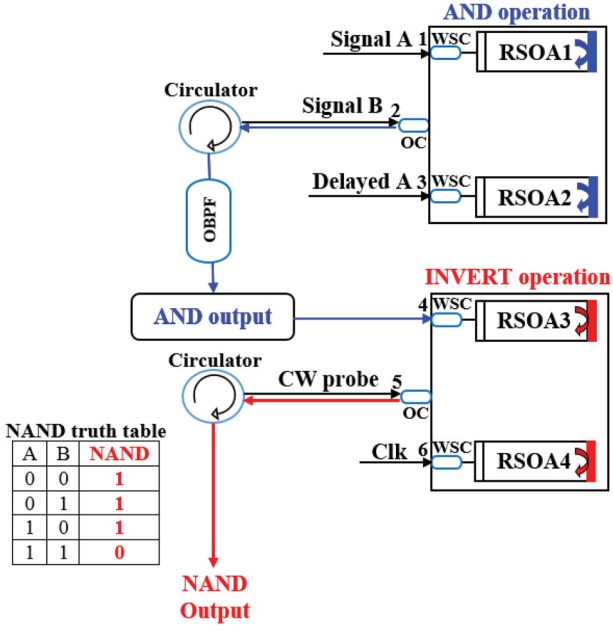

Figure 2. Schematic diagram and truth table of NAND logic gate using dual-RSOAs. OC: 3 dB optical coupler, WSC: wavelength selective coupler, and OBPF: 3 nm optical bandpass filter.

For AND operation, signal A and its delayed version are inserted into RSOA1 and RSOA2, respectively, while signal B is equally split by a 3 dB OC and then injected into both RSOA1 and RSOA2 from port 2. In the upper and lower arms, the phase of signal B will be modulated by signal A versions. When $A = 0$, the phase change induced by A does not exist, resulting in '0' output; when $B = 0$, no light injected by the signal carrying AND information into the system, resulting also in '0' output; when both A and B are '1', the upper and lower arms experience different gains and they have a constructive interference that means '1' output. To sum up, only when both signals A and B are '1' can this system produce '1' output, which is AND logic operation. After rejecting out all unwanted wavelength components using 3 nm OBPF, the AND output stream is guided into RSOA3 for INVERT operation. A Clk is injected into RSOA4 and a CW probe light is injected into the middle arm from port 5. In this way, the result coming out is INVERT AND, i.e. NAND gate.

For AND operation, the input optical powers going into RSOA1 and RSOA2 are, respectively, described by the following equations [6,12,13]:

$$P_{\text{in},RSOA_1}(t) = P_A(t) + 0.5P_B(t) \tag{9}$$

$$P_{\text{in},RSOA_2}(t) = P_{\text{Delayed }A}(t - \Delta\tau) + 0.5P_B(t) \tag{10}$$

where $\Delta\tau$ is the time delay of the delayed signal A.

Then, the AND output power at port 2 is given by [5,6,12,13]:

$$P_{\text{out,AND}}(t) = 0.25P_B(t)(G_{RSOA_1}(t) + G_{RSOA_2}(t) - 2\sqrt{G_{RSOA_1}(t)G_{RSOA_2}(t)} \times \cos[\Phi_{RSOA_1}(t) - \Phi_{RSOA_2}(t)]) \tag{11}$$

For INVERT operation, the optical powers inside RSOA3 and RSOA4 are, respectively, described by the following equations [6]:

$$P_{\text{in},RSOA_3}(t) = P_{AND}(t) + 0.5P_{CW} \tag{12}$$

$$P_{\text{in},RSOA_4}(t) = P_{Clk}(t) + 0.5P_{CW} \tag{13}$$

Then, the NAND output power at port 5 is given by [5,6]:

$$P_{\text{out,NAND}}(t) = 0.25P_{CW}(G_{RSOA_3}(t) + G_{RSOA_4}(t) - 2\sqrt{G_{RSOA_3}(t)G_{RSOA_4}(t)} \times \cos[\Phi_{RSOA_3}(t) - \Phi_{RSOA_4}(t)]) \tag{14}$$

To assess and examine the performance of the NAND logic gate, the QF metric is used. This metric is defined

as the mean peak powers of '1' and '0' divided by the sum of the corresponding noise standard deviations, i.e. $QF = (P_1 - P_0)/(\sigma_1 + \sigma_0)$ [4–6,13,14]. The QF value must exceed six to keep the related bit-error-rate [14,15] less than 10^{-9} [4,5,13,14] to ensure that the operational performance is acceptable. The differential equations of the RSOAs and SOAs are prepared and run by Adam's numerical method in Wolfram Mathematica using the operational parameters cited in Table 1. Notice, these parameters are completely harmonious with the cited publications that have used (R)SOAs with the same characteristics.

Figures 3 and 4 illustrate the numerical results for the NAND logic gate between indicative patterns of signals A and B using the dual-RSOAs-based scheme and SOAs-based Mach–Zehnder interferometers (MZIs) at 120 Gb/s, respectively. The QF using RSOAs is found to be 18.4, which is higher than when using conventional SOAs, i.e. 3.7.

The NAND QF variation against the rear-facet reflectivity (R) and internal loss coefficient (α_{loss}) using the proposed scheme based on RSOAs at 120 Gb/s is shown in Figure 5. It can be seen from Figure 5(a) that the

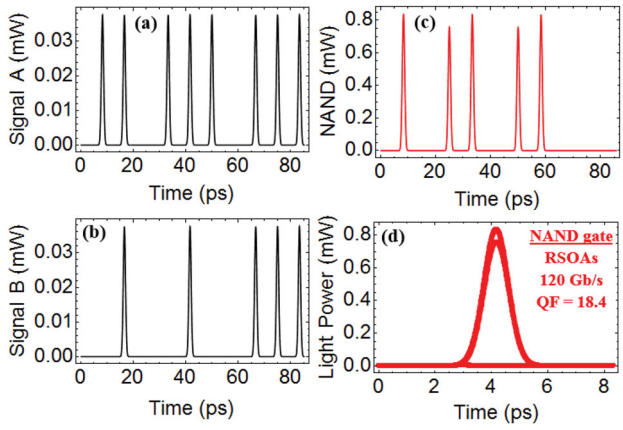

Figure 3. Numerical results of NAND logic gate using RSOAs. (a) Input signal A, (b) input signal B, (c) output NAND gate, and (d) corresponding eye diagram. The achieved QF is 18.4 at 120 Gb/s.

QF is increased as R becomes higher. The RSOAs' gain is mainly based on a rear-facet high-reflective coating that helps the input light to amplify and reflect back to the input port. This means that the input signal is amplified twice through propagating inside the RSOA active layer and, therefore, it receives twice as much

Table 1. Default parameters.

Symbol	Definition	Value	Unit	Ref.
E_0	Pulse energy	0.03	pJ	(*13*)
τ_{FWHM}	Pulse width	1	ps	(*4,5,11,13*)
T	Bit period	8.33	ps	(*4*)
N	PRBS length	127	-	(*4–7*)
$\Delta\tau$	Time delay	0.5	ps	(*13*)
λ_A	Wavelength of A versions	1580.4	nm	(*13*)
λ_B	Wavelength of B	1539.8	nm	(*13*)
λ_{CW}	Wavelength of CW	1545	nm	(*14*)
λ_{Clk}	Wavelength of Clk	1555	nm	(*14*)
P_A	Power of A versions	2	mW	(*16*)
P_B	Power of B	2	mW	(*16*)
P_{Clk}	Power of Clk	2	mW	(*16*)
P_{CW}	Power of CW beam	1	mW	(*16*)
P_{sat}	Saturation power	10	mW	(*4,6*)
I	Injection current	100	mA	(*4*)
R	RSOA rear-facet reflectivity	1	-	(*4*)
L	Length of active layer	400	μm	(*4*)
d	Thickness of active layer	0.3	μm	(*4,13*)
w	Width of active layer	1.5	μm	(*11*)
α_{loss}	Internal loss coefficient	10	mm^{-1}	(*4*)
α	α-factor	4	-	(*4,13,14*)
α_{CH}	CH linewidth enhancement factor	1	-	(*4–6*)
α_{SHB}	SHB linewidth enhancement factor	0	-	(*4–6*)
τ_C	Carrier lifetime	100	ps	(*4*)
τ_{CH}	Temperature relaxation rate	0.3	ps	(*4–6*)
τ_{SHB}	Carrier-carrier scattering rate	0.1	ps	(*4–6*)
ϵ_{CH}	CH nonlinear gain suppression factor	0.02	W^{-1}	(*4–6*)
ϵ_{SHB}	SHB nonlinear gain suppression factor	0.02	W^{-1}	(*4–6*)
N_{tr}	Transparency carrier density	10^{24}	m^{-3}	(*11,15*)
Γ	Optical confinement factor	0.15	-	(*4,13*)
α	Differential gain	2×10^{-20}	m^2	(*4,15,17*)
G_0	Unsaturated power gain	15	dB	(*4*)
B_0	Optical bandwidth	3	nm	(*5,11,13*)
υ	Optical frequency	193.54	THz	(*13*)
N_{SP}	Spontaneous emission factor	2	-	(*4,11,13*)
T_{OP}	Operating temperature	290	K	(*4,13*)

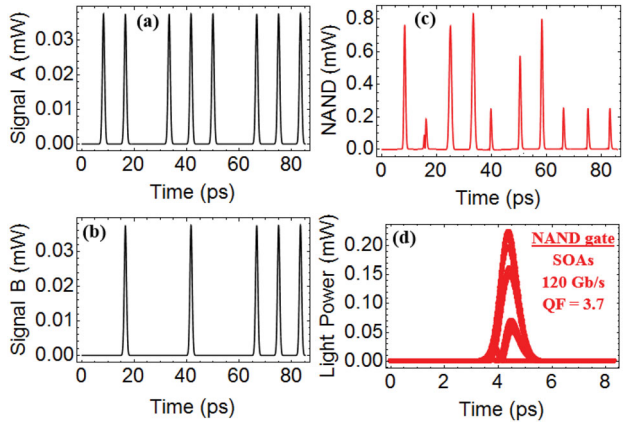

Figure 4. Numerical results of NAND logic gate using conventional SOAs. (a) Input signal A, (b) input signal B, (c) output NAND gate, and (d) corresponding eye diagram. The achieved QF is 3.7 at 120 Gb/s.

gain as in conventional SOAs ($R = 0$). On the other side (Figure 5(b)), we notice a different behaviour when QF versus α_{loss}; the QF is decreased as α_{loss} becomes more powerful. The reason for this is that the waveguide loss, which is caused by the uniform distribution of the input light, and the carrier absorption loss, which is caused by the carriers' recombination waste, are subject to α_{loss} [16,18]. The RSOAs scheme resists the internal loss and gives an acceptable quality value ($\sim$ 6.4) even at 40 mm^{-1}.

In the following results, we compare fairly between RSOAs and SOAs-based NAND gate by studying the QF dependence on the key operational parameters such as operating data rate, equivalent PRBS length, ASE noise, and operating temperature (T_{OP}).

The QF dependence on the operating data rate and equivalent PRBS length using both schemes, RSOAs- and SOAs-based NAND operation is shown in Figure 6. The QF is decreased by increasing the data rate as shown in Figure 6(a), but it remains higher and more acceptable ($\sim$ 7.2) even up to 220 Gb/s when only using RSOAs, while this is impossible even for less than a half data rate ($\sim$ 110 Gb/s) when using SOAs, which suffer a dynamic response problem. The same behaviour is observed in Figure 6(b) when the QF versus the equivalent PRBS length. The PRBS is very important for a huge range of applications in communication systems such as testing, bit-scrambling, and bit-descrambling [1]. The QF

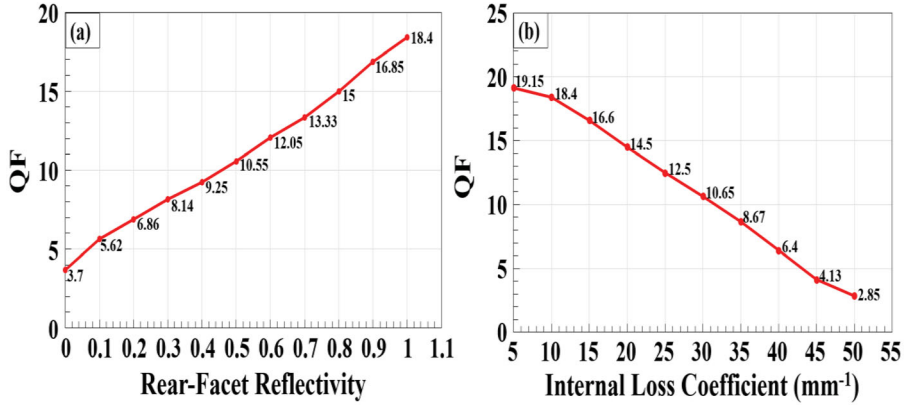

Figure 5. QF of NAND logic gate versus (a) rear-facet reflectivity and (b) internal loss coefficient for RSOAs at 120 Gb/s.

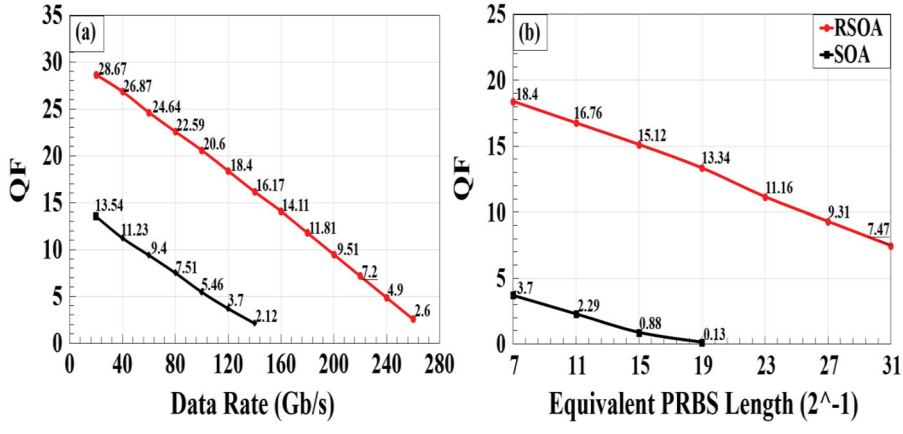

Figure 6. QF of NAND logic gate versus (a) operating data rate and (b) equivalent PRBS length for both RSOAs and conventional SOAs.

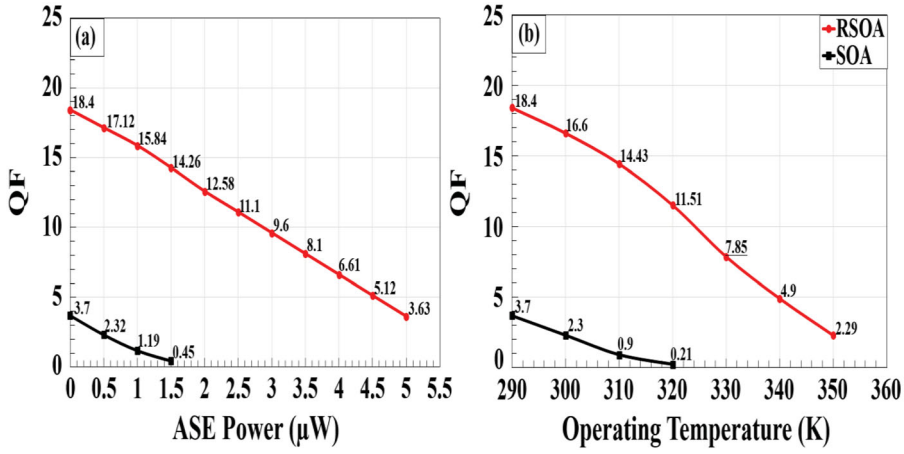

Figure 7. QF of NAND logic gate versus (a) ASE power and (b) operating temperature for both RSOAs and conventional SOAs at 120 Gb/s.

is decreased as the value of the PRBS increases in both cases, but the RSOAs scheme is tolerant to this effect and keeps the logic performance acceptable ($\sim$ 7.47) even up to 31 equivalent PRBS length, whilst this is impossible when using SOAs instead. The results of Figure 5(a) and (b) confirm that the scheme based on RSOAs is a more suitable candidate for applications in high-capacity and long PRBS.

During the above calculations, the effects of the ASE noise and T_{OP} are taken as fixed parameters. However, these parameters may also have critical effects on the NAND performance. Therefore, these parameters' effects on the QF should be taken into account, as done in Figure 7. The ASE acted as the noise causes the degradation of the amplifiers' performance. In this calculations, we took into account the ASE effect on the QF using $P_{ASE} = N_{SP}\ (G_0 - 1)\ 2\pi\hbar\upsilon B_0$, where N_{SP} is the spontaneous emission factor, which has a value of 2 for an ideal amplifier [17,19], υ is the optical frequency, and B_0 is the optical bandwidth [4–6,11,13]. This ASE power is numerically added to the AND and NAND output powers given from equations (11) and (14), respectively. It is seen from Figure 7(a) that the QF is decreased in the increase of the ASE power for both RSOAs and SOAs, but the RSOAs scheme provides an acceptable quality value even when the value of the ASE power is aggravated, while the situation is different for SOAs scheme. This happens because the RSOAs are operated around deep saturation, therefore their gain dynamics are not affected by ASE noise [4]. The RSOA gets more impressed when its performance is tested at high temperatures as shown in Figure 7(b), where the RSOAs can be operated up to 330 K, where it has 7.85 QF. The RSOAs are packaged in a TO-can type, which is very important for efficient cooling during operation. These results confirm that the RSOAs can operate in difficult conditions with keeping the performance acceptable.

Conclusions

We succeeded in the numerical simulation of an all-optical NAND logic gate using a dual-reflective semiconductor optical amplifiers (RSOAs) scheme at speed of 120 Gb/s. The ultrafast performance of the NAND logic gate was assessed and examined through studying the dependence of the quality factor (QF) on the critical operational parameters such as rear-facet reflectivity, internal loss coefficient, operating data rate, equivalent PRBS length, ASE power, and operating temperature. The outcomes indicate that the ultrafast performance of the all-optical NAND logic function can be executed using a dual-RSOAs scheme at 120 Gb/s with higher QF even at aggravated ASE or higher temperatures compared to conventional SOAs.

Disclosure statement

No potential conflict of interest was reported by the author(s).

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