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A general design method for full-frame area array CCD driving sequence generator based on sequence subdivision and finite state machine

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Abstract: To provide a general design method for a CCD timing drive, a simple CCD driving circuit design is presented. First, the internal structure and working mode of area array CCD485 are introduced, and its basic driving circuit design is given. Then, through the analysis of the driving sequence diagram of area array CCD485, the normal operation of a full-frame large-area array CCD is analyzed. A design method for a universal full-frame array CCD driving timing generator based on time sequence subdivision and a finite state machine is proposed. By grouping the driving timing of the CCD, each group of timing waveforms is divided into several basic output states. In this manner, the driving sequence needed in each working stage of the CCD can be obtained by combining the basic states, which are described by a Moore finite state machine, and the timing driver is modularized. A timing generator supporting the normal operation of a full-frame area array CCD is designed. The specific design of each module for generating the timing is given. The design process of the generator is simple. Finally, a CCD driving timing generator is designed by using Xilinx's Virtex-II Pro series FPGA-XC2VP20 and Xilinx's ISE software platform, and the waveform is simulated and analyzed. The output signal fully meets the driving timing requirements of the 485 chip, which proves the validity of the design method.

Keywords: Data processing methods; Detector modelling and simulations II (electric fields, charge transport, multiplication and induction, pulse formation, electron emission, etc); Timing detectors

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1 Introduction

1.1 Common design method for a full-frame area array CCD driving sequence generator

A CCD must be driven by a peripheral driving circuit to complete the generation, storage, transfer and output of the optical signal charge packet. For an area array CCD, a complete driving circuit system is composed mainly of a timing pulse generator circuit, clock driver circuit, DC bias circuit,

signal preprocessing circuit, and interface circuit, among other components. The driving sequence of a CCD is a set of periodic and complex sequential pulse signals with specific time relations.

The precise driving sequence guarantees the normal and stable operation of a CCD, so how to design a correct and reliable driving sequence circuit for CCDs has become one of the key problems in the application of CCDs. There are many methods for designing the timing pulse generator circuit of a CCD, such as the direct digital circuit driving method, single-chip computer driving method, erasable programmable read-only memory (EPROM) driving method, programmable logic device driving method and special IC driving method. According to the different types of CCDs, different design methods can be adopted.

1.1.1 Single-chip microcomputer generates driving time sequence signal

There are two main methods for generating time series signals with single-chip microprocessors. One is to generate signals directly with single-chip microprocessors, and the other is to generate signals with programmable counters. The former uses one chip to control the level change of the workpiece via programming, generates the driving signal, and realizes the timing requirement of each driving pulse using software delay. The peripheral circuit can be realized by using double flip-flops, counters and other circuits. Pulse width control can be designed with monostable flip-flops. The frequency of the driving signal produced by this method is low because it relies on software delay and takes up all the time of a single-chip computer. Moreover, when monostable flip-flops are used in the circuit, the width of the pulse is determined by the external circuit, and the width of the pulse is not easy to precisely control. The latter uses three timers to generate driving signals, and the time constant is inserted by software. As long as the initialization is completed, the inserted time constant can work. The periphery also needs some separate components to control. It can improve the speed without taking up the time of the single-chip computer, but it has little room to adjust the timing.

1.1.2 EPROM generates driving timing signals

The principle of this method is that the data determined according to the timing requirements are written in advance, the address is generated by a crystal oscillator and counter, the data line outputs the required timing according to the address, and then the clock driving signal is generated by a combination of logical circuits. At the end of one cycle, the counter clears and outputs the clock signal of the next cycle. To change the inverse time, a set of decoding circuits with variable values are used to generate zero-clearing pulses and make the counter zero-clearing. This method is the simplest and easiest when the driving signal and the line cycle are fixed. With this method, the structure of the sequential circuit is simple. When the circuit is debugged, it does not need to adjust the hardware circuit. The relationship between the sequential signals can be adjusted only by rewriting. However, as the number of pixels increases, the amount of data written to the chip and the workload both increase. When the clock frequency is high, the required reading speed is faster, which is not suitable for the design of high-speed sequential circuits.

1.1.3 The digital circuit directly generates the driving timing signal

The time series signals of the camera can be counted by the counter and produced by multiple comparing decoders. At the end of each line, a set of decoding circuits with variable values

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generates a zero-setting pulse, which makes the counter zero-setting and restarts the timing of the next line. According to the value read from the dial switch, the master computer calculates the number of inversion pulses and sends out instructions to change the value of the decoder to advance and postpone the generation time of zero-clearing pulses in order to achieve the goal of synchronization. Direct use of digital circuits can generate high-speed sequential driving signals, but at the cost of the use of separate component designs, the need for more devices, complex hardware circuits, and increased difficulty of debugging since the device can be debugged only once it is made into circuit boards, and once it is modified, the circuit boards must be redesigned. Thus, the method suffers from high cost and a lack of flexibility.

1.1.4 Driving timing signal generated by a field programmable gate array

Field programmable gate arrays (FPGAs) have the general structure of mask programmable gate arrays. They consist of logical function blocks arranged into arrays, and programmable interconnected resources connect these logical function blocks and the corresponding input and output to achieve different designs. FPGAs' device integration is much higher than that of the early traditional devices, and they have certain advantages in terms of speed. In the environment of programmable logic integrated development, many methods, such as schematic input, civil design input and waveform design input, can be used to establish the design input. Through front and back simulation, the errors are checked, the logic synthesis is performed and the device adaptation is selected. By using the method of generating a time series signal, the electricity is greatly reduced.

The volume of the circuit board shortens the delay of the device, reduces the power consumption of the circuit and increases the reliability. In the schematic design phase, this method can grasp whether the circuit is correct, design flexibly, debug conveniently, improve efficiency and save cost.

1.2 Main problems of using an FPGA as a sequence driver generator

Because the driving sequences of different manufacturers and models of CCD devices are different, it is difficult to standardize and produce the driving circuit of a CCD. The design of the driving circuit of a CCD is one of the key technologies in the application of CCDs. Only when the driving and controlling pulses cooperate well with the CCD can the photoelectric conversion characteristics of the CCD be brought into full play and stable and reliable photoelectric signals be output. The driving sequence of a high-resolution large-area array CCD camera system has a large number of time series signals, which are between each time sequence. Because of the complex relationship, high precision and high working frequency, the design of the time sequence generator is very difficult. Programmable logic devices are very suitable to serve as the timing generator of CCDs because of their high integration, high speed, good reliability and repeatable programming. At present, there are many reports about programmable logic devices as CCD timing generators [8, 9], but most of them are descriptions of the overall structure design and the final results, and the details of the implementation are basically not disclosed. Therefore, camera developers can only design the code for each specific CCD and need a universal design framework to quickly and efficiently design sequential generators. The purpose of this paper is to solve this problem.

1.3 The main contributions of this article

Aiming at the periodicity of a CCD driving sequence, a simple and general design method for CCD driving sequence generators is proposed. First, the driving sequence of a CCD is grouped, and the

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waveform of each sequence is divided into several basic output states, such that the driving sequence needed in each working stage of the CCD can be combined by each basic state. Then, the design process of the timing generator is simplified by using a Mohr finite state machine. This method can make the design process of the sequential generator simpler, greatly reduce the development difficulty of developers, and reduce the cost of developing sequential driving circuits . By using this method, both the time sequence and the time delay can meet the requirements of high frequency and high precision, and the operation is stable and reliable. The design method introduced in this paper is especially suitable for the timing design of high-speed and high-sensitivity area array CCDs. It has a certain reference significance for researchers who design timing driving circuits for CCDs. This method can effectively reduce the area of printed circuit boards, simplify the design, reduce the size of the circuit and save the cost of hardware design.

2 Introduction of full-frame area array CCD485 and the design of its driving circuit

2.1 Internal structure and working mode of full-frame area array CCD485

Area array CCD485 is a full-frame area array CCD image sensor produced by Fairchild Company. The number of pixels reaches 4096×4097, and the sensitive area is $61.2\,\text{mm} \times 61.2\,\text{mm}$. The optical effective pixels are 4080×4081, each of which has eight columns with eight behavioral optical dark pixels each, and the filling factor is close to 100%. As is shown in figure 1.

Figure 1. Dimensions of array CCD485.

Figure 2 shows the structure of the area array CCD485 CCD, which consists of an image array, a horizontal register and an output amplifier. The photosensitive region occupies the vast majority of the whole CCD area, and there are several electrodes arranged tightly across the whole array. Under the photosensitive region, there are horizontal output registers, which are composed of vertically arranged electrodes covered with a light-shielding layer. At the end of the horizontal register, there are output amplifiers. There is an independent horizontal electrode between the photosensitive region and the horizontal register, which can isolate the photosensitive region and the horizontal register. This electrode is called the transfer gate. It is mainly used to realize the charge vertical sampling output of the CCD. The summing gate between the output amplifier and the horizontal transfer register is mainly used for horizontal pixel merging (binning) of the output image of the CCD [2, 3].

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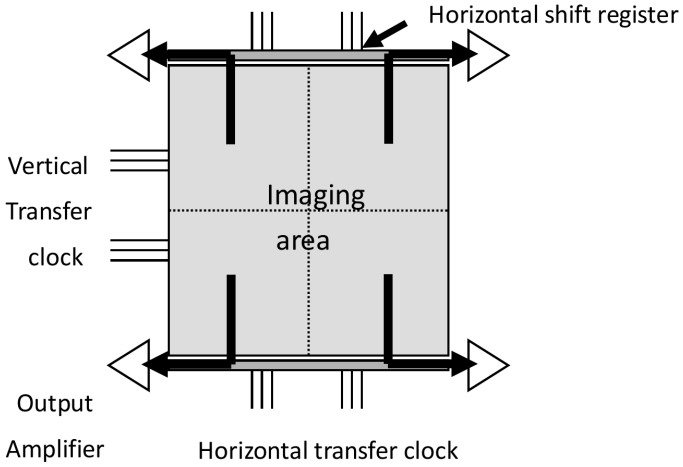

Figure 2. Plane array CCD485 structure and basic timing.

A CCD must be driven by a peripheral driving circuit to work properly. For full-frame array CCDs, the basic driving circuit system is composed mainly of a timing pulse generator circuit, clock driving circuit, DC bias circuit and signal preprocessing circuit, as shown in figure 3 [6, 7].

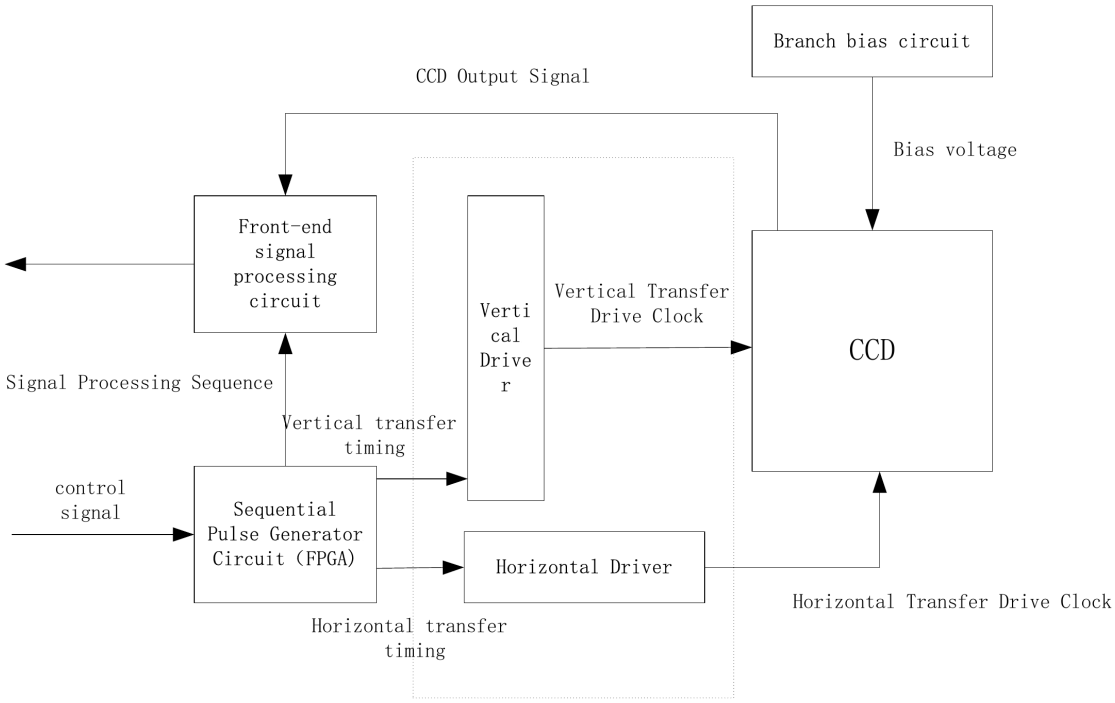

Figure 3. CCD driving circuit block diagram.

Correct driving timing guarantees normal and stable operation of the CCD device, so how to design a correct and reliable timing circuit for CCDs has become one of the key issues in the application of CCDs. There are many methods for designing timing pulse generator circuits of CCDs, such as the direct digital circuit driving method, single-chip computer driving method, EPROM driving method, programmable logic device driving method and special IC driving method.

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The core controller of these units is the FPGA, whose function is to generate the most basic driving signal timing required by the CCD. The FPGA includes clock management, timing generation, duty cycle control and power-on sequencing. This scheme uses Xilinx's Virtex-II Pro series of FPGA-XC2VP20, which is a high-performance processor with abundant resources to complete all control functions in image acquisition and image compression systems [8].

When the mechanical shutter opens, the photosensitive unit of the area array CCD is sensitizing the light without charge transfer, so there is no need to output the driving signal; when the mechanical shutter is completely closed, the four quadrants simultaneously output the driving signal and remove all the photogenerated charges, that is, collect an image. The basic time sequence of vertical and horizontal transfer signals needed for charge transfer of the CCD is generated by the FPGA; however, the high level of the output driving signal of the FPGA is only +3.3 V, and the load capacity is poor. Therefore, the main function of voltage modulation of the horizontal and vertical signals is to generate the basic time of the FPGA. The sequence signal is modulated to the level required by the CCD. At the same time, the driving pulse generated by the FPGA is converted into a pulse signal with strong driving ability, which is eventually output to the CCD. The power supply unit of the CCD provides the working voltage and modulation voltage to the CCD [9, 10].

2.2 Driving signal analysis

There are five main types of driving signals for area array CCD485:

1. ΦV1, ΦV2, and ΦV3 are vertical transport clocks. These clocks need to satisfy the principle of overlapping driving of a three-phase drive. After optical integration, the charge in each row of pixels is transferred vertically to the horizontal shift register driven by the three-phase vertical transfer clock.

2. ΦVTG is the vertical transfer gate. During vertical transfer, charges accumulated in the last row of pixels in the photosensitive area adjacent to the horizontal shift register are removed from the photosensitive area and moved into the horizontal shift register.

3. ΦH1, ΦH2, and ΦH3 are vertical transport clocks. These clocks also need to satisfy the overlapping driving principle of a three-phase drive. At the end of the vertical transfer period of each line, the charge in the horizontal shift register shifts horizontally to the output amplifier driven by the three-phase horizontal transfer clock.

4. ΦRG is the reset clock. During its high-level period, the field-effect transistor in the output structure of the CCD is turned on, and the residual charge of the former pixel is removed such that the potential of the output port can be restored to the initial high level.

5. ΦSG is the summing gate. The additive potential well adjacent to the last cell of the horizontal shift register is controlled. The charge of one or more adjacent pixels is accumulated and then output to the output amplifier as a charge.

Since the array CCD485 is divided into four quadrants, upper left (UL), upper right (UR), lower left (LL) and lower right (LR), the five driving signals are symmetrically distributed in these four quadrants. Among them, V and VTG are divided into UP and LOW, which control the upper

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and lower half of the CCD, respectively; H, RG and SG are divided into UL, UR, LL and LR, which control the upper left, upper right, lower left and lower right quadrants of the CCD, respectively. The total number of driving signals of CCD485 is 132 [11, 12].

The working cycle of full-frame array CCD485 can be divided into three stages: the exposure stage, vertical transfer stage and horizontal transfer stage. In the light exposure stage, the photosensitive unit array in the imaging area receives photogenerated charge; i.e., an image is captured in the imaging area, and the exposure time is controlled by the mechanical shutter. In the vertical transfer stage, the photogenerated charges in each row are transferred to the horizontal shift register. In the horizontal transfer stage, the photogenerated charges in the horizontal shift register transfer to the output end one by one and are finally converted to the voltage output by the amplifier. When the full-frame image is removed, all transmission clocks are closed. If continuous photography is required, the mechanical shutter is opened again to enter the exposure stage, and the above process is repeated. Among these clocks, V1, V2, V3, H1, H2 and H3 must meet the requirements of the overlapping driving principle of a three-phase drive when the charge is transferred vertically or horizontally by the CCD. The driving signal timing of area array CCD485 is shown in figure 4.

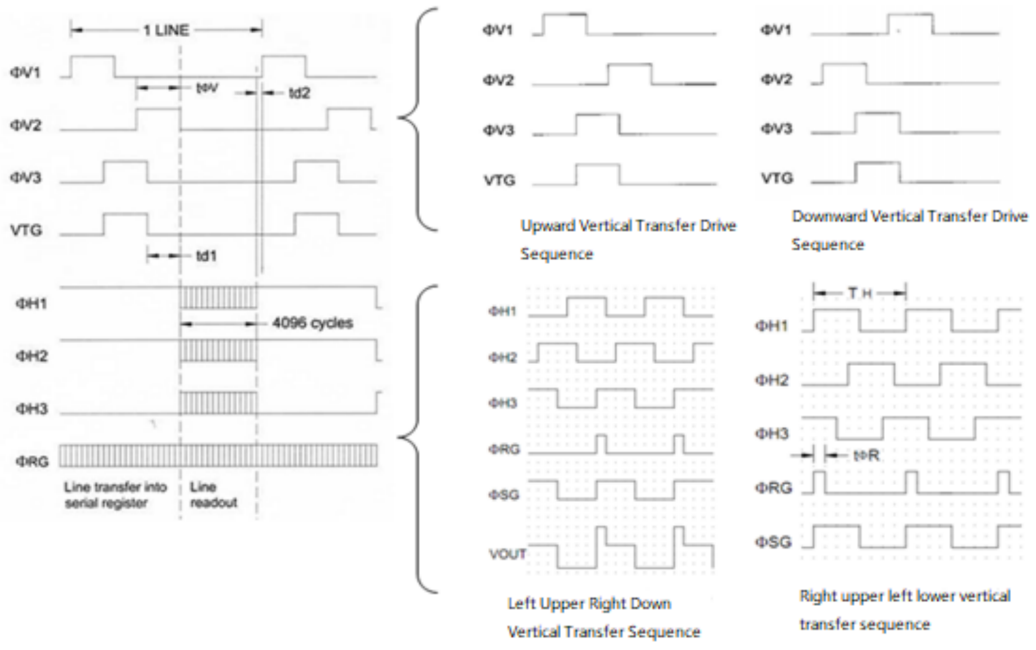

Figure 4. The driving signal sequence of area array CCD485.

3 Design and implementation of a driving sequence generator based on time sequence subdivision and a finite state machine

The design of timing generators for high-resolution large-area array CCD camera systems is difficult. When there is no special chip available for the CCD or a special chip cannot meet the demands, this chip must be designed independently. It is a better choice to use programmable logic devices than special chips for implementation. Next, a simple design method is proposed.

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3.1 Modular partitioning

From the previous analysis of the full-frame CCD timing, we can see that the timing can be divided into three groups:

a) High-frequency sequential pulses closely related to horizontal pixel transfer, mainly including H1-H3, SG, RG, SHP, SHD, CLKADC and CLKP; the phase relationship of each signal must be accurate.

b) Clocks related to vertical row transfer, mainly including V1-V3 and TG.

c) Clocks related to the output state of the CCD, including line clock signal HD and frame clock signal VD.

In circuit design, the top-down design method is used to generate different groups of timing signals with different modules. The circuit is divided into six modules: the bus interface module (3-wire bus interface), control module (controller), high-frequency timing generation module (H-Gen), vertical row transfer timing generation module (V-Gen), main clock generation module (CLK-Gen) and image timing generation module (S-Gen), as shown in figure 5 [13].

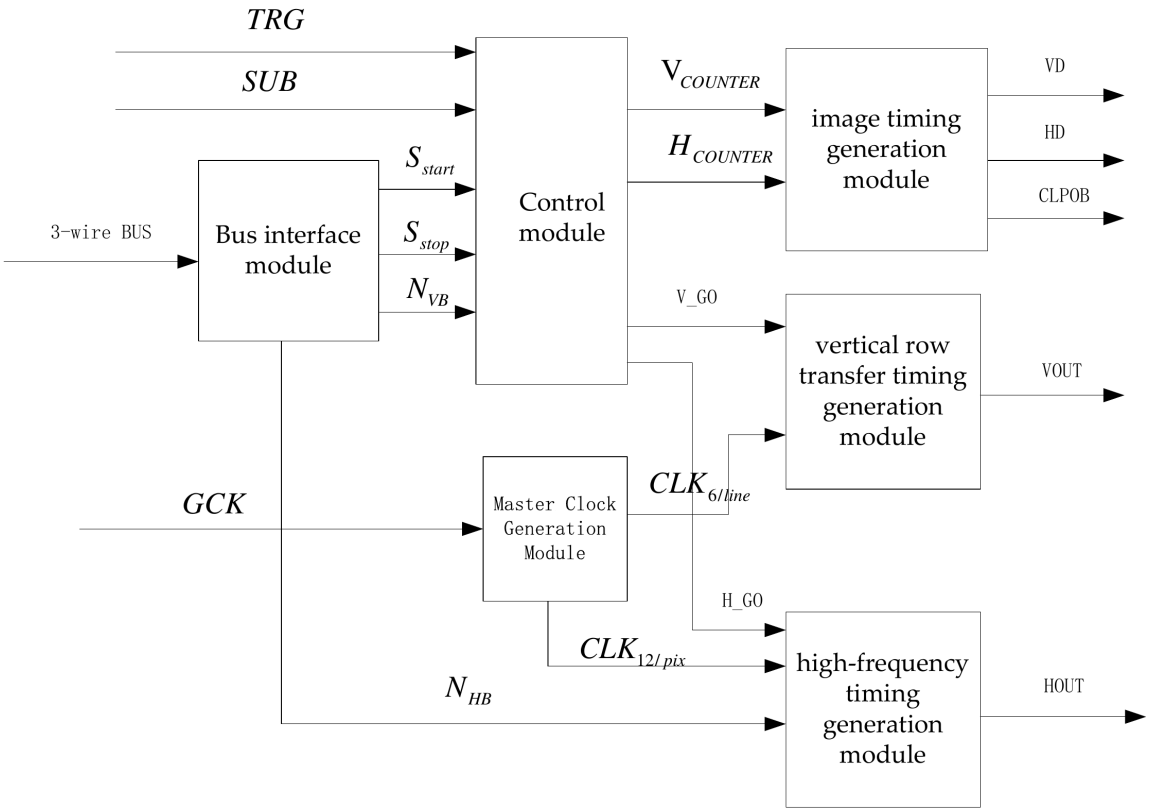

Figure 5. The modular division of the timing generator.

3.2 Design and implementation of each module

3.2.1 Bus interface module

The 3-wire bus is used to receive some variable parameters, such as the start and end position of the window when the window is output, the number of vertical binning rows NVB and the number of horizontal binning pixels NHB. The module converts the serial input data into parallel parameters and stores them in different registers according to their addresses.

3.2.2 Design of the high-frequency sequence generation module

The output waveform can be divided into several states according to the phase relationship of each clock. Figure 6 shows the results of the division of the above high-frequency driving sequence. The waveform is divided into 13 basic output states [14].

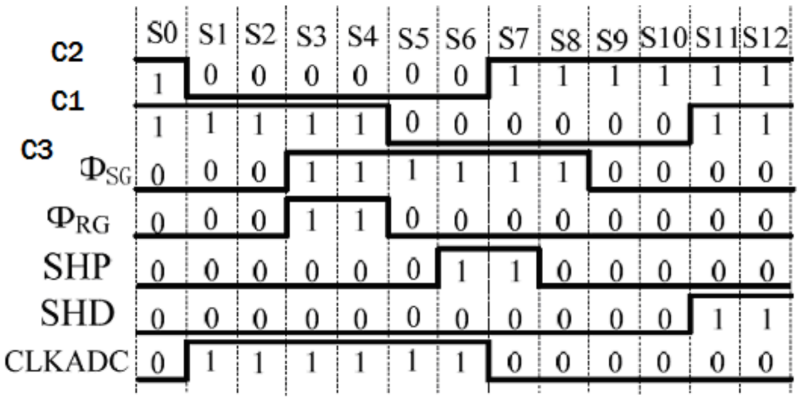

Figure 6. The timing segments of the pixel clock module.

All types of high-frequency driving timing pulses needed by an operating CCD are composed of the above 13 basic states: when the CCD performs vertical row transfer, it outputs the signal of the S0 state; when horizontal pixel transfer is performed, it continuously outputs the signals of S1~S12 in turn, and every output cycle completes a horizontal pixel transfer. A Moore finite state machine can be used to describe the working process of the pixel clock generator module, as shown in figure 6. The clock signals of each state are represented together by an 8-bit logic vector, HOUT [15].

The transfer relationship of each state is determined by the control signals GoLineTransfer and GoPixTransfer: GoLineTransfer equaling 1 indicates that the CCD is in the vertical line transfer stage and that the circuit enters the S0 state and outputs the driving clock needed for the vertical line transfer; GoPixTransfer equaling 1 indicates that the CCD is in the horizontal pixel transfer stage and that the circuit advances in turn. In the states S1 ~ S12, the driving sequence required for horizontal pixel transfer is generated by continuous cycling. The transfer of each state is triggered by the external clock CLK12fpix, whose frequency is 12 times that of the pixel clock fpix. To achieve horizontal pixel merging, a counter is needed to count the output H3 signal and then generate the SG signal. The overflow value of the counter is determined by the merged pixel number NHB [16]. As is shown in figure 7.

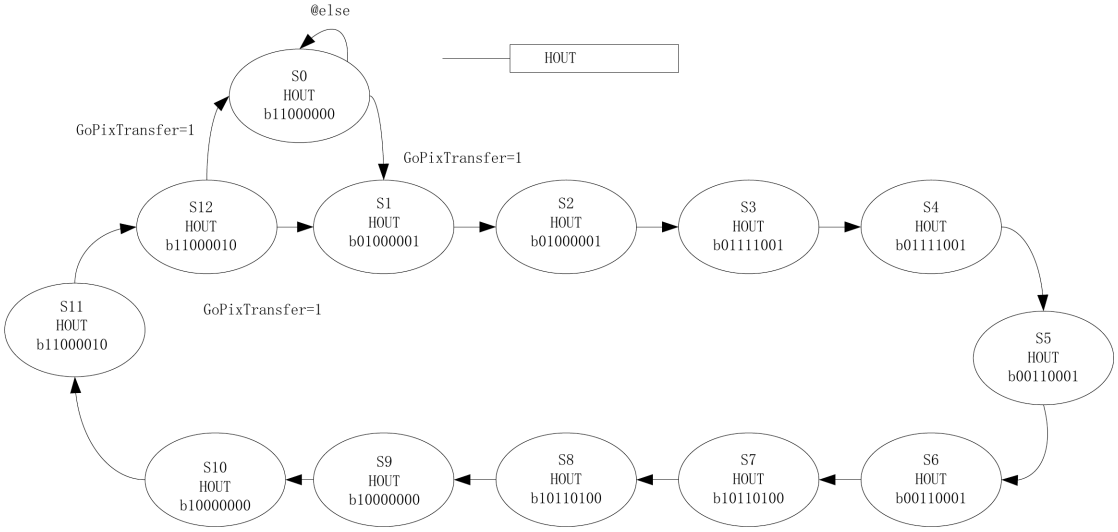

Figure 7. Pixel clock generation module for the description of a finite state machine.

3.2.3 Design of the vertical row transfer timing generation module

The module is used to generate the driving sequence of photosensitive area electrodes needed for vertical row transfer of the CCD. According to the design concept of the pixel clock generating module, the waveform is subdivided. The subdivision results are shown in figure 8.

The timing signal of electrode driving in the photosensitive region of the CCD is composed of the above eight basic states: the signal of the SS state is output when idle, the signal of the S0 state is output during optical integration and horizontal pixel transfer, and the signals of S1~S6 are output continuously and sequentially when vertical line transfer occurs. During every output cycle, the signals of S1~S6 are completed vertically. Line transfer is also described by a Mohr-type finite state machine, as shown in figure 8b. The transfer relationship of each state is determined by three control signals: GoIdle is 1 when the CCD is idle, GoPixTransfer is 1 when optical integration or horizontal pixel transfer is performed, and GoLineTransfer is 1 when vertical row transfer is performed. The transfer of states is triggered by CLK6fline, which is six times the line transfer frequency. In the charge transfer output of the CCD, only GoLineTransfer and GoPixTransfer need to be made to 1 in turn so that the CCD can be transferred horizontally after vertical transfer of a row. If M-pixel merging in the vertical direction is to be realized, only the effective time of GoLineTransfer is prolonged, so the CCD transfers the M-row continuously and then performs horizontal pixel transfer [17].

3.2.4 Design of the main clock generator module

The main clocks are CLK12fpix and CLK6fline. CLK12fpix is provided by the external clock source GCK, and CLK6fline is obtained by frequency division. If the CLK12fpix frequency is high, the PLL (Altera's FPGA) or DCM (Xilinx's FPGA) hardware resources can be used to multiply the frequency.

3.2.5 Design of the control module

The control module is used to control the coordination of each module. The working process of the CCD is divided into five basic states: idle, optical integration, vertical row transfer, horizontal

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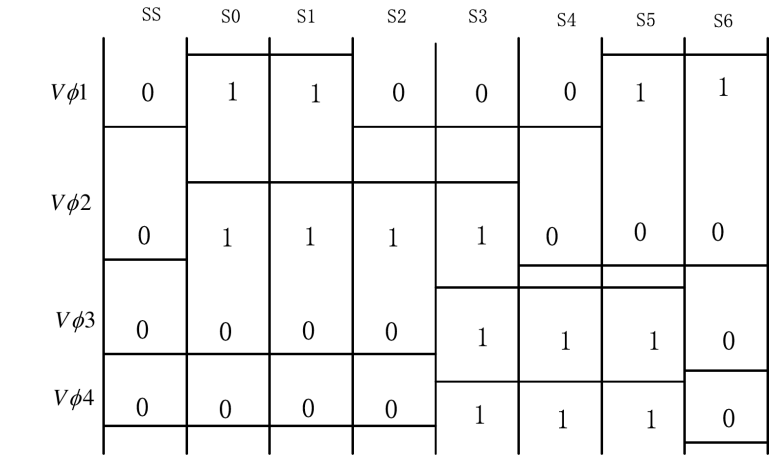
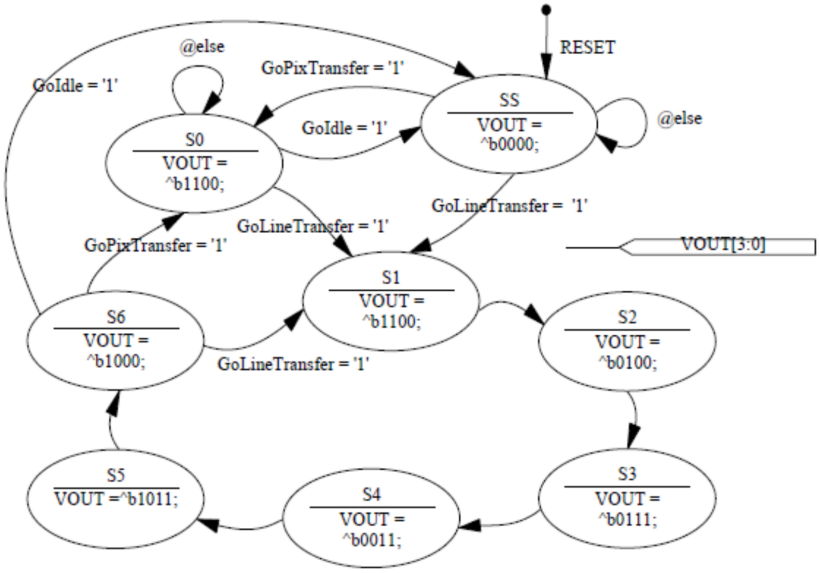


(a)



(b)

Figure 8. Vertical line transfer clock module timing subdivision and the state machine description.

pixel transfer and fast erasure. After the camera is turned on, the CCD enters the idle state; after receiving the shooting instructions, it enters the optical integration state, transfers and outputs the charge packet after reaching the prescribed integration time, and continuously circulates between the two states of vertical line transfer and horizontal pixel transfer. After all line output is completed, it enters the idle state. If the window output of the image is to be performed, the image will be erased quickly in the charge packet transfer process, and the unnecessary rows will be erased quickly. If vertical M-pixel merging is to be realized, horizontal pixel transfer will be performed after continuous vertical M-line transfer during the charge packet transfer process. This process can be described by a finite state machine, as shown in figure 9 [18].

The external control signals provided to the module mainly include optical integration start and stop trigger signal TRG and window output control signal SUB. In addition to Sstart, Sstop and NVB provided by the bus interface, the required operating parameters include row number NL and column number NP of the CCD.

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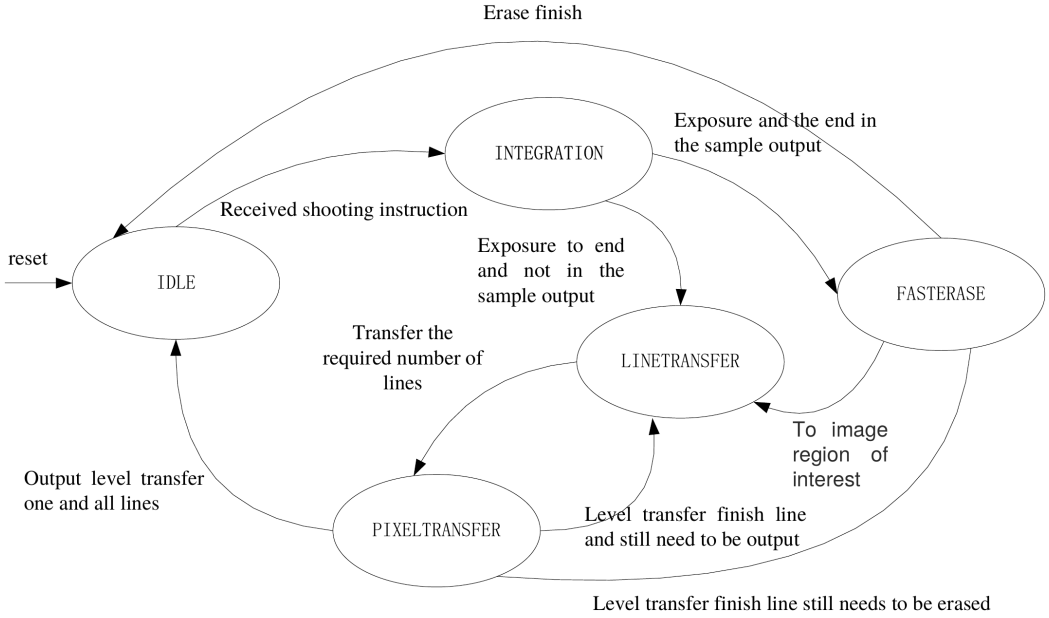

Figure 9. Control module state transition diagram.

Three counters are designed in the module: (1) the NL counter counts the falling edge of V3, and VCOUNTER counts the number of transferred rows; (2) the NP counter counts the falling edge of H3, and HCOUNTER counts the number of transferred pixels in a row; and (3) the NVB counter counts the falling edge of V3. During the count, the count value BCOUNTER is the number of rows that have been merged. The transition conditions of each state are specified in table 1.

Table 1. Specific Description of State Transition Conditions of Control Modules.

Condition	Concrete expression
Receive shooting instructions	TRG = 1
Exposure ended without window output	TRG = 0 & SUB = 0
Number of rows transferred	$B_{\mathrm{COUNTER}} = N_{\mathrm{VB}}$
Horizontal transfer of one line and output of another line	(SUB = 0 & $H_{\mathrm{COUNTER}} = N_p$ & $V_{\mathrm{COUNTER}} < N_L$) || (SUB = 1 & $H_{\mathrm{COUNTER}} = N_p$ & $V_{\mathrm{COUNTER}} < S_{\mathrm{stop}}$)
Horizontal transfer of one line and output of another line	$H_{\mathrm{COUNTER}} = N_p$ & $V_{\mathrm{COUNTER}} = N_L$
Exposure end and window output	TRG = 0 & SUB = 1
Arriving at the region of interest	$V_{\mathrm{COUNTER}} = S_{\mathrm{start}}$
Horizontal transfer completed one line and there are still lines to erase	SUB = 1 & $H_{\mathrm{COUNTER}} = N_p$ & $S_{\mathrm{stop}} \leq V_{\mathrm{COUNTER}} < N_L$
Erase completed	$V_{\mathrm{COUNTER}} = N_L$

The output signal of the control module mainly includes the control signal that controls the working state of the high-frequency sequential generator module.

H_GoLine Transfer, H_GoPixTransfer and the control signals V_GoIdle, V_GoLineTransfer and V_GoPixTransfer control the working state of the vertical line transfer timing generation module. The values of the output signals in each state are reported in table 2.

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Table 2. Output value of each state of control module.

	IDLE	INTEGRATION	LINETRANSFER	PIXELTRANSFER	FASTERASE
H_GoLineTransfer	0	0	1	0	0
H_GoPixTransfer	1	1	0	1	1
V_GoIdle	1	0	0	0	0
V_GoLineTransfer	0	0	1	0	1
V_GoPixTransfer	0	1	0	1	0

3.2.6 Design of the image sequence generation module

This module is used to generate line clock signal HD, frame clock signal VD and black level compensation control signal CLPOB. These three signals are directly related to the line counter and pixel counter. When the value of VCOUNTER or HCOUNTER reaches the preset range, the corresponding signals are generated.

3.2.7 Integration and integrated realization of modules

At present, many EDA development tools support the use of finite state machines for top-level input, such as StateCAD in Xilinx ISE. The state machines of each module are input into the StateCAD separately and converted into the integrated VHDL. The main clock generating module and the image timing generating module are directly described by the VHDL and are finally synthesized and realized [19].

Using the method proposed in this section to design timing generators has high versatility and flexibility: modifying each shape. The output value of the state can change the waveform and the relationship of the time series, the number of output signals can be expanded by increasing the bit width of the output value, and the time resolution can be improved by increasing the number of states of the waveform partition. The main disadvantage is that the greater the number of state partitions, the more device resources needed and the higher the main clock frequency required to generate signals of the same frequency

4 Design and simulation of the driving signal

4.1 Driving signal simulation

With the ISE8.2 development software from Xilinx Company, the internal function modules of the FPGA shown in figure 5 are described by the VHDL. The top-down development method is adopted to realize the design of high-level complex logic, which makes the logic relationship very clear and reduces the complexity of logic design, thus realizing the hardware design.

The FPGA generates the most basic driving signals needed for charge transfer of the CCD, including vertical signals (PV1, PV2, PV3 and PVTG) and horizontal signals (PH1, PH2, PH3, PRG and PSG). The driving signals of CCD485 are divided into five categories, totaling 132 signals. Using an external active crystal oscillator as a clock input, the basic driving signal timing required by the CCD is obtained by frequency division and counting. All driving signal timing is integrated into one module for description. By changing the value of the counter, the frequency and duty cycle of each signal timing can be changed conveniently.

The design process is to divide the external clock signal into 10 MHz horizontal signal sequence PH, count the PH cycle, and calculate the time needed to transfer a row of pixels. Because each row of effective pixels has eight optical dark pixels at the beginning and end of the row , the output time of a row is at least 8 + 4080 + 8 = 4096 PH, which is also because the output time of each row is 8+4080+8 = 4096 PH. For two ports of the same horizontal shift register to output simultaneously, it takes 2048 PH to output one line of pixels. Similarly, the time needed to transfer a frame pixel is calculated by counting the period of PV, which is one line of time. Since there are eight lines of dark optical pixels in each frame, the output time of a frame pixel is at least 8 + 4081 + 8 = 4097 lines because there are two horizontal shift registers that can output at the same time. It takes at least 2049 lines to output a frame of pixels by outputting 2048 lines followed by another 2049 lines. The horizontal and vertical signal timing are tested using the ModelSim SE simulation software. The simulation results for the horizontal signal timing are shown in figure 10, and the simulation results for vertical signal timing are presented in figure 11. In the simulation results, the label behind the signal represents the position of the CCD where the signal is located; UL represents the upper-left part, ur represents the upper-right part, ll represents the lower-left part, LR represents the lower-right part, up represents the upper half, and low represents the lower half. Trig_in is a timing trigger signal. Low level represents the opening of the mechanical shutter, and high level represents the closing of the mechanical shutter. Closing the shutter generates a frame driving signal sequence, removes all photogenerated charges, and collects the image information from one frame [20, 21].

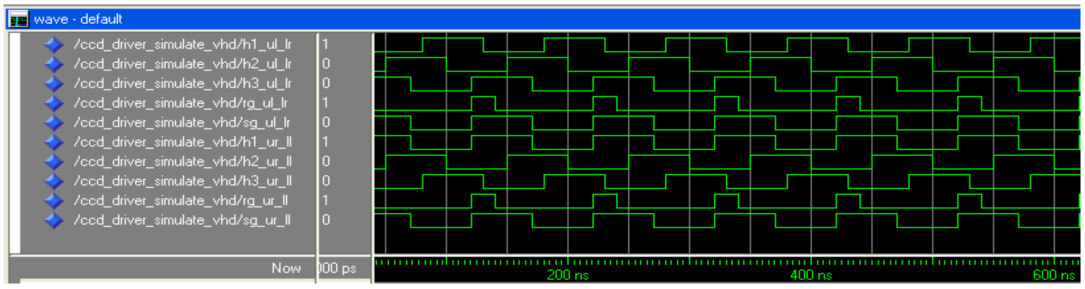

Figure 10. The sequential emulation of the horizontal signal.

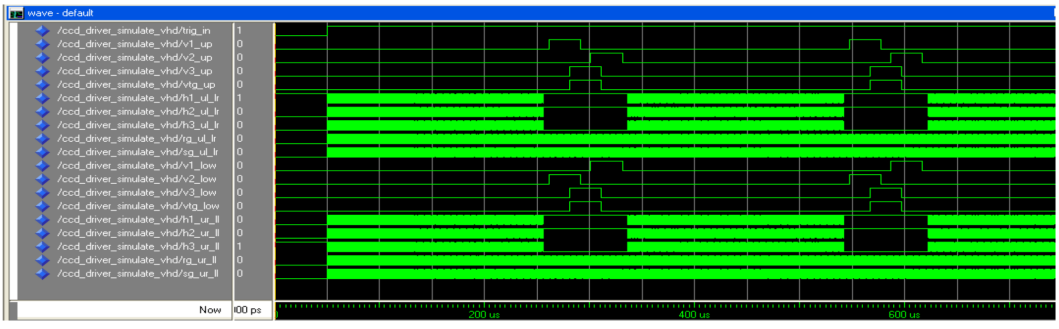

Figure 11. The sequential emulation of the vertical signal.

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4.2 CCD driving sequence test

After the program ImageJTAG is downloaded to EPCS, the software test of the restart and reset of the FPGA is performed. After power-on, the FPGA resets through RESET keys, drives each module and processes the collected data at the same time. The timing of the CCD drive is the key part of the whole system, so the signal-receiving pin of the CCD drive is tested using an oscilloscope probe [22, 23]. The real video signal voltage is the difference between the reference level and the video level [24]. The waveform is shown in figure 12.

First, all the power supply voltage and driving signal voltage and timing of the CCD are detected. If upper array CCD485 is connected normally, the analog video signal output by CCD485 is measured by an oscilloscope [25–27]. Figure 13 displays the analog signal waveform of the driving signal RG, SG and corresponding pixels. The analog signal of the CCD includes the reset level and reference level. The real video signal voltage is the difference between the reference level and the video level. Under full exposure, the maximum output video saturation voltage of CCD485 is 1V,which meets the performance index [28, 29]. Figure 14 presents a row of pixels of the output signal of the CCD. The right side of the CCD is occluded by a cover. From the video signal, it can be observed that the right side of the video signal is low and the response of the CCD is good.

5 Conclusion

First, the internal structure, working mode and driving sequence of area array CCD485 are introduced, and the basic driving circuit design is given. Aiming at the periodicity of the driving sequence of a CCD, a simple and general design method for a CCD driving sequence generator is proposed. First, the driving sequence of the CCD is grouped, and the waveform of each sequence is divided into several basic output states such that the driving sequence needed in each working stage of the CCD can be obtained by combining each basic state. Then, the design process of the timing generator is simplified using a Moore finite state machine. The method presented in this paper has high versatility and flexibility: modifying the output value of each state can change the waveform and interrelationship of the time series, increasing the bit width of the output value can expand the number of output signals, and increasing the number of states of waveform division can improve the time resolution. The main disadvantage of this method is that the greater the number of state partitions, the more device resources needed and the higher the main clock frequency required to generate signals of the same frequency. Finally, using the Virtex-II Pro Series FPGA-XC2VP20 from Xilinx Company and the ISE8.2 development software from Xilinx Company, a waveform simulation is performed using ModelSim. The waveform diagram fully meets the timing requirements, which proves the validity of the timing design method for array CCDs.

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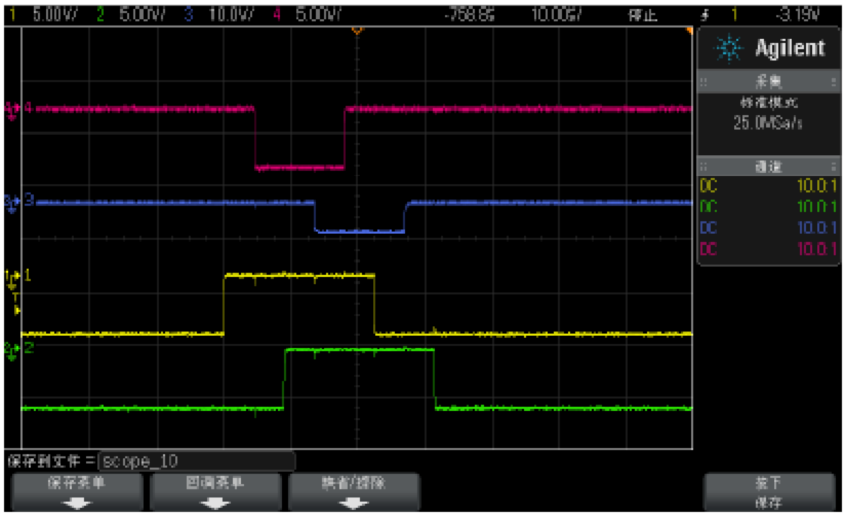
(a) A frame start signal waveform.

(b) Frame period drive waveform.



(c) Line periodic driving waveform.

Figure 12. Actual measurement of driving oscilloscope.

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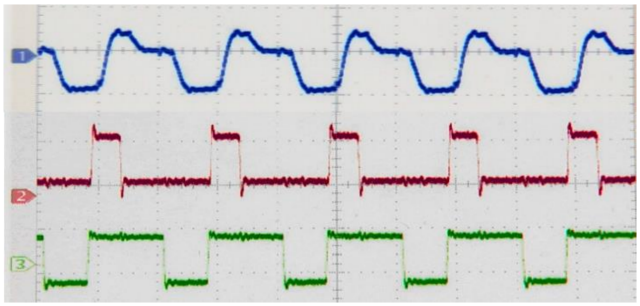

Figure 13. The analog video signal of some CCD pixels.

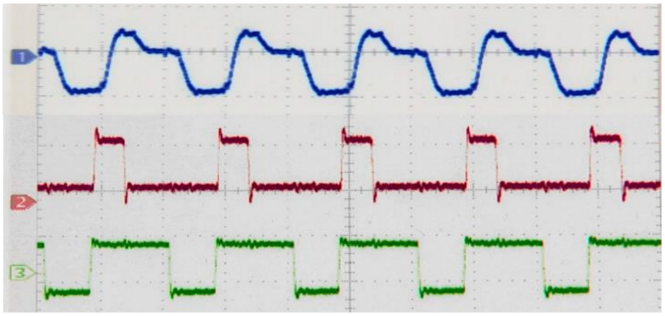

Figure 14. The analog video signal of a line CCD pixels.

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