20 August 2019

Design of a high frame rate driver circuit for a 22 M-pixel high-resolution large-area array CCD camera and its nonuniformity correction

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Optical Engineering, 58(8) (/journals/optical-engineering/volume-58/issue-8), 083104 (2019).
https://www.proxydgb.buap.mx:2168/10.1117/1.OE.58.8.083104
(https://www.proxydgb.buap.mx:2168/10.1117/1.OE.58.8.083104)

Abstract

When using a high-resolution full-frame area array charge-coupled device (CCD) FTF4052M as the aerial image sensor of a camera, the frame rate is generally below 1 frame / second (fps), which cannot meet the requirements of applications with high frame rates. First, the FTF4052M drive circuit is introduced. Next, an improved driver circuit of the CCD 4052M is proposed. Using the CCD to output four amplifiers simultaneously yielded a maximum frame rate of 3.4 fps. Then, the timing of the CCD driver, the front-end processing circuit, the DC bias circuit, and the interface circuit of the four outputs are designed. The improved driver circuit could meet the application requirements of various aerial cameras. In addition, the FTF4052M nonuniformity is analyzed, and a nonuniformity response detection system is established. Using this system, the FTF4052M array's nonuniformity among the four quadrants and among the pixels is tested. Based on the CCD's linear responsivity, two correction algorithms are proposed to correct the nonuniformity. Finally, using the correction, the four quadrants' standard deviations of the response sensitivity are reduced by a factor of 1 / 13, and the responsive nonuniformity among all pixels is reduced by a factor of 1 / 10. Through the reshooting of the identified rate board, it is found that the nonuniformity of the CCD array is markedly improved.

< Previous Article (/journals/optical-engineering/volume-58/issue-8/083103/Fusion-of-interpolated-frames-superresolution-in-the-presence-of-atmospheric/10.1117/1.OE.58.8.083103.fu | Next Article (/journals/optical-engineering/volume-58/issue-8/083105/High-throughput-outdoor-characterization-of-photovoltaic-modules-by-moving-electroluminescence/10.1117/1.OE.58.8.08 >

1. Introduction

1.1. General Method for Increasing the Frame Frequency of a Full-Frame Type Area Array CCD

The general methods for increasing the frame frequency of a full-frame area array charge-coupled device (CCD) are as follows: the method of increasing the driving clock frequency of the CCD; the binning method; the image window output method; and the multiple parallel outputs method.[1] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r1)

The method of increasing the driving clock frequency of the CCD: The greatest limitation of this method is that the frame frequency of the CCD cannot be greatly improved. This is because when the driving clock frequency of the CCD exceeds a certain value, the full well capacity and charge transfer efficiency will decrease sharply. The limit frequency of the vertical transfer drive clock in the photosensitive region is mainly limited by the equivalent RC time constant of the electrode, while the upper limit frequency of the horizontal transfer drive clock is mainly limited by the inherent time when the charge is transferred from one electrode to another.

The merge pixel method: The most significant disadvantage of this method is that it will reduce the spatial resolution of the CCD; thus, it cannot be applied when the CCD resolution needs to be maintained.[2] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r2)

Window output method: Although this method can greatly improve the frame rate of the CCD, its most significant disadvantage is that it cannot acquire a complete full-frame image[3] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r3) or be applied when a large-format image needs to be captured.

The multichannel parallel output technology overcomes the shortcomings of the pixel merging method and the image window output and greatly increases the frame frequency; thus, this technology has been widely used. However, it also has disadvantages. The most serious of these is that when the output images of the various channels are spliced together, obvious splicing marks can be observed, which can make the image produce "seam noise."[4] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r4) Second, multiple signal processing circuits are used in the system to process the signal's output via the CCD in parallel, which complicates the system.[1] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r1),[2] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r2)

1.2. Common Nonuniformity Correction Algorithm

Currently, the nonuniformity correction algorithm mainly corrects the nonuniformity of solid image sensor pixels, such as infrared focal plane arrays and low-light CCDs.[5] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r5) The correction methods are divided into two categories: calibration-based and scene-based correction. The basis for the calibration-based nonuniformity correction is to assume that the response characteristics of the pixel do not vary over a period of time.[6] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r6),[7] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r7) The response output of each detector element of the sensor array is calibrated in advance using a calibration radiation source (usually a blackbody radiation source). The basis of the calibration-based nonuniformity correction is to assume that the response characteristics of the pixels do not vary over a period of time. This steadiness with time is a prerequisite for the calibration-based nonuniformity correction. This detail is mentioned in Refs. 6 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r6) and 7 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r7).

The correction coefficient of each pixel is calculated, the output of each pixel is made consistent, and the correction coefficient is recorded to perform the same correction on the subsequently acquired image.[8] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r8) The main options for this correction method include the single-point correction method, the two-point correction method, the multipoint correction method, and the polynomial fitting algorithm.[9] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r9) Scene-based calibration is useful only for quickly varying sensors, such as microbolometers, or in the case of vicarious calibration, i.e., when there is no time for a thorough ground-based calibration such as for a space mission.[4] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r4)

Although the scene-based correction method has been extensively studied and has made great progress, in actual imaging systems, especially when real-time corrections are performed using hardware circuits,[10] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r10) the calibration method (based on calibration) is still the most robust image sensor in terms of nonuniformity.[11] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-

a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r11) The method of calibration most widely used is the two-point calibration method because it has a simple algorithm, easy hardware implementation, and good correction effect; in addition, it is suitable for correcting all linear systems due to its mathematical nature.[1] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r1) Within the linear output range of the CCD, each output channel can be linear; thus, the nonuniformity of the output channel can be corrected using the two-point calibration method.

1.3. Main Contributions of this Article

Regarding the structural characteristics of the FTF4052M, this paper proposes a method to improve the basic driving circuit by making full use of its four output amplifiers for a simultaneous output to achieve the maximum readout rate and overcome the camera frame frequency of the current FTF4052M, with few disadvantages. In this paper, the causes of the nonuniformity of the full-frame area array CCD are analyzed, and a response nonuniformity detection system is established. The nonuniformity between the four quadrants of the area array CCDFTF4052M is detected by the system. Based on the linearity of the area array CCD, a two-point correction algorithm is proposed, and the nonuniformity is corrected. Finally, the performance of the correction algorithm is analyzed, and a comparison of the response nonuniformity before and after correction is given.

2. Hardware Design

2.1. Overall Design Scheme of the FTF4052M Drive System

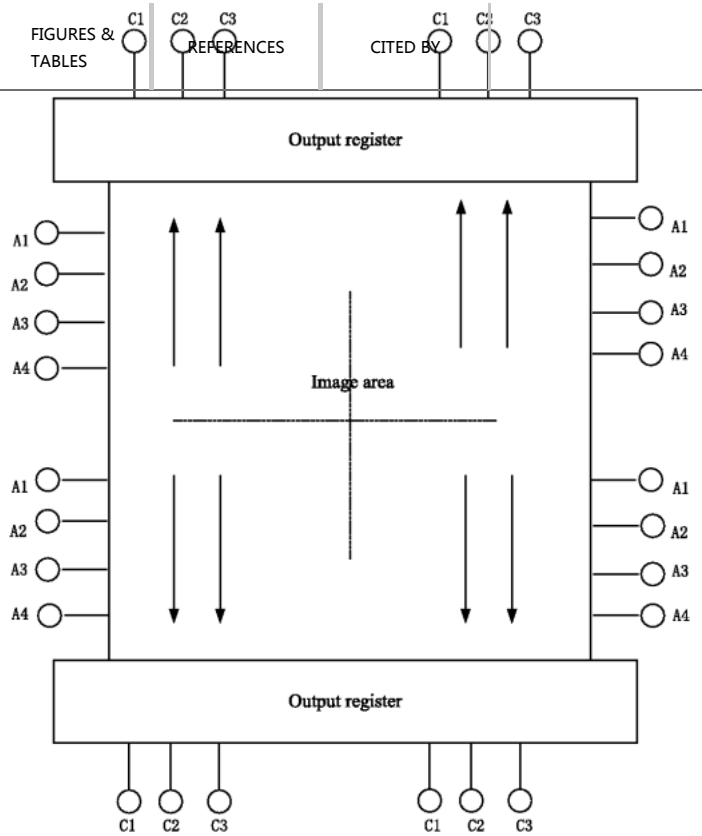
2.1.1. Introduction of FTF4052M

Large-area array CCDs have a wide range of applications in areas such as aerial photography, digital photo studios, medical biochemistry, and national defense, all of which require high resolution and high image quality. This article selects a 22 M-pixel camera produced by Canada's DALSA company. The FTF4052M is a 22 M-pixel -full-frame CCD image sensor with a vertical antiblooming structure, a large-area array (*[Math Processing Error]*), a high resolution (*[Math Processing Error]*), a high fill factor (100%), a large dynamic range (*[Math Processing Error]*), a fast pixel output (up to 27 MHz), and a high charge transfer efficiency (0.999999); thus, it is a suitable image sensor for scientific cameras. This CCD has low noise, a stable output, and stable imaging. It is thus suitable as an image sensor for scientific cameras. Based on the price, technical maturity, and project requirements (scientific cameras), we chose this FTF4052M.[12] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r12),[13] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r13)

The most significant feature of the FTF4052M is that it has a four-quadrant symmetrical structure. The entire device can be regarded as being composed of four symmetrical parts: W, X, Y, and Z. Each part has a set of identical but independent drive clocks and offsets. Each quadrant has its own vertical and horizontal transfer clock inputs A1–A4 and C1–C3. The direction of the charge transfer is determined by the phase relationship of the transfer clock. This symmetrical structure enables the CCD to output in 1, 2, or 4 channels, but it achieves the fastest output speed in four channels. At this time, the charge in the image area moves to the top and bottom simultaneously, and the charge in the output register moves to both the left and right ends at the same time, as shown in Fig. 1 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#f1).[12] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r12),[13] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r13)

Fig. 1 Download (/proceedings/DownloadFigures?url=/ContentImages/Journals/OPEGAR/58/8/083104

Structure of FTF4052M output state.



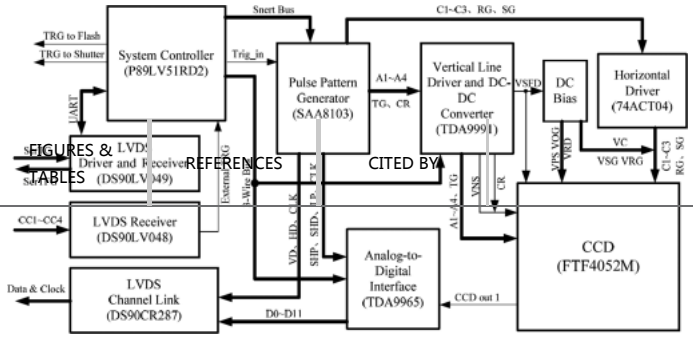
Regarding the voltage input, by changing the driving timing of each part, the signal charge of each quadrant can be shifted to different directions, thereby achieving a flexible output number and output mode selection. When using a single-ended output, the maximum frame rate is *[Math Processing Error]* (fps), and when four simultaneous outputs are used, the maximum frame rate is *[Math Processing Error]*.

2.1.2. Drive circuit design of FTF4052M

Figure 2 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#f2) shows the circuit block diagram of the designed camera circuit system. The system consists of a pulse pattern generator (SAA8103), a vertical driver (TDA9991), a horizontal driver (74ACT04), a DC bias circuit, a front-end signal processor (TDA9965), a system controller (P89LV51RD2), and a camera link interface circuit (DS90CR287,DS90LV048/049).[14] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r14),[15] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r15)

Fig. 2 Download (/proceedings/DownloadFigures?url=/ContentImages/Journals/OPEGAR/58/8/083104

FTF4052M drive circuit system structure diagram.



A1–A4 are the vertical transfer drive clocks, VA high is the high-level transfer clock, and TG is the transfer clock. The CR signal is a charge reset signal of the CCD photosensitive area, and its function is to remove the residual charge of the CCD photosensitive area before integration begins. C1–C3 are the horizontal transfer drive clocks. RG, SG, SHP, SHD, and LP are high-frequency timing pulses closely related to the ADC (TDA9965). CLK is the pixel clock. HD is the line clock signal, and VD is the frame clock signal. Trig_in is an external trigger signal. RG is the output amplifier reset pulse, and SG is the horizontal pixel merge gate drive clock. VNS is the voltage applied to the n-type substrate of the CCD, and VPS is the voltage applied to the p-type substrate of the CCD. VSFD is the DC voltage applied to the CCD output amplifier, and VRD is the voltage applied to the drain of the reset transistor of the CCD output amplifier. VOG is the electricity added to the CCD output gate (OG).[16] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r16),[17] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r17)

The driver timing pulse generator generates various timing pulse signals required by the system. The vertical driver amplifies the vertical transfer timing to drive level signals that have sufficient voltage and the current drive capability to generate the main DC bias voltage required by the CCD, and the horizontal driver amplifies the horizontal transfer timing to a drive level signal that satisfies the CCD operation requirement. The DC bias circuit divides the main DC bias voltage generated by the vertical driver to generate other DC bias voltages required by the CCD. The front-end signal processor performs a correlation acquisition of the analog signal output from the CCD sample, controllable gain amplification, dark level clamp compensation, and analog-to-digital conversion. The camera link interface circuit is responsible for outputting the digital image signals generated by the analog-to-digital converters from the camera and providing them to the host computer. The system controller is mainly responsible for initializing and configuring the IC (Integrated Circuit) in the system during power-up, sending control commands and data, changing the parameters of each IC in real time, and controlling the shooting process.[16] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r16),[17] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r17)

2.2. High-Frequency Frame Drive Circuit Design of FTF4052M

Currently, digital cameras based on the FTF4052M mostly use a single-channel output, and the frame rate does not exceed 1 fps, which cannot meet the requirements of some applications with high frame rates. FTF4052M has a four-quadrant symmetrical structure, and each of the four corners has an output amplifier. The charge transfer direction of each quadrant can be independently controlled, and the number of output channels and which output amplifiers to use for a specific output can therefore be flexibly selected. To achieve a frame rate of 3.4 fps, four outputs must be used, and the integration time cannot be greater than 40 ms. When there are four outputs, the drive circuitry of the FTF4052M needs to be improved.

When *[Math Processing Error]* outputs are used, since the outputs of the output amplifiers are simultaneously obtained, the readout time can be shortened to *[Math Processing Error]* of the single output; since each output amplifier outputs a complete image of the area, the output image has a full frame format and the original resolution. The improved drive circuit FTF4052 can support the simultaneous output of four CCD channels.

With a 25-MHz pixel clock, the readout time of an image is 293.1 ms, and the maximum frame frequency can reach 3.4 fps. We give the relationship between the frame frequency and integration time when 1, 2, and 4 output channels are used. Four output channels can be clearly seen. With the increase in the integration time, the degree of improvement gradually decreases due to the smaller proportion of the readout time to the

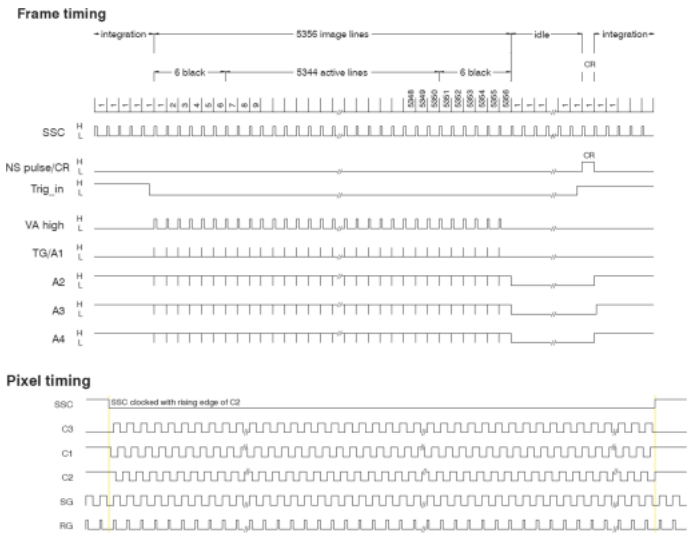
In practical applications, an appropriate number of output channels can be selected according to the integration time and the frame frequency to achieve the best cost-effect ratio.

2.2.1. Driver timing design

When the FTF4052M uses four outputs, the charge in the CCD image area is simultaneously transferred to the top and bottom horizontal output registers during the vertical line transfer. During horizontal pixel transfer, the charges of the two horizontal output registers are simultaneously transferred to the left and right output amplifiers. The required drive timing is shown in Fig. 3 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#f3).[12] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r12)

Fig. 3 Download (/proceedings/DownloadFigures?url=/ContentImages/Journals/OPEGAR/58/8/083104

Transfer drive timing diagram for the four outputs of the FTF4052M.



To implement the transfer method shown in Fig. 2 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#f2), it is necessary to connect the drive clocks of the proper phase to the vertical and horizontal transfer clock input terminals of each quadrant of the CCD. It can be seen that the change in the charge transfer direction is achieved through the interchange of A2 and A4 and of C1 and C2. To generate the drive timings of the four outputs, only the SAA8103-related registers need to be reconfigured to change the number of line transitions and pixel transitions, as well as the waveforms of the image line and the field sync signals. Other configurations are the same as that for a single-ended output. The waveforms of A1–A4 and C1–C3 are shown in Fig. 3 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#f3).

Table 1 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#t001) shows the connections of the quadrant drive clock. To realize the transfer mode shown by four output channels, it is necessary to vertically and horizontally move the clock in each quadrant of the CCD, and each input is connected to the appropriate phase drive clock.

Table 1

Each quadrant of the four-output clock signals of the input signal table.

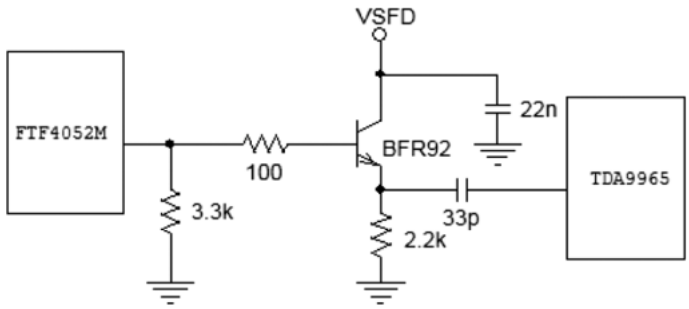
	A1 terminal	A2 terminal	A3 terminal	A4 terminal	C1 terminal	C2 terminal	C3 terminal
[Math Processing Error] quadrant	A1	A2	A3	A4	C1	C2	C3
[Math Processing Error] quadrant	A1	A2	A3	A4	C1	C2	C3
[Math Processing Error] quadrant	A1	A2	A3	A4	C1	C2	C3
[Math Processing Error] quadrant	A1	A2	A3	A4	C1	C2	C3

2.2.2. Improvements in the vertical driver circuit

When using four outputs, four high-frequency transistors, BFR92, are required to constitute an emitter follower to output the four analog signals of the CCD. This circuit is shown in Fig. 4 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#f4).

Fig. 4 Download (/proceedings/DownloadFigures?url=/ContentImages/Journals/OPEGAR/58/8/083104

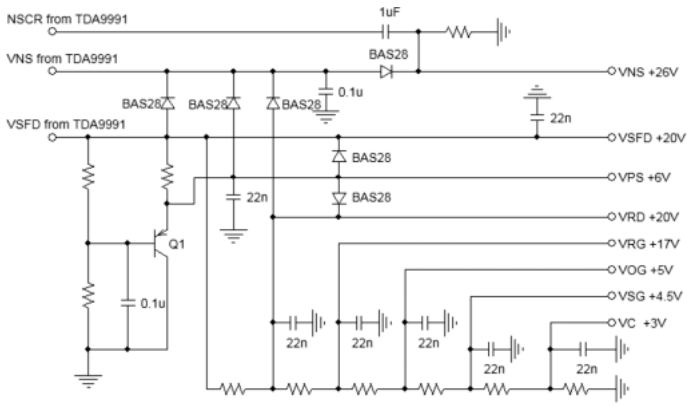
FTF4052M output tracker and coupling circuit.



The four transistors are powered by the 20-V VSFD provided by the TDA9991. The four output amplifiers on the CCD are also powered by the VSFD. In addition, various DC bias voltages are obtained from the VSFD voltage divider, which requires the VSFD to have a sufficient voltage drive capability, as shown in Fig. 5 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#f5).

Fig. 5 Download (/proceedings/DownloadFigures?url=/ContentImages/Journals/OPEGAR/58/8/083104

FTF4052M DC bias circuit.



The typical current supplied by the VSFD to each on-chip output amplifier is stated on the FTF4052 data sheet at 4.5 mA. The current supplied to each emitter follower can be estimated as

Eq. (1)

[Math Processing Error]

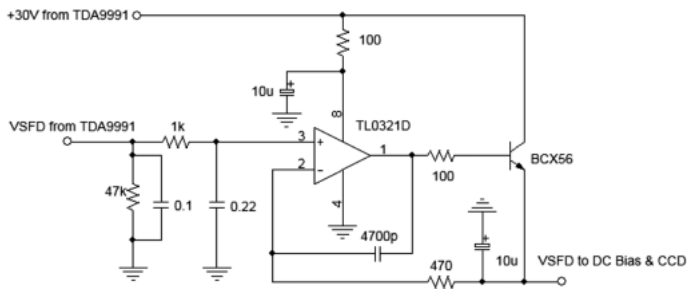
[Math Processing Error] is the base voltage of the transistor, which is approximately equal to the output on-chip amplifier. When the calculation is made, the reset reference voltage VRD (20 V) is taken, and *[Math Processing Error]* becomes the turn-on voltage of the emitter junction; 0.8 V is used for the calculation.

In this way, the current supplied by the VSFD to each output amplifier is *[Math Processing Error]*, and that of the fourth channel is *[Math Processing Error]*. From the TDA9991 data sheet, the VSFD terminal can only output a maximum current of 20 mA, which obviously cannot meet the four-channel output drive requirements.[17] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r17)

To improve the current driving capability of the VSFD, a buffer circuit is designed to buffer the VSFD. As shown in Fig. 6 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#f6), the VSFD is amplified using an integrated op amp and power transistor to form a voltage follower. The op amp and transistor are powered by the 30-V output of the DC-DC module of the TDA9991.[18] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r18)

Fig. 6 Download (/proceedings/DownloadFigures?url=/ContentImages/Journals/OPEGAR/58/8/083104

VSFD buffer circuit.



This circuit can effectively improve the current drive capability of the VSFD and ensure the safety of the CCD because the voltage at the circuit output terminal always changes with the input terminal and does not change the order of the previous power-up and power-off.

2.2.3. Improvement in the front-end signal processing circuit

Four channels of the TDA9965 are required to form a parallel channel for the front-end processing of the video signal output by the CCD when outputting four channels. Four TDA9965s are connected in parallel, and the required timing signal is generated by the SAA8103. After two levels of the 74ACT04, the signal is converted into four channels and distributed to each chip. To maintain the consistency of the transmission characteristics of each channel, the PCB should be designed so that the transmission distances of the video signal between the input of the TDA9965 and the output of the CCD are approximately the same. The transmission delays of the timing signal to the TDA9965s should be the same, and the channels should also be the same. To control the gain, bandwidth, and clamp level of each channel independently, four TDA9965s receive configuration data over four independent three-wire bus interfaces. Although the system controller is designed for only two three-wire bus interfaces, the timing generator SAA8103 itself has three three-wire interfaces; thus, it is sufficient. The configuration data of the TDA9991 and the two TDA9965s are transmitted by the system controller to the SAA8103 for forwarding. The configuration data of the other TDA9965s are sent directly by the system controller.[1] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r1),[10] (/journals/optical-engineering/volume-58/issue-

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8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r10) The limit frequency of the horizontal transfer of the FTF4052M is 27 MHz. In the design, a 25-MHz crystal oscillator is used as the clock source of the time sequence generator. When using a single-ended output, the maximum frame frequency is *[Math Processing Error]*. When using four simultaneous output channels, the maximum frame frequency can reach *[Math Processing Error]*. The CCD uses a single output. When using a 25-MHz clock frequency, the maximum frame frequency is near *[Math Processing Error]*, which cannot always meet the speed requirements. In this research task, the frame frequency must reach *[Math Processing Error]*; thus, the designed circuit system must be improved. In Sec. 3.3 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#sec3.3), the improvement in the front-end signal processing circuit is described. Our circuit design is proven to meet our needs. Our design has been applied to products, and it has proven to be feasible.

2.2.4. Improvements in the output interface circuit

When the CCD uses four outputs, *[Math Processing Error]* bit parallel image data are generated. The Camera Link interface in the base mode cannot meet the data transmission requirements; thus, medium mode is used in the design. Only one Channel Link chip DS90CR287 can be added to the system. The clock and synchronization signal inputs are connected in parallel with the system's original DS90CR287. In addition, the lengths of the two wires are approximately equal.

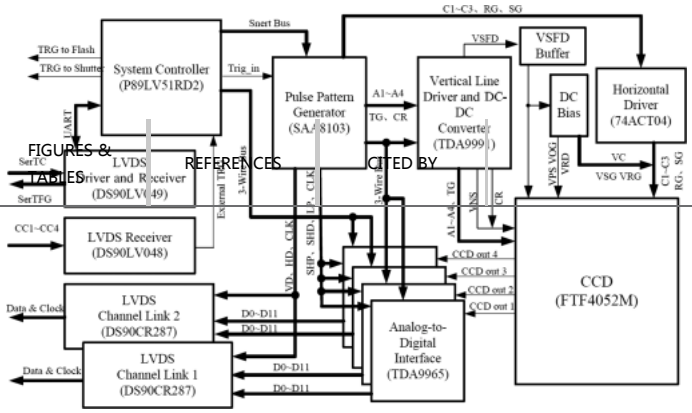
According to the characteristics of the area array CCD FTF4052M, which is a black-and-white CCD, the CCD is divided into four quadrants: upper left, lower left, upper right, and lower right. The same frame can be divided into four parts, and the digital image information of each part is eight bits. There are two methods of image transmission and display. The first method is parallel real-time transmission and the display of images in four quadrants; this transmission mode requires a sufficient data bit width. For the area array CCD FTF4052M, the total data bit width is *[Math Processing Error]*, and the data transmission frequency is 25 MHz (the pixel clock of the CCD FTF4052M is 25 MHz). For the second method, the four digital images are first transferred, and the image information is integrated into a complete frame of image information and then transmitted to the host computer through a high-speed image digital interface. At this time, the data bit width is 8 bits, but the data transmission frequency is *[Math Processing Error]*. The system adopts the first transmission mode, and the image is transmitted by the four parts in parallel. There are many types of image acquisition cards. The Matrox Meteor-II/Digital acquisition card is selected in this system; it uses a 32-bit PCI bus master/slave interface. Bus master mode can transmit data at a rate of up to *[Math Processing Error]* without occupying the bus continuously. At the same time, this mode supports a 32-bit data bandwidth that can be configured as *[Math Processing Error]*, *[Math Processing Error]*, or *[Math Processing Error]*. For this system, the configuration is *[Math Processing Error]*. Under LVDS transmission mode, the sampling rate can reach 25 MHz. The 8-bit bandwidth is suitable to meet our needs. Thus, we use the 8-bit bandwidth.

2.2.5. Improved circuit block diagram

After the above improvements, the designed large-area CCD drive circuit system can support the CCD in outputting the signal charge from the four output amplifiers simultaneously. The circuit structure of the system is shown in Fig. 7 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#f7).

Fig. 7 Download (/proceedings/DownloadFigures?url=/ContentImages/Journals/OPEGAR/58/8/083104

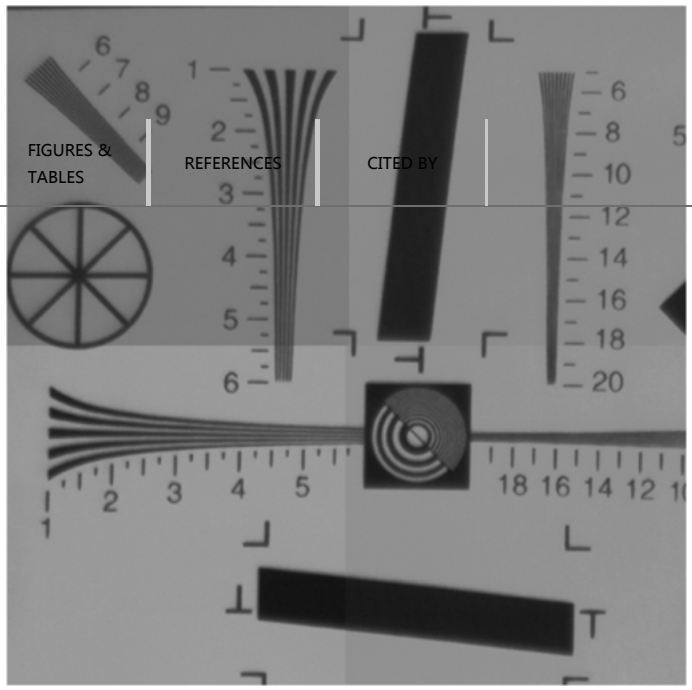
High frame rate FTF4052M drive circuit system structure diagram.



When using a 25-MHz pixel clock, the time required for the FTF4052M to transfer a frame of charge in this circuit system is *[Math Processing Error]*. Therefore, the maximum frame frequency can reach 3.4 fps, which is 2.5 times higher than that of the single-channel output. In terms of the design goals, the actual circuit system was photographed, and a clear image was obtained; the signal-to-noise ratio of each output image was equal to that of a single output. However, after splicing each image into a complete image, it can clearly be observed that the image is composed of four small images, and the gradation transition at the splicing part is relatively obvious. That is, "joint noise" appears, as shown in Fig. 8 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#f8). In this system, the FTF4052M uses four quadrants for a simultaneous output. When the CCD uses four output channels, the output image has an obvious seam, or strip effect, which is caused by the inconsistency of the transmission characteristics between output channels. This inconsistency is called channel inhomogeneity, and it manifests after the output image is spliced into a complete image, where it can be clearly observed that the image is spliced from four small images and the gradation is obvious. Many factors contribute to the nonuniformity of the output channel. The most important one is that each channel's on-chip amplifier and on-chip emitter-follower transistor have different gain, offset, and nonlinearity characteristics, which results in an output channel that is not completely symmetrical. In this way, even if the CCD is illuminated by uniform light, the gray mean values of the images obtained in each output channel differ.[17] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r17) In addition, there are differences in the transmission paths of the CCD video signals. These factors make it impossible for the transmission characteristics of the four quadrants to be exactly the same, resulting in the presence of nonuniformity in the response between the output images of the various quadrants. To correct the four quadrant images to be consistent, these differences must be quantified, which will be described in detail in the next section.[2] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r2),[3] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r3)

Fig. 8 Download (/proceedings/DownloadFigures?url=/ContentImages/Journals/OPEGAR/58/8/083104

Joining the four quadrant export images of the FTF4052M.

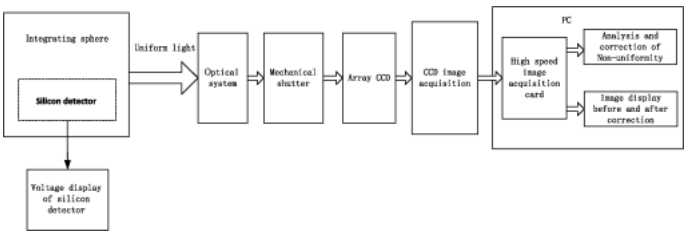


2.3. Response Nonuniformity Detection System for FTF4052M

The detection and correction system of the response nonuniformity of the FTF4052M is composed of an integrating sphere, a silicon detector, an area array CCD, a CCD image acquisition component, a high-speed image acquisition card, and an upper computer. The block diagram of the structure is shown in Fig. 9 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#f9).

Fig. 9 Download (/proceedings/DownloadFigures?url=/ContentImages/Journals/OPEGAR/58/8/083104

Structural block diagram of the nonuniformity detection system.



The integral sphere consists of a sphere, a lamp group, and a silicon detector, which simulates the total radiation illuminance formed by the ground radiant illumination and the backscattering of the sky when there are different sun zenith angles and degrees of ground object reflectivity. The beam from the integrating sphere is uniform. The radiation illuminance of the light source is controlled by adjusting the number of the inner lamp in the integral sphere. The irradiance of the integral ball is measured using a calibrated radiation illuminometer. Compared with the silicon detector in the integrating sphere, the relationship between the output voltage and radiation illumination of the silicon detector for monitoring in the integrating sphere is determined. During the nonuniformity detection, the radiation illuminance at the outlet of the integral ball light source can be calculated using the output voltage of the silicon detector in the integral sphere. The surface array CCD and its subsequent processing circuit are placed at the outlet of the integral ball so that the photosensitive surface of the surface array CCD is directly next to the exit of the integral ball. Because the CCD chip FTF4052M is a full-

frame CCD chip, the photosensitive surface accounts for the majority of the area of the CCD. To get a 100% pollution-free image, for exposure stability and instant photoelectric conversion during the shutter opening and closing time, a mechanical shutter should be added in front of the FTF4052M.[5] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r5) [19] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r19)

The experiment was calibrated under a mechanical shutter exposure time of 1.2 ms. The analog video signal of the CCD array output is converted to a digital video signal through the CCD image acquisition component, and the digital video signal is transmitted to the PC using a high-speed image acquisition card. The nonuniformity detection and correction are completed by the PC test software, and the performance of the correction algorithm is analyzed.

3. Nonuniformity Detection and Correction Algorithm

When the CCD uses four output channels, the output image has an obvious seam, or strip effect, which is caused by the inconsistency of the transmission characteristics between output channels. This inconsistency is called channel inhomogeneity. There are many factors that contribute to the nonuniformity of the output channel. The most important one is that each channel's on-chip amplifier and on-chip emitter-follower transistor have different gain, offset, and nonlinearity characteristics, which results in an output channel that is not completely symmetrical. In this way, even if the whole CCD is illuminated by uniform light, the gray mean values of the images obtained in each output channel differ. To eliminate this type of joint, it is necessary to correct the nonuniformity between channels. In addition to the response nonuniformity among the four quadrants, there is also response nonuniformity among the pixels of each quadrant. For example, a calibration point with an irradiance of 2.5887 is selected, and an image with *[Math Processing Error]* is taken from the original image, which was taken with uniform light. The image is enlarged, as shown in Fig. 13 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#f13). As seen from the figure, the image has many vertical stripes with different gray values. Therefore, we first discuss the nonuniformity between the four quadrants of the planar array CCDFTF4052M. In the following section, we discuss nonuniformity detection between the pixels of each quadrant. The first is the nonuniformity between the four quadrants, and the second is the nonuniformity between the pixels of each quadrant.

3.1. Nonuniformity Detection and Correction between Four Quadrants of FTF4052M

During the nonuniformity detection, the CCD array is first calibrated. The calibration outputs an amount of uniform light of different radiant irradiances at the outlet of the integral ball, shoots, and stores a number of images, measures the response linearity of the CCD array, and then selects a nonuniformity correction method according to the response linearity of the CCD array. The responsivity of the CCD planar array can be characterized by the sensitivity and dark current signals.[8] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r8)

Eq. (2)

[Math Processing Error]

In the equation, *[Math Processing Error]* represents the sensitivity of the CCD array, *[Math Processing Error]* represents the radiation illumination at the outlet of the integral sphere, and *[Math Processing Error]* represents the number of target points. Here, standard point *M* is selected, *[Math Processing Error]* is expressed as the mean value of all pixel output signals of the surface matrix CCD when the radiation illumination is *[Math Processing Error]*, and *[Math Processing Error]*represents the average dark electric current signal of the CCD array elements.[8] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-

a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r8),[9] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r9)

current signal of the area array CCD is measured without illumination, which is the background. Then, at each calibration point, the corresponding digital images are collected and stored. For each radiation illumination, the output signal value of each pixel of the full-frame array CCD is not exactly the same but rather fluctuates up and down in a certain signal value, so the mean of the output signal value of all pixels is used as the signal value of the image output in the calibration. Random noise inevitably exists in the process of image acquisition, and it will interfere with the results of the nonuniformity correction. Random noise belongs to a normal distribution, and its mathematical expectation is 0. Therefore, whether acquiring a dark current image signal or image signal at each calibration point, it is necessary to continuously collect 50 frames of image data. The influence of random noise can be eliminated by averaging.

The experiment was calibrated under a mechanical shutter exposure time of 1.2 ms, a video signal processing gain of 9 dB, and an offset of 0. Eight calibration points were selected, and the four quadrants of the CCDF F4052M area array were calibrated. The calibration results are shown in Table 2 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#t002). UL represents the upper left, UR represents the upper right, LL represents the lower left, and LR represents the lower right.

Table 2

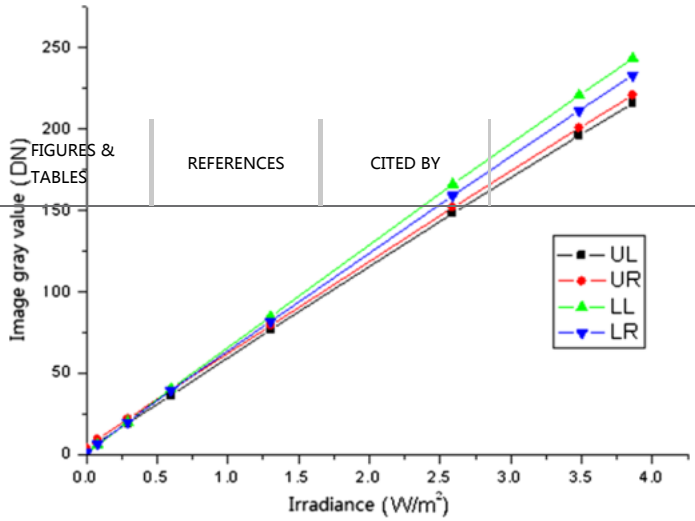
Calibration result of the four quadrants of area CCDFTF4052M.

Radiant illumination (W/m2)	Gray value of image (DN)			
	UL	UR	LL	LR
0	2.47	4.31459	1.23875	1.36
0.079	7.45757	9.45722	5.80375	6.6
0.2908	19.65738	21.8835	19.92625	20.125
0.5987	35.96667	38.79612	41.5275	40.55
1.3008	76.00952	78.91068	83.79	81.925
2.5898	147.90952	150.70879	165.065	160.325
3.4872	195.09524	199.68176	221.93875	212.45
3.8619	213.70486	218.74272	244.37125	234.165

A fit of the calibration results and the resulting responsivity curve is shown in Fig. 10 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#f10). It can be seen from the figure that the response linearity of the four quadrants is quite good, with a reliability of linear fitting of 0.9994.[4] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r4),[11] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r11) This result shows that the driving circuit of the FTF4052M is working properly, and the ordinate is the image gray value. Because the collected digital image is represented as 8 bits, the image grayscale is 0 to 255, and the abscissa is the irradiance (*[Math Processing Error]*).

Fig. 10 Download (/proceedings/DownloadFigures?url=/ContentImages/Journals/OPEGAR/58/8/0831

Response degree curves of the four quadrants of the FTF4052M.



The fitting equations for the response curves of the four quadrants of the FTF4052M are as follows:

The upper left (UL) quadrant:

Eq. (3)

[Math Processing Error]

The upper right (UR) quadrant:

Eq. (4)

[Math Processing Error]

The lower left (LL) quadrant:

Eq. (5)

[Math Processing Error]

The lower right (LR) quadrant:

Eq. (6)

[Math Processing Error]

The standard deviation of the sensitivity of the four quadrants reached 3.5525. Obviously, such a standard deviation affects the consistency of the four quadrants' responsivities,[20] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r20) as seen from Fig. 10 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#f10).

There are many correction methods. The four-responsiveness curve can be rotated and translated to the average responsivity curve, and the responsivity curves in the other three quadrants can also be rotated and translated to the curve of another quadrant, which can meet the expected requirements.[21] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r21) The correction method used here rotates and translates the responsivity curves of the UL, LL and LR quadrants to the curve of the UR quadrant. Ideally, the four quadrant responsivity curves will completely coincide. The rotation and translation of the curves are achieved by changing the sensitivity and dark current signals, while the sensitivity and dark current signals are changed by adjusting the gain and offset in the video signal processing circuit. The minimum adjustment step of the gain is 0.125 dB, and the minimum adjustment step of the offset is 1 code (DN);[6] (/journals/optical-engineering/volume-58/issue-

8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r6) thus, the theoretical calculation value cannot be fully achieved, but the adjustment step length according to the gain and offset is close to the theoretical value, which does cause small errors. See Table 3 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#t003) for the theoretical calculations and the actual gain and offset values for the UL, LL, and LR quadrants that need to be changed.

Table 3

Theoretical and actual values of the gain and offset of the UL, LL, and LR quadrants.

Quadrant	Gain (dB)		Offset (DN)	
	Theoretical value	Actual value	Theoretical value	Actual value
UL	9.213	9.234	1.979	2
LL	7.983	8	3.079	3
LR	8.45	8.5	3.05	3

According to the actual value correction, the UL, LL, and LR quadrants are recalibrated. The calibration results are shown in Table 4 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#t004).

Table 4

Calibration result of the four quadrants of area CCDFTF4052M after correction.

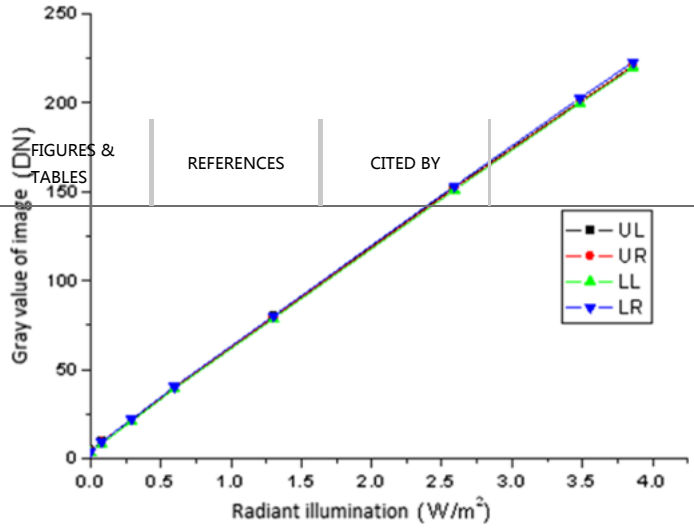
Radiant illumination (W/m2)	Gray value of image (DN)			
	UL	UR	LL	LR
0	4.5362	4.21359	3.11475	4.18234
0.079	9.53614	9.35922	8.26201	9.3248
0.2908	21.73405	21.8835	20.8494	21.998
0.5987	39.1976	39.79612	39.12216	40.3352
1.3008	79.92173	79.31068	78.66246	80.2428
2.5898	152.45705	151.90777	151.00482	153.214
3.4872	200.9347	200.62136	199.83358	202.6088
3.8619	221.03106	220.74272	219.90788	223.07

The experiment was calibrated under a mechanical shutter exposure time of 1.2 ms, a video signal processing gain of 9 dB, and an offset of 0. Eight calibration points were selected, and the four quadrants of the CCDF F4052M area array were calibrated. The calibration results are shown in Table 2 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#t002). According to the value correction, the UL, LL, and LR quadrants are recalibrated. The calibration results are shown in Table 4 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#t004). When the irradiance is 0, the gray values of the quadrants are 4.5362, 4.21359, 3.11475, and 4.18234. In Table 2 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#t002), when the irradiance is 3.8619, the gray value of LL is 244.37125. We limit the irradiance to the range from 0 to 3.8619, and the quadrant values are all within [0,255].

The response curve fitting of the FTF4052M is shown in Fig. 11 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#f11).

Fig. 11 Download (/proceedings/DownloadFigures?url=/ContentImages/Journals/OPEGAR/58/8/0831

Response degree curves of the four quadrants of the FTF4052M after correction.



To fit the calibration results and the response curves of the four quadrants of the FTF4052M, the fitting equations are

The upper left (UL) quadrant:

Eq. (7)

[Math Processing Error]

The upper right (UR) quadrant:

Eq. (8)

[Math Processing Error]

The lower left (LL) quadrant:

Eq. (9)

[Math Processing Error]

The lower right (LR) quadrant:

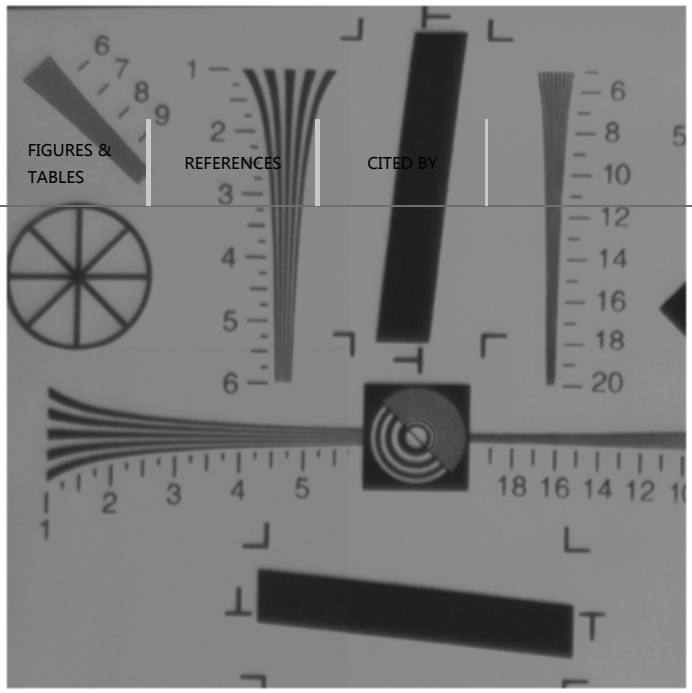
Eq. (10)

[Math Processing Error]

The standard deviation of the four quadrant sensitivity values is reduced to 0.2668 after calibration, which is a reduction of *[Math Processing Error]*. At the same time, after the correction, the resolution plate image of Fig. 8 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#f8) is retaken. It can be seen from Fig. 12 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#f12) that the response inhomogeneity of the four quadrants has been greatly improved.[6] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r6)

Fig. 12 Download (/proceedings/DownloadFigures?url=/ContentImages/Journals/OPEGAR/58/8/0831

Joining the four quadrants' export images after correction.



3.2. Nonuniformity Detection and Correction of the FTF4052M between the Pixels of Each Quadrant

In addition to the response nonuniformity among the four quadrants, there is also response nonuniformity among the pixels of each quadrant. For example, a calibration point with an irradiance of 2.5887 is selected, and an image with *[Math Processing Error]* is taken from the original image, which was taken with uniform light. The image is enlarged, as shown in Fig. 13 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#f13). As seen from the figure, the image has many vertical stripes with different gray values. For low-light shooting, such stripes will seriously affect the imaging quality. Figure 14 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#f14) shows the stereoscopic distribution of the gray value of the intercepted original image. The gray value is between 105 and 118, and the pixel response nonuniformity is large; thus, it must be corrected.[7] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r7),[22] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r22)

Fig. 13 Download (/proceedings/DownloadFigures?url=/ContentImages/Journals/OPEGAR/58/8/0831

Original picture that was cut out before correction.

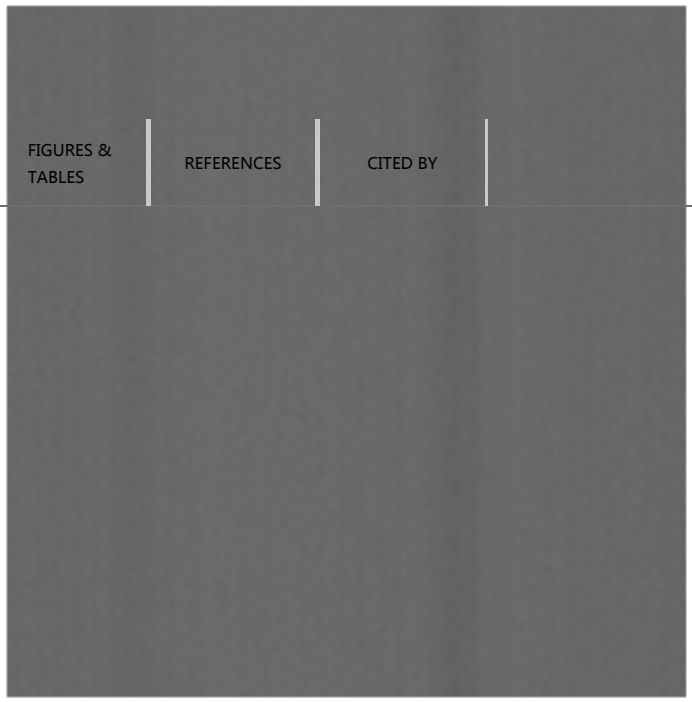
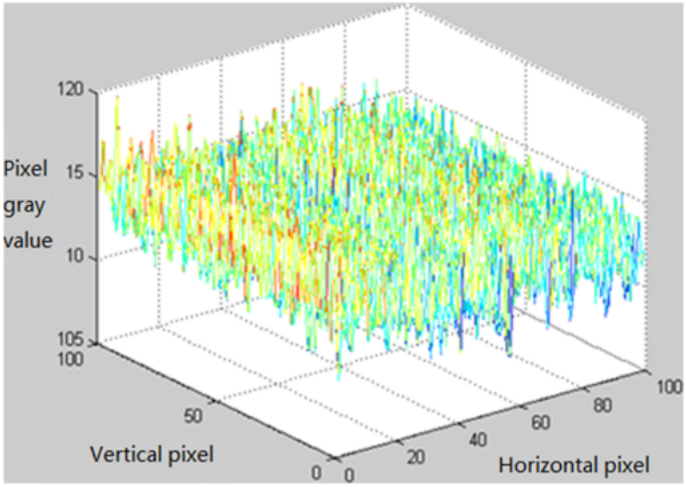


Fig. 14 Download (/proceedings/DownloadFigures?url=/ContentImages/Journals/OPEGAR/58/8/0831

Cube of the original picture's gray values.



According to the linearity of the area array CCD response, response nonuniformity correction can adopt single-point, two-point, and multipoint correction methods. Since the single-point correction method corrects only the different pixel output signals to the average signal under one illuminance,[6] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r6),[21] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r21) the integration point has certain limitations. When the area array CCD response is linear, the two-point correction method is used; that is, under two illuminances, the output signals of each pixel of the area array CCD are corrected to the average signal. If the response of the area array CCD is nonlinear, a multipoint calibration segmentation correction is adopted; that is, the calibration interval is divided into many segments, and the nonlinear response of the area array CCD is treated as a linear response in each segment. The method is the same as for the two-point correction algorithm, but the greater the calibration point is, the larger the amount of data calculated. In this paper, since the responsivity of the FTF4052M is linear, the nonuniformity correction using the two-point

correction method is optimal. The sensitivity and dark current signal of each pixel of the area array CCD cannot be exactly the same; thus, each pixel has its own unique responsiveness. To distinguish it from the calibration area CCD responsiveness expression, the sensitivity and dark current signals of each pixel are described here as a gain factor and an offset factor, which are collectively referred to as correction factors, and established as follows:[6] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r6)–[23] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r23)

Eq. (11)

[Math Processing Error]

[Math Processing Error] indicates the average gray value of all pixels of the area array CCD when the irradiance is *[Math Processing Error]*. After correction, the gray values of the other pixels are converted to the average gray value. *[Math Processing Error]* indicates the actual output gray value of row *[Math Processing Error]* and column *[Math Processing Error]* of the uncorrected area CCD. *[Math Processing Error]* represents the gain of row *[Math Processing Error]* and column *[Math Processing Error]* of the area array CCD, and *[Math Processing Error]* indicates the offset of row *[Math Processing Error]* and column *[Math Processing Error]* of the area array CCD. *[Math Processing Error]* and *[Math Processing Error]* are the numbers of rows and columns of the effective pixels of the area array CCD, respectively. For the area array CCD4052M, *[Math Processing Error]* and *[Math Processing Error]* are 4008 and 5344, respectively.[24] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r24)–[26] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r26)

The two-point calibration method requires two calibration points to be selected, and two equations are obtained:

Eq. (12)

[Math Processing Error]

Eq. (13)

[Math Processing Error]

From Eqs. (12) and (13), the gain factor and offset factor of each pixel of the area array CCD can be derived

Eq. (14)

[Math Processing Error]

Eq. (15)

[Math Processing Error]

The gain factor and offset factor of each pixel of the area array CCD are determined and then stored in the correction factor matrix. To remove the random noise, the above test is repeated 50 times, and the average of the 50 results is used as the final correction factor. The correction process is to multiply the output value of each pixel in the image by the respective gain factor and add the offset factor, thereby achieving the consistency of the responsivity of each pixel of the area array CCD, that is, completing the response nonuniformity correction.[27] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r27)

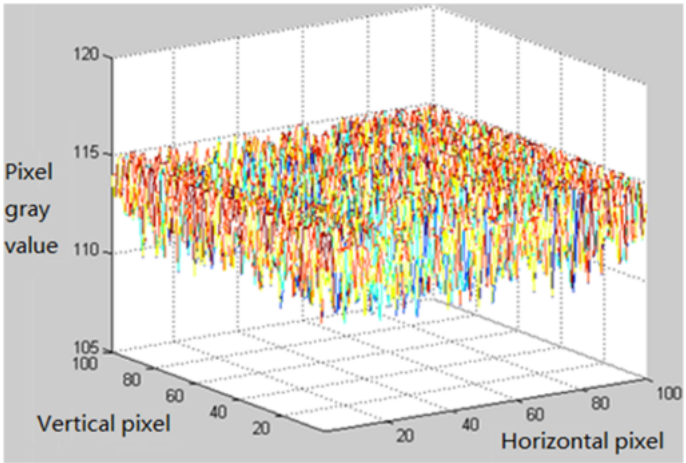
The corrected image in Fig. 13 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#f13) is shown in Fig. 15 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#f15). The gray values of the image are between 110 and 115. The three-dimensional distribution of the gray values in Fig. 14 (/journals/optical-engineering/volume-58/issue-

8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#f14) is shown in Fig. 16 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#f16). The nonuniformity is obviously improved.

Picture after correction.

Fig. 16 Download (/proceedings/DownloadFigures?url=/ContentImages/Journals/OPEGAR/58/8/0831

Cube of the corrected picture's gray values.



Comparing Figs. 13 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#f13) and 15 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#f15), it can be seen that there is a significant difference between the gray values corresponding to the uncorrected image, and the image after a two-point correction looks very uniform, which illustrates the performance of the two-point correction algorithm. Four images under irradiance were selected, and precorrection and postcorrection nonuniformity analyses were performed, as shown in Table 5 (/journals/optical-engineering/volume-58/issue-

8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#t005). This table shows that the nonuniformity among the pixels of the corrected area CCD4052M is reduced by *[Math Processing Error]*, and the nonuniformity is obviously improved.[28] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r28)–[30] (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#r30)

Table 5

Comparison of the nonuniformity response before and after correction.

Radiation illuminance at the exit of the integrating sphere (W/m2)	Precorrection nonuniformity	Corrected nonuniformity
0.2909	0.0536	0.0054
0.5964	0.0484	0.0048
2.5887	0.0459	0.0046
3.4814	0.0421	0.0049

3.3. System Imaging Results

According to the design proposal presented above, a schematic diagram and PCB design of the circuit system were produced, and finally the actual circuit debugging was completed. The designed system works fine, is stable and reliable, and can obtain clear images. Figure 17 (/journals/optical-engineering/volume-58/issue-8/083104/Design-of-a-high-frame-rate-driver-circuit-for-a/10.1117/1.OE.58.8.083104.full#f17) shows the actual image taken. The large image on the left is a full-frame *[Math Processing Error]* image, and the small image on the right is a partial enlargement of the full-frame image.

Fig. 17 Download (/proceedings/DownloadFigures?url=/ContentImages/Journals/OPEGAR/58/8/0831

Real image and partial magnification.

4. Conclusions

The basic driving circuit of the area array CCD FTF4052M was first given. The general method of frame frequency of the full-frame type area array CCD was then studied, and the advantages and disadvantages of various methods were analyzed. The maximum frame frequency of the FTF4052M was improved by using four parallel output technologies. At 3.4 fps, the design requirements were met. For a problem in a four-output system where the vertical drive current drive capability of the system is insufficient, a special buffer circuit was designed, which satisfied the CCD safe power-on and power-off sequences and the drive requirements. The nonuniformity of the full-frame area array CCDFT4052M was analyzed, and a response nonuniformity detection system was established. The nonuniformity among the four quadrants of the FTF4052M and that among the pixels were detected by the system. Based on the linearity of the CCD, a two-point correction algorithm was proposed, and the uniformity was corrected. By correcting the standard deviation of the four quadrant response sensitivities by a factor of 1/13, the responsive nonuniformity among all pixels was reduced to that of the original by a factor of 1/10; thus, the nonuniformity of the FTF4052M was significantly improved. Due to the limitations of the experimental conditions, we do not discuss the influence of the wavelength and *[Math Processing Error]*-number on the calibration; we will analyze this issue in future work.

Acknowledgments

All authors contributed to the article. Hang Ren conceived and designed the simulations under the supervision of Tao Tao Hu and Yu Long Song. Hang Ren performed the experiments, analyzed the data, and wrote the paper. Tao Tao Hu, Yu Long Song, and Ming He Gao reviewed the manuscript and provided valuable suggestions. This work was supported by the Fundamental Research Funds for the Central Universities (No. 2412019FZ037).

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Received: 26 February 2019; Accepted: 6 August 2019; Published: 23 August 2019