PAPER

# Novel single-transverse-mode control of VCSELs with dielectric mode filter

# Novel single-transverse-mode control of VCSELs with dielectric mode filter*

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We establish a novel method of controlling the transverse modes of vertical cavity surface emitting lasers (VCSELs) to achieve 1 mW single-fundamental-mode lasing. A dielectric mode filter is installed on top of the VCSEL. The dielectric layer ($SiO_2$) is deposited and patterned to modify the mirror reflectivity across the oxide aperture via antiphase reflections. This mode selection is nondestructive and universally applicable for other structures under single transverse mode. Destructive etching techniques (dry/wet) or epitaxial regrowth are also not required. This method simplifies the preparation process and improves the repeatability of the device. Measurements show that under continuous-wave current injection, the side-mode suppression ratio exceeds 30 dB.

**Keywords:** single-mode, dielectric mode filter, anti-phase reflection, mirror reflectivity, VCSEL

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## 1. Introduction

Vertical cavity surface emitting lasers (VCSELs) are effective solutions to end users' requirements for engineering applications because of their low power consumption, narrow bandwidth, high speed, polarization stability, and single mode in cloud services, internet protocol television, optical storage, gas sensing, and atomic chip devices.[1–4] Single-mode and high-power items are important in optical systems. The number of transverse modes rises dramatically as lateral dimensions increased. Thus the balance between maintaining single mode and increasing output power is a key research content. Several different solutions have been proposed to achieve single-mode high-power devices, which include weakening lateral cladding with a photonic crystal structure,[5,6] the high-order-mode loss with a triangular hole structure,[7] anti-resonant reflecting optical waveguide structure,[8] metal windows,[9] impurity-induced disordering of DBRs,[10] buried tunnel junctions,[11] and surface relief structure.[12–15] The highest output power of 7.5 mW at a side-mode suppression ratio (SMSR) of approximately 40 dB is demonstrated via triangular hole structure.[7] A single mode power of above 6 mW with SMSR higher than 30 dB is reported at 850 nm.[14]

However, these methods have disadvantages, such as complex epitaxial growth or device processing. Furthermore, the control precision of etching depth or epitaxial regrowth affects the reproducibility and yield of devices. In this study, a novel type of VCSEL with a dielectric mode filter is developed, and its performance is investigated. The new method for mode selection does not require additional lithography or semiconductor etching. The deposition of a dielectric material ($SiO_2$ layer) on top of the surface results in current insulation and mode filter through one self-aligned photoresist process and etching. Then we can create spatially dependent out-of-phase without semiconductor etching or regrowth, thereby suppressing the higher-order mode and preserving the fundamental mode.

## 2. Simulation and experiment

We deposit a single $\lambda/4$-thick dielectric material ($SiO_2$ layer) to maximize the out-of-phase reflection on the surface of VCSEL. The $SiO_2$ layer is deposited over the entire top surface of the top GaAs current-spreading layer to maximize threshold modal gain for all transverse modes, as shown in Fig. 1 with $SiO_2$.[16] The threshold modal gain decreases with the etching of the fundamental transverse mode region, because the $SiO_2$ layer corresponds to an increase in mirror reflectivity and loss, as shown in Fig. 1 without $SiO_2$.

A transfer matrix based method is used to calculate the threshold modal gain, and the optimum single-mode region is designed for the mode discriminator that minimizes the threshold modal gain in the center of the device and maximizes in high-order-mode regions. By calculating different patterns distribution along the radius direction, $LP_{11}$ and $LP_{21}$ are the main factors that affect single mode operation ($LP_{01}$). Thus

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we focus on the distribution of the three modes ($LP_{01}$, $LP_{11}$, and $LP_{21}$). The mesa diameter and oxidation aperture in the simulation are 20 and 6 μm, respectively. The mesa center is the origin of the coordinates, and the distribution of three patterns ($LP_{01}$, $LP_{11}$, and $LP_{21}$) along the radius direction is observed in Fig. 2. Therefore, the suppression of high order modes ($LP_{11}$ and $LP_{21}$) and the reservation of $LP_{01}$ are the main purposes. The mirror loss and threshold modal gain of the fundamental mode will decrease if the middle region of dielectric film ($LP_{01}$) is etched, as shown in Fig. 1 without $SiO_2$. In the same drive current, the fundamental mode lases, but high-order modes are suppressed due to the enlarged threshold modal gain. Therefore, a mode control is implemented. The fundamental mode is concentrated in the central area, and the high-order modes and fundamental mode have considerable overlap. From the simulation, we can see that the diameter of the fundamental mode region is 2 μm, but we adopt the diameter of 3 μm. This is the tradeoff between output power and mode composition. The balance is actually to enlarge the size of dielectric film relief and increase the volume of the fundamental mode, which will increase the single-mode output power and does not cause higher-order modes lasing within a certain degree of current range. If we control the diameter of dielectric film relief as 2 μm, the dielectric film relief suppresses the high-order modes while also limits the output power of single-mode. The dominant advantage of the fundamental mode compared to other high-order modes gradually decreases when the dielectric film relief diameter changes from 2 μm to 3 μm. However, when the diameter of dielectric film relief is 3 μm, it increases the size of the active area and the output power of the fundamental mode.

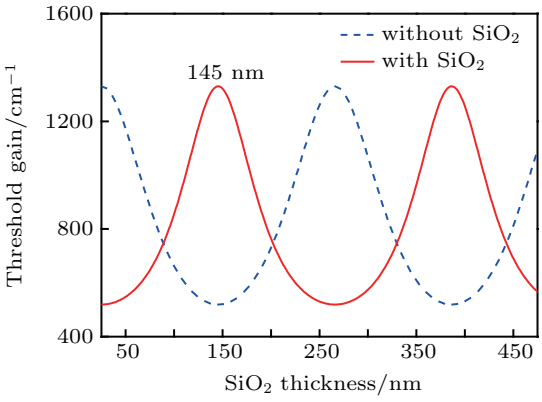


**Fig. 1.** (color online) Calculated VCSEL threshold gain with (red line) and without (blue line) $SiO_2$ layer.

This method creates a circular annulus with a depth of $\lambda/4$ and an inner diameter of 3 μm, which is etched into the center of the VCSEL. The deposited $SiO_2$ layer–GaAs and $SiO_2$ layer–air interfaces are out of phase with respect to the reflections from the DBR interfaces. The mirror loss increases further and the higher-order modes are suppressed. The $SiO_2$ layer in the central region is etched to make the fundamental mode lase and suppress the higher-order modes.

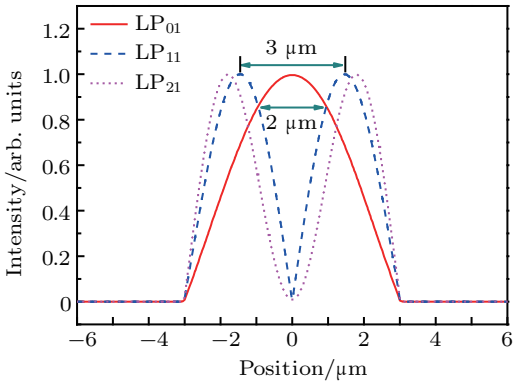


**Fig. 2.** (color online) The distribution of three patterns ($LP_{01}$, $LP_{11}$, and $LP_{21}$) along radius direction.

A schematic representation of the VCSEL structure is shown in Fig. 3. Our samples include AlGaAs structures with DBRs and oxide layer on both sides of the active region, which consists of three 7.2 nm GaAs quantum wells. The DBRs are quarter-wave-thick pairs of $Al_{0.12}Ga_{0.88}As/Al_{0.9}Ga_{0.1}As$ with 34 and 20.5 pairs in the bottom and top DBR, respectively. A 30-nm-thick $Al_{0.98}Ga_{0.02}As$ layer is inserted between the active region and the p-DBR. For the standard preparation of the device, a circular mesa structure is fabricated via dry etching. To achieve current and light confinement, an oxide aperture with a diameter of 6 μm is formed by selectively oxidizing the $Al_{0.98}Ga_{0.02}As$ layer. The next step is to fabricate the current insulation and dielectric mode filter. We firstly design a suitable mask to preserve the position of the annulus regions with higher-order modes, leaving the fundamental transverse mode unchanged (as shown in the inset of Fig. 3). An antiphase $SiO_2$ layer (145 nm) is then deposited by PECVD, with the $SiO_2$ layer patterned via a self-aligned photoresist process into a hollow circular cylinder. The inner diameter is 3 μm and the outer diameter is 8 μm. Finally, the p- and n-contacts are formed via magnetron sputtering.

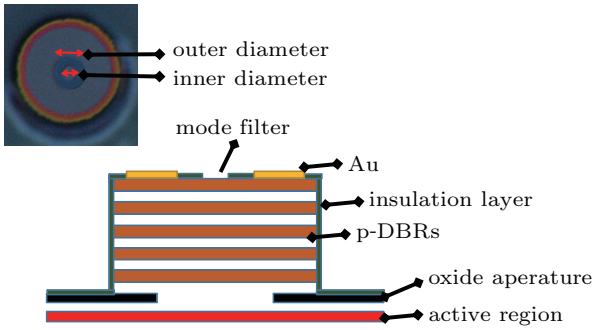


**Fig. 3.** (color online) Cross section of the VCSEL with dielectric mode filter. The inset is the top view image of the VCSEL with dielectric mode filter. The inner diameter is 3 μm and the outer diameter is 8 μm.

## 3. Results and discussion

Lasing characteristics are measured under continuous-wave current injection at room temperature. Figure 4 shows the output power characteristics of the VCSEL with a dielectric mode filter under different temperatures. The threshold current and turn-on voltage of the VCSEL with a dielectric mode filter under room temperature are 1.8 mA and 1.396 V, respectively. The maximum output power of the VCSEL with a dielectric mode filter is 1 mW. The output power gradually decreases and the threshold current increases under the same current with the increasing temperatures. These conditions are because the gain peak wavelength exceeds the cavity with the increasing temperatures, and the corresponding cavity-mode gain decreases because the gain–cavity mode offset is positive. The increasing temperature increases the separation between the cavity mode and gain peak, which results in a rapidly increased threshold current, as shown in the inset of Fig. 4.[16] The threshold current of VCSEL usually varies with temperature, which can be expressed as[17]

$$I_{\rm th}(T) = I_{\rm th,min}[1 + C_T(T - T_{\rm min})^2], \tag{1}$$

where $C_T > 0$ and the threshold current increases rapidly when the temperature exceeds $T_{\rm min}$. In our work, the minimum threshold current occurs when the temperature is 25 °C, and the threshold current rapidly increases with the increasing temperature.

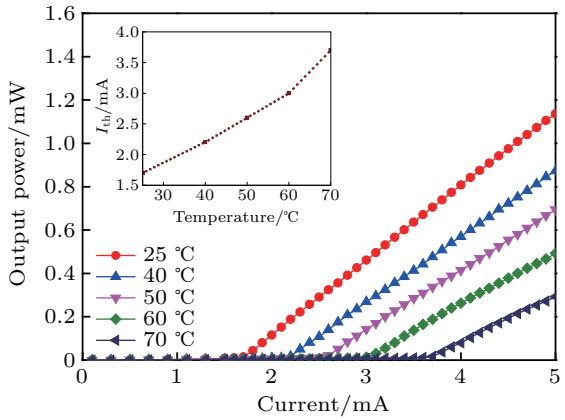


**Fig. 4.** (color online) *L–I–V* characteristics and the variation of threshold current (the inset) of the continuous-wave current injection for the VCSEL with a dielectric mode filter.

The samples with mode filter and without mode filter are compared, as shown in Fig. 5. The VCSEL with mode filter has higher threshold current and lower output power than the VCSEL without mode filter. The main reason is that the introduction of mode filter increases the threshold modal gain of high-order modes, which leads to an overall increase in threshold current. In this case, the threshold current of the *L–I–V* curve slightly increases because the dielectric mode filter elevates the threshold gain of all modes.[18,19] To suppress the high-order modes, the total output power of VCSEL with mode filter is less than that of the VCSEL without mode filter. The low output power is mainly caused by the conversion of electric power to heat and the light scattering via the edge of the dielectric mode filter.

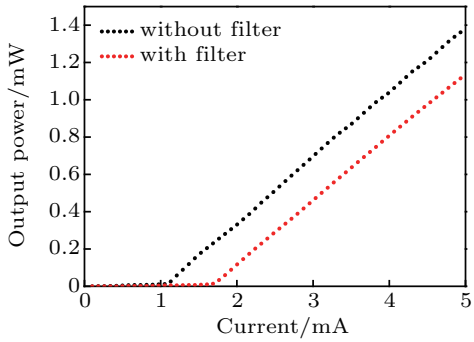


**Fig. 5.** (color online) Comparison of VCSEL output power with and without mode filter.

Figure 6 shows the mode characteristics of the VCSEL with a dielectric mode filter measured under continuous-wave condition ($I = 4$ mA) at room temperature. The optical spectra of the VCSEL with a dielectric mode filter remains at a single peak state. The fundamental mode is still dominant, and no other modes appear when the current is 4 mA. The SMSR exceeds 30 dB when the current is less than 5 mA. $LP_{11}$ is observed in the spectra and rapidly increases when the current exceeds 5 mA, and the SMSR between $LP_{01}$ and $LP_{11}$ is less than 25 dB. In this experiment, in order to obtain high single mode power, the diameter of the inner mode filter is 3 μm. The $LP_{11}$ will lase when the current is more than 5 mA, which is because when the diameter of dielectric film relief is 3 μm, it increases the size of the active area and the output power of the fundamental mode. But the 3 μm size dielectric film relief does not adequately suppress high-order modes, and high-order mode $LP_{11}$ will reach the threshold condition under high current injection and lase. $LP_{11}$ will lase and the wavelength of $LP_{11}$ is shorter than the fundamental mode wavelength when the current exceeds 5 mA, and the fundamental mode is no longer dominant. $LP_{01}$ and $LP_{11}$ will exist at the same time.

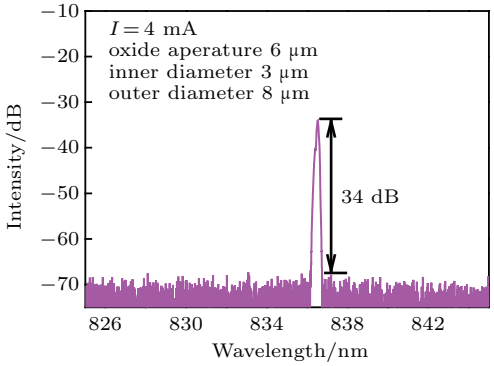


**Fig. 6.** (color online) Spectra of the VCSEL with a dielectric mode filter. The fabricated device is tested under $I = 4$ mA.

The measured near field patterns at different continuous-wave currents ($I = 2$, 3, and 4 mA) are shown in Fig. 7. On the basis of the near field patterns, we can see that only $LP_{01}$ mode appears at different currents. This result is in agreement with the measured results in Fig. 4. The introduced dielectric mode filter serves as a mode discriminator for the fundamental mode output. Consequently, the single mode is realized. The near field patterns prove that the dielectric mode filter provides mode selectivity to obtain the fundamental mode.

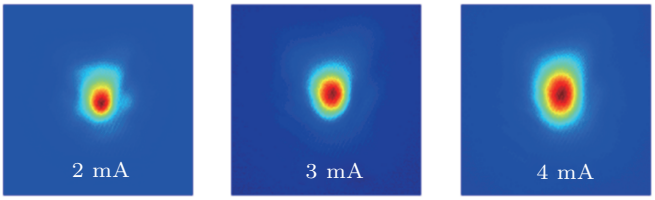


**Fig. 7.** (color online) Measured near field patterns under different continuous-wave currents $I = 2$, 3, and 4 mA.

## 4. Conclusion

We fabricate and measure VCSEL with a dielectric mode filter, which demonstrates a stable single mode performance. Measurements reveal that at continuous-wave current injection, the single-mode output power is 1 mW with the SMSR exceeding 30 dB throughout the current operating range (below 5 mA). The dielectric mode filter modifies the optical properties via antiphase reflections. Meanwhile, the method for the simple deposition and patterning of a single $SiO_2$ layer is deemed appropriate for VCSELs of any wavelength. Unlike other single-mode techniques, the proposed method could make device adjustment biased due to the thickness of the $SiO_2$ layer. Furthermore, the size of the pattern could be adjusted at any time via process variability. The dielectric mode filter could be patterned using a simple self-aligned photoresist process/etching process to improve reproducibility and yield in future single-mode technologies.

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