International Association of Scientific Innovation and Research (IASIR)
(An Association Unifying the Sciences, Engineering, and Applied Research)

ISSN (Print): 2279-0047
ISSN (Online): 2279-0055

International Journal of Emerging Technologies in Computational and Applied Sciences (IJETCAS)

www.iasir.net

Performance Enhancement and Characterization of Junctionless VeSFET

Tarun Chaudhary[1], Gargi Khanna[2]
[1,2] Department of Electronics and Communication Engineering
National Institute of Technology, Hamirpur (HP), INDIA

Abstract: *The design of double gate n-channel transistor named as junctionless vertical slit field effect transistor (JL VeSFET) is demonstrated in this paper. JLVeSFET is novel twin gate device which turns on and off depending upon the extension of depletion region from two gates inside the channel. It is observed that it offers very low OFF current with ideal subthreshold slope. JLVeSFET is compared with bulk MOSFETs at 65nm technology node. Characteristics of JLVeSFET with high-k dielectric are demonstrated through simulations in this paper. The device shows optimized performance with OFF current (~10^{-18}A/μm), high I_{on}/I_{off} (~10^{12}) and subthreshold slope of ~65mV/decade for a 50nm radius of simulated JLVeSFET*

Keywords: *JLVeSFET, Slit width, I_{on}/I_{off}, Ssub, DIBL, High –k dielectric.*

I. Introduction

The junctionless Vertical Slit Field Effect Transistor is a novel concept which provides new manufacturing and design paradigm. This JLT (junctionless transistor) based on the ideas and vision of Wojciech Maly is a promising device for future technology as it reduces the fabrication complexity as well as cost of fabrication, with the maintenance of design flexibility and inbuilt properties of power optimization in JLVeSFET [1]. To optimise the performance of JLT and to reduce the short channel effects in submicron technologies, new design approaches, such as, SOI JLFET, bulk planar JLFET, nanowire junctionless transistors [2-3], gate all around FET [4] etc, have been investigated to obtain a better gate control and improved performance. For V_{GS}=0V, junctionless transistor is in the OFF state with no current conduction path between source and drain, for this reason a very low OFF current is obtained. A study in [5] suggests that circuits implemented with JLVeSFET can have similar performance to CMOS circuits but occupy very small chip area. A junctionless transistor due to absence of sharp junctions provides better scalability and easy fabrication steps and offers many advantages which makes it suitable in ballistic transport at short channel lengths and as a future device for high speed memories [6].The simulation-based feasibility studies presented here are very promising and confirm many attractive properties of JLVeSFETs [7-8], such as very high I_{on}/I_{off} ratio, low leakage currents and effective current control by twin gate configuration. It has been found that the threshold voltage can be modified by either independently biasing two gates or by changing the doping levels, gate oxide thickness and slit width In the paper the structure and operation of junctionless vertical slit field effect transistor (JLVeSFET) are explained, the voltages of two gates TGC (tied gate configuration) is varied from 0 to V_{DD} to operate the device in ON and OFF mode. These devices exhibit high I_{on}/I_{off} ratio and subthreshold slope of 65mV/decade at room temperature. The working principle of VeSFET is similar to MOSFET and JFET which is explained in Section2. In Section3 the optimization of device characteristics are performed by introducing high-k gate dielectric, the variation of device characteristics at different gate doping concentration and different substrate doping concentration are also presented in Section 3. Section 4 presents the conclusion of the paper.

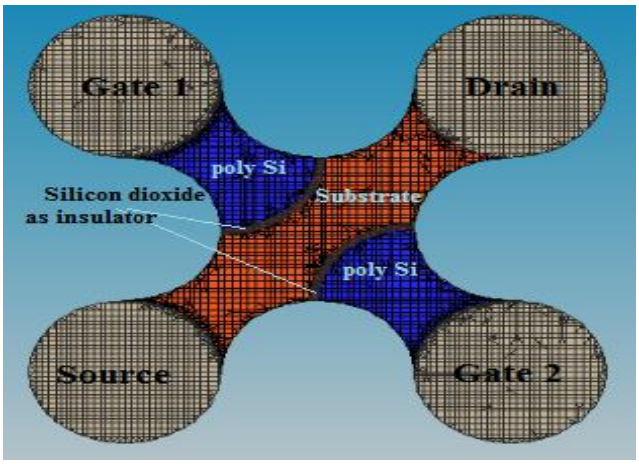

Fig. 1 Structure of n-channel double gate JLVeSFET with r=50nm and uniform channel doping of 1×10^{17} cm^{-3}

II. Device Structure and Operation

The JLVeSFET is a junctionless transistor with a gate controlled bulk current using either a p-type or n-type substrate for the complementary transistor types. The device is hybrid of JFET and MOSFET. The operation is JFET-like because it is based on transport of majority carriers in a bulk channel, whose effective width is controlled by depleted regions induced by two gates on both sides of this channel. The gates, however, are separated from the channel by a layer of oxide, like in a MOSFET [9].

Fig. 1 shows the structure of JLVeSFET that we use for simulation and the device comprises of source, drain and channel region with same dopants. It is a gated resistor in which the current is controlled by depletion regions created by the two gates on either side of the channel. In the OFF state, the depletion region, created due to the work function difference between the channel and the gate material, packs up the channel completely, leading to low OFF current. In the ON state, when a voltage is applied on the gate to counter the work function difference, the depletion region recedes and a path is created for the current to flow between source and drain. VeSFET exhibits majority carrier flow unlikely MOSFET that exhibit minority carrier flow [7]. All relevant parameters considered for simulations are listed in Table 1

Table 1: Parameters used for device simulation

Parameters	Value
Radius of metal pillars	50nm
Radius of STI fillers	50nm
Thickness of gate dielectric (t_{ox})	3nm to 4nm
Slit width (W_s)	37.9nm
Height of the device (h)	200nm
Substrate doping (N_{sub})	1×10^{16} cm^{-3} to 1×10^{18} cm^{-3}
Polysilicon gate doping (N_{Poly})	1×10^{18}cm^{-3} to 1×10^{20} cm^{-3}
Gate voltage for G1 and G2(TGC)	1V
Drain bias (V_{ds})	1V
High- k dielectric (Si_3N_4)	k=7.5
Low-k dielectric (SiO_2)	k=3.9

All simulations are carried out using Sentaurus TCAD [10]. The I_D-V_{GS} plot for JLVeSFET is shown in Fig. 2 for different values of V_{DS} and it shows the effect of DIBL short channel effect on the device. The simulated result shows very less variation in ON current with increase in drain voltage. The simulated device structure is a vertical n-type JLT with two gates, named gate1 and gate2. The voltage is sweeped at both the gates simultaneously (TGC) from 0 to V_{DD} for turning the device ON.

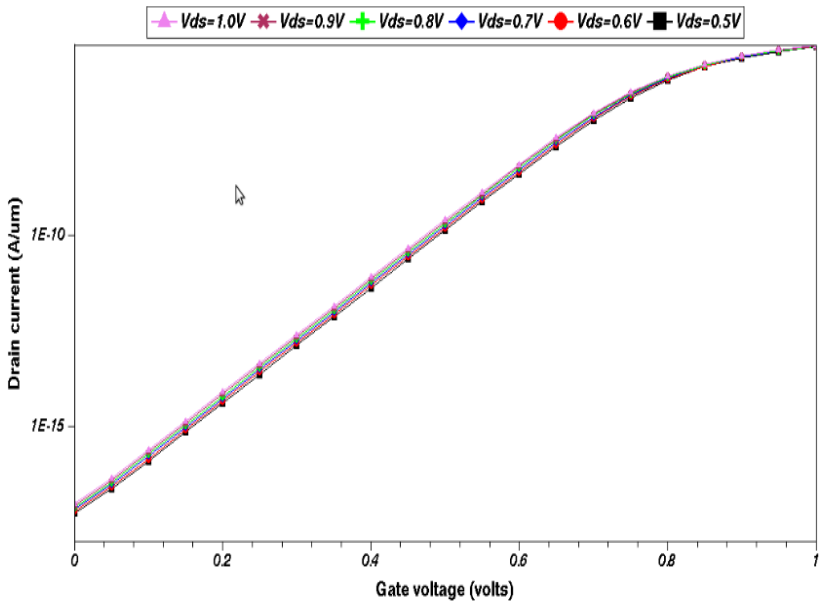

Fig. 2 I_D-V_{GS} plot for JLVeSFET with r=50nm, w_s=37.9nm t_{ox} = 4nm and V_{DS}=1.0V

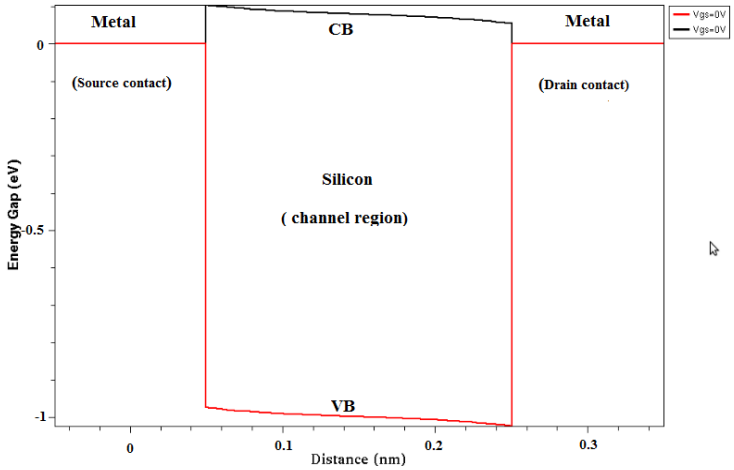

Fig. 3 Energy band diagram of OFF state of the JLVeSFET with V_{GS}=0V

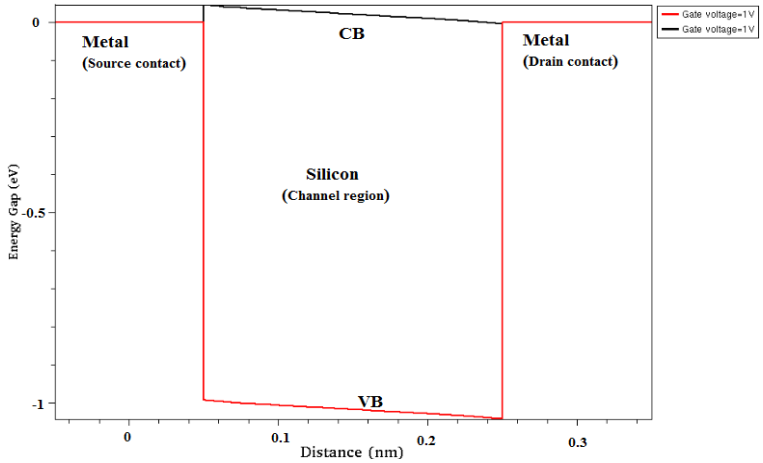

Fig. 4 Energy band diagram of JLVeSFET with V_{DS}=0V and V_{GS}=1V

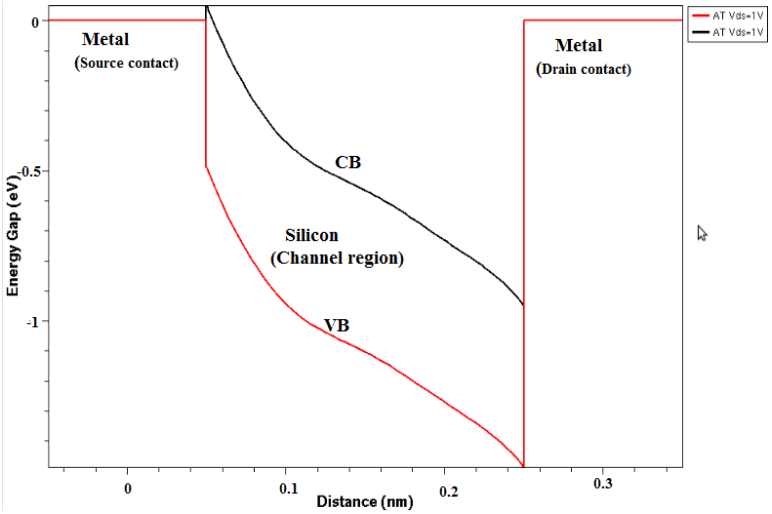

Fig. 5 Energy band diagram of JLVeSFET with V_{DS}=1V and V_{GS}=1V

In order to achieve low subthreshold swing, the device is made without any sharp junctions (ultra steep doping profile) [6] which reduces the need of high and different doping profiles. In order to get the better control of gate on output, material with high-k dielectric (Si_3N_4, k=7.5) is utilized. Through simulations it is obtained that use of high-k material results in optimized low subthreshold swing of 63mV/decade and low OFF current of ~10^{-18}Amp at room temperature When positive gate voltage is applied to TGC JLVeSFET the device turns ON, with variation in the gate voltage from 0V to 1V, band bending occurs and continuous path for current to flow between source and drain of the device occurs as shown in Fig. 3, 4 and 5. All simulations are carried out by taking the gate doping concentration to be $1\times10^{19}cm^{-3}$. The gate work function is 4.25eV for gate1 and

gate2 with gate material as poly silicon. A key issue of JLVeSFET is to optimize the I_{on}/I_{off} ratio and to get minimized subthreshold swing comparable to subthreshold slope of MOSFET at 65nm technology node. The device JLVeSFET device demonstrates a subthreshold slope of 65mV/decade with SiO_2 as oxide, whereas it is between 70-100 mV/decade as reported in [12] for MOSFET.

Fig. 6 represents the energy band diagram of both the oxide regions at two gates of TGC and the silicon channel in between, it is clear from the energy band diagram that due to very high band gap ≈ 8eV there is no current conduction through the oxide region, thus this leads to the reduction of gate leakage current which occurs due to tunneling through the oxide region and also inhibit the hot carrier injection in the JLVeSFET device and thus the device is suitable for low power applications.

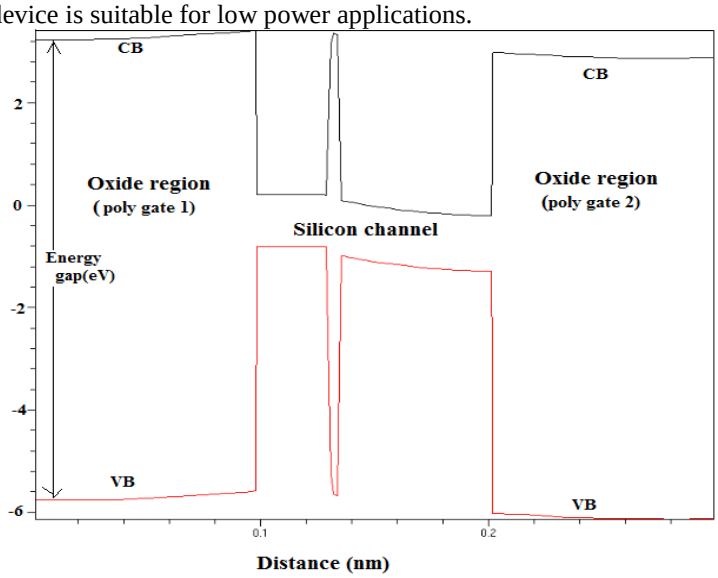

Fig. 6 Energy band diagram of JLVeSFET considering two insulators and silicon channel in between

III. Results and Discussion

A. Simulation Parameters

The n channel VeSFET device at radius of 50nm is simulated using Sentaurus TCAD device simulator. The height of the device is 200nm, gate oxide thickness is 4nm, the substrate doping concentration is 1×10^{17} cm^{-3} and boron concentration for twin gate structure is 1×10^{19} cm^{-3} . The device is operated at 1.0V for TGC structure.

B. High-k gate dielectric with Low- k STI filler

An improved double gate (DG) JLVeSFET with superior performance is observed by the use of high k dielectric (in this simulation Si_3N_4 with a dielectric constant, k=7.5), with low-k STI fillers (we use SiO_2 with k=3.9). The simulation results show that by proper choice of suitable gate dielectric and fillers I_{on}/I_{off} ratio ~10^{11} and low subthreshold slope ~ 63mV/decade is achieved as shown in Fig. 7 .

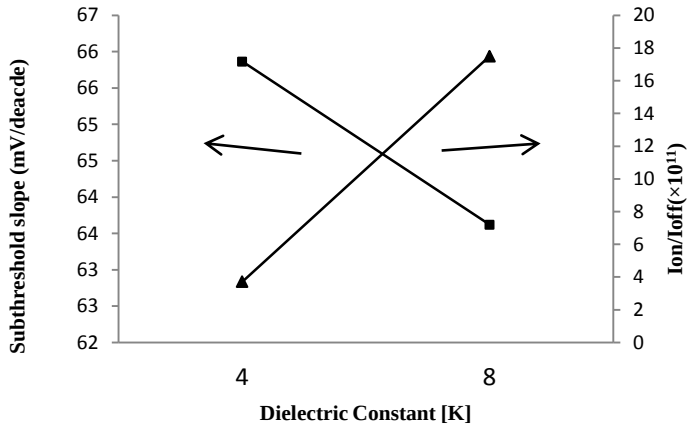

Fig. 7 Subthreshold slope and I_{on}/I_{off} dependence on gate dielectric constant for r=50nm, w_s=37.9nm, t_{ox}=4nm and V_{DS}=1V

High-k dielectric is used to enhance gate control and STI filler are used to separate the three regions so that proper isolation can be maintained. In Fig. 7 both I_{on}/I_{off} and subthreshold slope are plotted for two different dielectric constant materials. The simulation result shows that, with increase of gate dielectric constant, OFF current reduces considerably, where as ON current remains almost constant. Hence I_{on}/I_{off} increases by a factor of

~10 with increase in dielectric constant from 3.9 to 7.5. Fig. 7 shows that I_{on}/I_{off} increases from 3.72×10^{11} to 17.5×10^{11} with increase in gate dielectric from 3.9 (SiO_2) to 7.5 (Si_3N_4) respectively.

The JLVeSFET shows a significant improvement by lowering the subthreshold slope below 65mV/decade. When the gate dielectric constant increases, there is a drop in subthreshold slope from 65mV/decade at k=3.9 to 63mV/decade at k=7.5.The I_D-V_{GS} plot for different gate dielectric constants is shown in Fig. 8. The results show that the OFF current is greatly dependent on the dielectric constant. When the dielectric constant increases, the OFF current reduces while there is a negligible change in ON current. In our simulations, we use Si_3N_4 (k=7.5) as high-k dielectric and compare it with SiO_2 whose dielectric constant is 3.9, the OFF current reduces by the factor of 4.

C. ***Dependence of Device Charcteristics on Doping Variations***

Fig. 8 and 9 show the variation of device characteristics such as I_{on}, Ion/I_{off}, subthreshold slope and DIBL with doping concentration. In this work gate doping is varied from $1\times10^{18}cm^{-3}$ to $7\times10^{19}cm^{-3}$. The thickness of slit width is 37.9nm, besides with increase in channel doping the OFF current reduces whereas ON current reduces as well, subthreshold slope remains almost constant and DIBL value is reduced from 58mV/V to 40mV/V, which shows that the effect of drain bias voltage on the ON current reduces and gate control over the channel enhances as we increase gate doping concentration. The I_{on}/I_{off} ration is increases from 2.34×10^{10} to 0.84×10^{12} with increase in gate doping concentration.

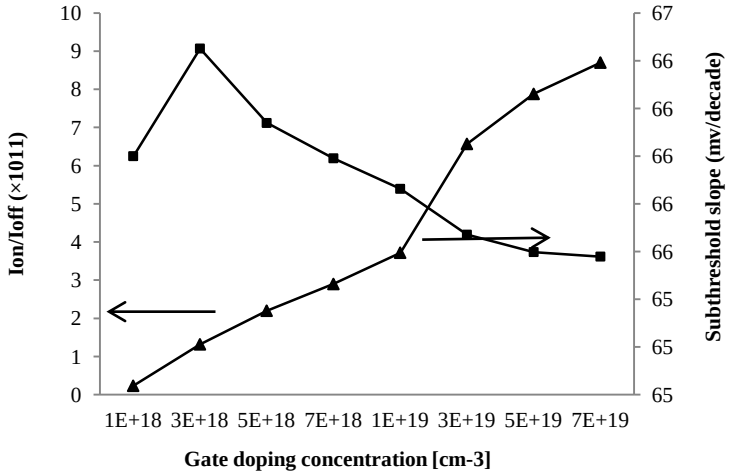

Fig. 8 I_{on}/I_{off} ratio and subthreshold slope dependence on gate doping variation for r=50nm, t_{ox}=4nm channel doping=$1\times10^{17}cm^{-3}$and w_s=37.9nm

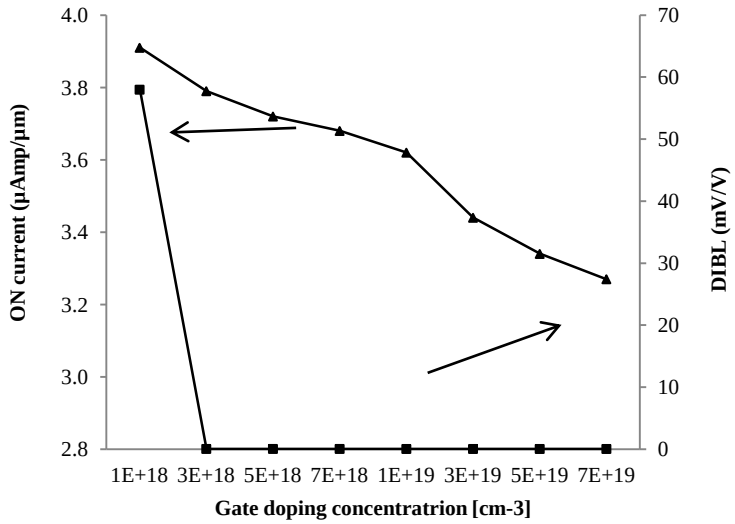

Fig. 9 ON current and DIBL dependence on gate doping variation for r=50nm, t_{ox}=4nm

Fig.10 shows the effect of variation in channel doping concentration ($1\times10^{16}cm^{-3}$ to 1×10^{18} $cm^{-3)}$, on the device electrical parameters, such as I_{on}/I_{off} ratio and subthreshold slope. Subthreshold slope has shown significant reduction from 300mV/decade to 65mV/decade, and remains almost constant with reduction from $5\times10^{17}cm^{-3}$ to $1\times10^{16}cm^{-3}$ in channel doping concentration.

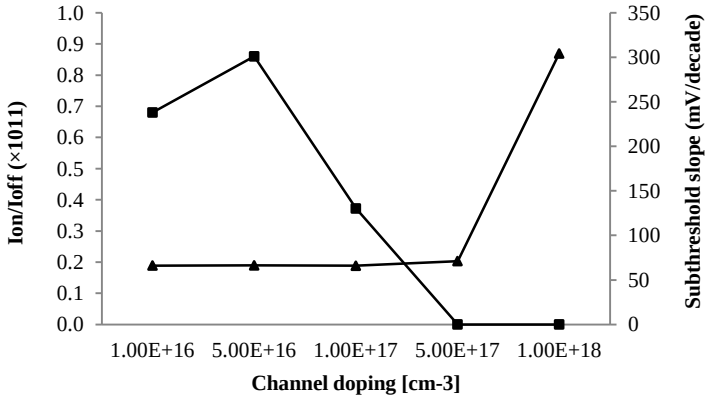

Fig. 10 I_{on}/I_{off} ratio and subthreshold slope dependence on channel doping variation for r=50nm, t_{ox}=4nm gate doping=$1\times10^{19}cm^{-3}$, w_s=37.9nm and h=200nm

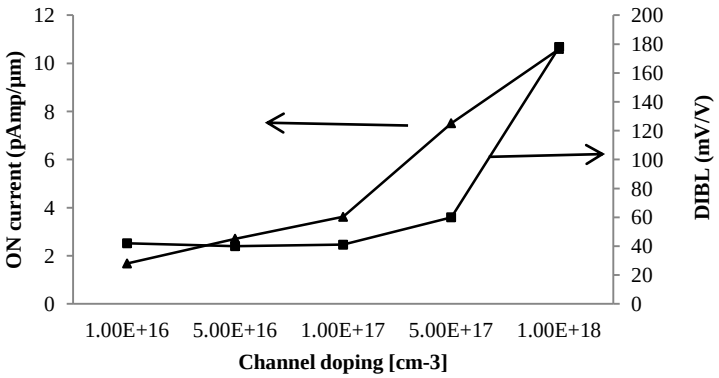

Fig. 11 ON current and DIBL dependence on channel doping variation for r=50nm, t_{ox}=4nm gate doping=$1\times10^{19}cm^{-3}$, w_s=37.9nm and h=200nm

Fig. 11 describes the reduction of ON current and reduction in DIBL (drain induced barrier lowering) with decrease in channel doping concentration. Significant reduction has been seen from 170mV/V to 42mV/V with reduction in doping concentration from $1\times10^{18}cm^{-3}$ to $1\times10^{16}cm^{-3}$.

IV. Conclusion

In this work, the proposed device is simulated with variation in different device parameters and it has been observed that the characteristics of JLVeSFET are comparable to conventional MOSFET without the need of any junction. The device shows minimum gate tunneling current and when observed with high-k dielectric material (Si_3N_4) and low –k STI fillers (SiO_2) with optimised gate doping concentration and channel doping concentration it offers OFF current of $\sim10^{-18}$ A/µm, I_{on}/I_{off} ratio of $\sim10^{12}$ order and a subthreshold slope as low as ~65mV/decade. Such low and optimised value signifies its importance both in addressing fabrication issues and low power applications

V. References

[1] W. Maly, " Integrated Circuits Fabrication and Associated Methods Devices and Systems", U.S. Non-Provisional Patent Application serial Number CMU Docket 06-091; DMC Docket 06-001PCTCMU
[2] Lee C.W., Ferain, I., Kranti, A., DehdashtiAkhavan, N., Razavi, McCarthy, B., Gheorghe, S., Murphy, R., Colinge, J.P Short-channel junctionless nanowire transistors. In: Proc. SSDM, pp. 1044–1045 (2010)
[3] Kranti, A., Yan, R., Lee, C.-W., Ferain, I., Yu, R., DehdashtiAkhavan, N., Razavi, P., Colinge, J.P.: Junctionless nanowire transistor(JNT): properties and design guidelines. In: Proceedings of theEuropean Solid-State Device Research Conference (ESSDERC),April 2010, pp. 357–360 (2010)
[4] Su, C.-J., Tsai, T.-I., Liou, Y.-L., Lin, Z.-M., Lin, H.-C., Chao,T.-S.: Gate-all-around junctionless transistors with heavily doped polysilicon nanowire channels. IEEE Electron Device Lett. **32** (4) (2011)
[5] Y-W. Lin, M. Marek-Sadowska, W. Maly, A. Pfitzner and D.Kasprowicz, "Is There Always Performance Overhead for Regular Fabric?" *Proc. ICCD*, pp. 557-562, October 2008.
[6] Ghosh B., Bal.P., M Partha., " A junctionless tunnel field effect transistor with low subthreshold slope", J Comput Electron (2013) 12: 428-436
[7] W. Maly and A. Pfitzner, "Complementary Vertical Slit Field Effect Transistors", Carnegie Mellon University, Techreport No. CSSI 08-02, 01/2008.
[8] http://vestics.org
[9] W Marcus., A Pfitzer., D Kasprowicz., R Emling., W Maly., D Schmitt., "Adder circuits with transistor using Independently controlled gates" IEEE 2009.
[10] "Sentaurus Structure Editor User's Manual", Synopsys International
[11] "Sentaurus Inspect User's Manual", Synopsys International