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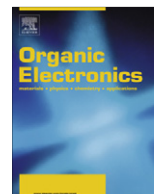

Interfacial dipole in organic p–n junction to realize write-once–read-many-times memory

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ABSTRACT

A new approach is exploited to realize nonvolatile organic write-once–read-many-times (WORM) memory based on copper phthalocyanine (CuPc)/hexadecafluoro-copper-phthalocyanine ($F_{16}CuPc$) p–n junction. The as-fabricated device is found to be at its ON state and can be programmed irreversibly to the OFF state by applying a negative bias. The WORM device exhibits a high ON/OFF current ratio of up to 2.6×10^4. An interfacial dipole layer is testified to be formed and destructed at the p–n junction interface for the ON and OFF states, respectively. The ON state at positive voltage region is attributed to the efficient hole and electron injection from the respective electrodes and then recombination at the CuPc/$F_{16}CuPc$ interface, and the transition of the device to the OFF state results from the destruction of the interfacial dipole layer and formation of an insulating layer which restricts charge carrier recombination at the interface.

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1. Introduction

In recent years, organic resistive memory devices in which the active organic materials process at least two stable resistance states have been extensively investigated due to their simplicity in device structure, good scalability, low-cost potential, low-power operation, and large capacity for data storage [1–15]. There are three types of organic memory devices: random access memory, read–write–erase–rewritable memory, and write-once–read-many-times (WORM) memory. WORM memory is a type of nonvolatile memory that is capable of storing data permanently and being read from repeatedly. Thus it bears the potential application for permanent data storage, such as wireless identification tags, smart cards, and personal data depositories. A wide variety of materials, such as small molecular organic material [16,17], polymer [18–20], organic/inorganic heterojunction [21,22], conjugated copolymer [23], organic donor/acceptor composite [24], have been explored for organic WORM memory. Correspondingly, the mechanisms accounting for the transition between the high conductivity (ON) and low conductivity (OFF) states include charge carrier traping and detraping [16–18], filament formation and destruction [19], conformation change [20], oxidation/reduction reaction [21,22], charge-transfer complex formation [23,24], and etc.

Organic p–n junction has attracted much interest in relation to the rapid development of the organic optoelectronic devices, such as organic light-emitting diodes [25], solar cells [26], photodetectors [27], and field-effect transistors [28]. Band bending and interfacial dipole are often found in organic/organic p–n junctions, and such effects play crucial roles in determining the performance of the multilayer organic optoelectronic device [29–32]. Copper phthalocyanine (CuPc) and hexadecafluoro-copper-phthalocyanine ($F_{16}CuPc$) are hole and electron transporting materials, respectively, with high field-effect mobilities both in the order of 10^{-2} $cm^2/(V\,s)$ as well as excellent thermal stability [33,34]. Lin and Ma have observed WORM

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memory characteristic in CuPc by controlling the evaporation rate and the ON/OFF transition was proposed to be managed by charge carrier traping and detraping [17]. Choi et al. have observed WORM memory characteristics based on a hyperbranched CuPc polymer, and the ON/OFF transition was proved to be governed by the rupture of filaments [19]. In a previous work, we have demonstrated an organic WORM memory in device indium tin oxide (ITO)/F_{16}CuPc/Al with an ON/OFF current ratio of 2.3×10^3, and the ON/OFF transition results from the formation and destruction of the interfacial dipole layer formatted in the ITO/F_{16}CuPc interface [35].

In this study, a nonvolatile organic WORM memory device based on CuPc/F_{16}CuPc p–n junction is demonstrated. The device shows an ON/OFF current ratio in the order of 10^4. And a new mechanism is proposed to govern the conductivity transition. The ON state of the WORM device is attributed to the low barrier for charge carriers injection and then recombination at the CuPc/F_{16}CuPc p–n junction interface. The transition from the ON state to the OFF state by applying a negative bias results from the destruction of the interfacial dipole layer which forms an insulating layer and hence restricts charge carriers recombination in organic layers.

2. Experimental details

Devices were fabricated on patterned ITO coated glass substrates with a sheet resistance of 15 Ω/sq. The substrates were routinely cleaned and treated in an ultraviolet–ozone environment for 10 min before loading into a high vacuum chamber. Organic layers and Al cathode were deposited onto the substrates via thermal evaporation at 5×10^{-4} Pa. Two devices with the configurations were fabricated as follows:

- Device A: ITO/CuPc (40 nm)/F_{16}CuPc (40 nm)/Al (100 nm)
- Device B: ITO/CuPc (30 nm)/4,7-diphenyl-1,10-phenanthroline (Bphen, 20 nm)/F_{16}CuPc(30 nm)/Al (100 nm)

Deposition rates and thickness of the layers were monitored in situ using oscillating quartz monitors. The evaporating rates were kept at 0.5–1 Å/s for organic layers and 10 Å/s for Al cathode, respectively. Fig. 1 shows the schematic energy level diagram of Device A. The energy level alignments at the ITO and Al electrodes are cited from Refs. [36,37], respectively, while the others from Ref. [38]. The contributions of band bending, interfacial dipole, and chemical reaction to the vacuum level (E_F) shift are not distinguished at the interfaces. Current–voltage (J–V) characteristics of the devices were measured with a Keithley 2400 power supply and were recorded simultaneously with measurements. The forward electric voltage is defined as that the ITO electrode is positive biased. To investigate the interface proprieties of CuPc/F_{16}CuPc, X-ray diffraction (XRD) patterns of the ITO/CuPc/F_{16}CuPc film before and after conductivity transition in Device C with the structure of ITO/CuPc (40 nm)/F_{16}CuPc (40 nm)/poly (ethylene oxide) (PEO)/Al (100 nm) were measured. To carry out these experiments, Al cathode was peeled off. Thin

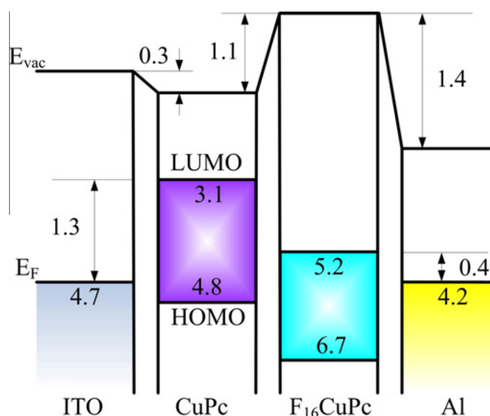

Fig. 1. Schematic energy level diagram of Device A: ITO/CuPc/F_{16}CuPc/Al. All the values shown are in unit of eV. E_{vac}, E_F, LUMO, and HOMO denote the vacuum level, Fermi level, the lowest unoccupied molecular orbital, and the highest occupied molecular orbital, respectively.

PEO layer has been adopted as the cathode buffer layer to improve the performance of organic solar cells [39]. Here it was used as the cathode buffer layer to facilitate the peeling off of the Al cathode by a dilute NaOH solution. Al cathode can be peeled off easily while keeping the CuPc/F_{16}CuPc interfacial properties unaffected. PEO layer was spin-coated onto F_{16}CuPc with a speed of 2000 rpm from aqueous/isopropanol (1:4 by volume ratio) with a concentration of 3 mg/ml followed by baking in vacuum at 60 °C for 1 h. XRD patterns were measured with a Burker D8 Focus diffractometer using Cu Kα radiation (λ = 1.54056 Å). All the measurements were carried out at room temperature under ambient conditions (temperature of ~20 °C and relative humidity of 20–30%) without encapsulation.

3. Results and discussion

Fig. 2 depicts the J–V curves of Device A: ITO/CuPc/F_{16}CuPc/Al. The as fabricated device remains in the ON state for the first voltage sweep from 0 to 10 V and for the second one from 0 to −7.6 V. However, with further increase

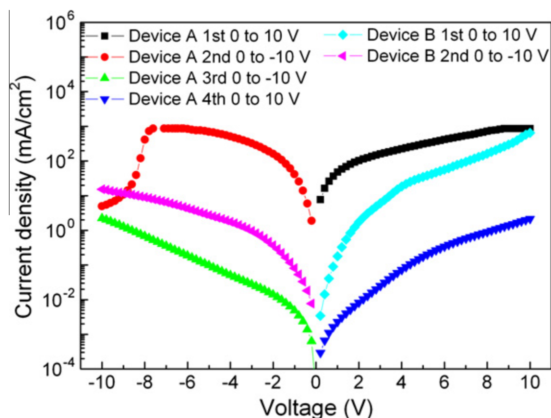

Fig. 2. J–V curves of Device A: ITO/CuPc/F_{16}CuPc/Al and Device B: ITO/CuPc/Bphen/F_{16}CuPc/Al.

of the reverse voltage from −7.6 to −10 V, the current density decreases gradually and a negative differential resistance (NDR) region appears, indicating that the device switches from the ON state to the OFF state. Such a transition corresponds to the "writing" process of a digital memory cell. After this voltage sweep, the device remains in the OFF state for the latter voltage sweeps in both the positive and negative voltage regions, and it cannot be recovered to the ON state again. Moreover, it is found that the ON/OFF transition in the negative voltage region is independent to the voltage sweep sequence, that is, the ON/OFF transition can also be observed if the first voltage sweep is performed from 0 to −10 V (not shown here). Such a finding rules out that the ON state and the NDR are correlated to the voltage sweep in the positive voltage region. Besides, it is interesting to note that the ON state current at negative bias is a little higher than at the positive bias at a given voltage. From the ON and OFF states current at positive voltage region, a maximum ON/OFF current ratio that reaches up to 2.6×10^4 is obtained. Compared with the ITO/F_{16}CuPc/Al single layer WORM memory device reported previously [35], the introduction of CuPc layer forms a p–n junction with F_{16}CuPc, which dramatically improves the hole injection efficiency into the device when it is positive biased. Thus the ON state current of the p–n junction memory device is one order of magnitude higher than that of the single layer device, which boosts the ON/OFF current ratio to the order of 10^4. The increased ON/OFF current ratio would significantly eliminate the memory error and elevate the reliability of the memory device for practical applications.

The ON and OFF states retention time of Device A is shown in Fig. 3. Both the ON state and OFF state current densities were measured by applying a constant voltage of 0.5 V to the device with a time interval of 1 s. As the number of the measured data points is limited by the software of our measurement equipment, only the retention time of 1000 s is provided here. It can be found that the ON state and OFF state current densities are almost invariable during 1000 s. Besides, an ON/OFF current ratio of about 9×10^3 can even be observed in the device after it is stored in air for 1 week (no shown here). This finding indicates that the device presents a good stability and such a property is more important for practical applications.

To explore the working mechanisms of the WORM device, Device B with a structure of ITO/CuPc/Bphen/F_{16}CuPc/Al was fabricated. Inserting a Bphen layer between CuPc and F_{16}CuPc is to preventing the formation of the CuPc/F_{16}CuPc p–n junction. As can be found in Fig. 2, no conductivity transition is found in Device B during the voltage sweeps. This finding implies that the ON/OFF transition in Device A is governed by the CuPc/F_{16}CuPc p–n junction rather than the ITO/CuPc and F_{16}CuPc/Al interfaces as well as the CuPc and F_{16}CuPc bulk properties. Besides, the current density of Device B is on the intermediate state between the ON and OFF states of Device A. Moreover, the reverse current is lower than the forward one at a given voltage, suggesting that a rectifying *J–V* characteristic presents in Device B.

To investigate the interface proprieties of CuPc/F_{16}CuPc in Device A before and after conductive transition, XRD patterns were investigated. To carry out the experiments, Al cathode should be peeled off. Water-soluble PEO layer was adopted as the cathode buffer layer in Device C to facilitate the peeling off of the Al cathode by a dilute NaOH solution. The introduction of the PEO cathode buffer layer preserves the WORM memory character in Device C, as shown in Fig. 4, which further confirms that the conductivity transition is not managed by the F_{16}CuPc/Al interface. In addition, both the ON and OFF states current are lower than that of Device A, and the ON states current at positive region is higher than that at negative region which is contrary to Device A. Such differences should be engendered by the introduction of the PEO layer, which may form an extra barrier for holes and electrons to inject from Al cathode especially for holes when the device is negative biased.

Fig. 5 reveals the XRD patterns of glass/ITO/CuPc, glass/ITO/CuPc/F_{16}CuPc, and glass/ITO/CuPc/F_{16}CuPc films in Device C before and after the conductivity transition, for reference, small angle XRD patterns of quartz/CuPc and quartz/CuPc/F_{16}CuPc films are also provided. No discernable structure is found in both the quartz/CuPc and

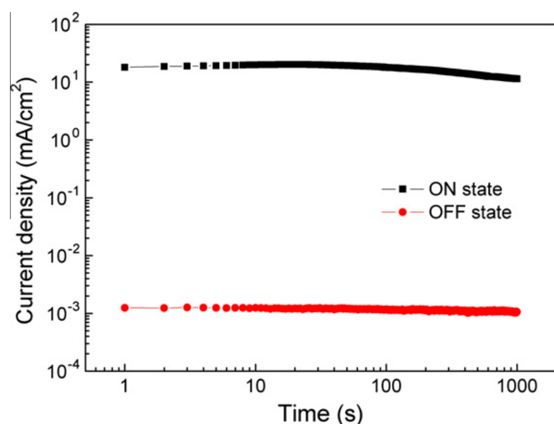

Fig. 3. Retention stability of the ON and OFF states of Device A: ITO/CuPc/F_{16}CuPc/Al under constant bias of 0.5 V.

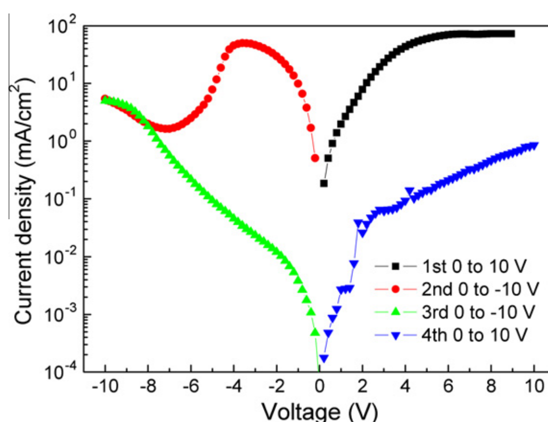

Fig. 4. *J–V* curves of Device C: ITO/CuPc/F_{16}CuPc/PEO/Al.

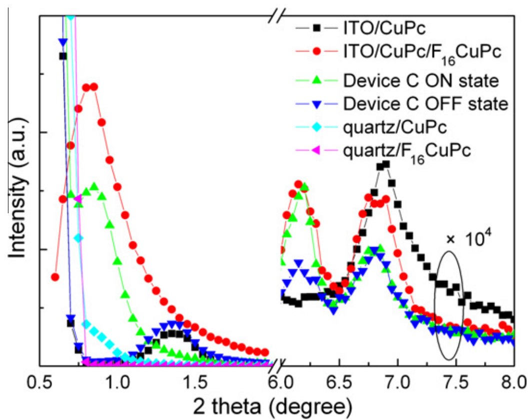

Fig. 5. XRD patterns of the glass/ITO/CuPc/F_{16}CuPc films in Device C before and after conductivity transition, as well as the glass/ITO/CuPc, glass/ITO/CuPc/F_{16}CuPc, quartz/CuPc, and quartz/CuPc/F_{16}CuPc films.

quartz/CuPc/F_{16}CuPc films at small angle, indicating that neither the bulk property of CuPc nor that of F_{16}CuPc can produce diffraction peak at small angle. On contrast, strong diffraction peaks at small angle and weak ones at large angle are discovered for all the other four samples. The diffraction peaks at 2θ of ca. 6.15° and 6.85° are attributed to the diffraction of the (200) lattice planes of F_{16}CuPc and CuPc, respectively [33,34]. Band bending and an interfacial dipole layer were observed at the CuPc/F_{16}CuPc interface due to the electron transfer from CuPc to F_{16}CuPc, which results in holes and electrons accumulation in CuPc and F_{16}CuPc, respectively [38,40,41]. Such an energy level alignment makes it beneficial to be used as the active materials in organic field-effect transistors [28] and as the connection unit in tandem organic light emitting diodes [42]. Charge carriers are known to accumulate in organic layers in the form of polaron. A polaron is a charge plus a distortion of the charge's surroundings. Putting a charge onto a certain organic molecular site can deform the whole molecule. Such deformation of the organic molecule may form an ordered structure of the molecules in the interface, which can be detected by XRD with diffraction peak at small angle [43]. Thus the diffraction peak at $2\theta = 1.35°$ in the glass/ITO/CuPc film and Device C after conductivity transition is a consequence of the interfacial dipole layer formed in ITO/CuPc, while the one at $2\theta = 0.83°$ in the glass/ITO/CuPc/F_{16}CuPc film and Device C before conductivity transition results from the interfacial dipole layer formed in CuPc/F_{16}CuPc. It should be noted that the diffraction peak at 1.35° is not observed in the glass/ITO/CuPc/F_{16}CuPc film and Device C before conductivity transition. Such a phenomenon may be ascribed to the high intensity of the diffraction at 0.83°, which conceals the diffraction at 1.35°. The XRD results indicate that the interfacial dipole layer of CuPc/F_{16}CuPc is destructed while the ITO/CuPc one is unaffected by the conductivity transition. Combining with the results found in the *J*–*V* curves, it comes to the conclusions that the conductivity of Device A is controlled by the CuPc/F_{16}CuPc interfacial dipole layer, and such a layer interfacial dipole layer is destructed by applying a negative bias.

In order to further understand the conduction mechanisms of the WORM device, the *J*–*V* characteristics of Device A are fitted by different current transport models. Fig. 6 shows the experimental and theoretical fitting curves of the ON and OFF states current in positive voltage region. Both the ON and OFF states current at low positive voltage can be well fitted by a Schottky emission model:

$$J = A^{*}T^{2}\exp\left[\frac{-(\phi_b - \sqrt{q^3V/4\pi\varepsilon_0\varepsilon_r d}}{k_bT}\right] \quad (1)$$

where A^{*} is the effective Richardson constant, T is the temperature, ϕ_b is the barrier height, q is the electron charge, ε_0 is the permittivity of the vacuum, ε_r is the relative permittivity of the organic semiconductor, d is the thickness of the organic layer, and k_b is the Boltzmann constant. As shown in Fig. 6a, a linear relation between log$J$ and $V^{1/2}$ is obtained for both the ON and OFF states current, indicating that the current is predominantly injection limited which is determined by the electrode/organic properties. Meanwhile, both the ON and OFF states current at high positive voltage compliance with a trap-limited space charge limited current (SCLC) model:

$$J = q\mu_0 N_c\left(\frac{\varepsilon_0\ \varepsilon_r}{q\ N_t}\frac{l}{l+1}\right)^{l}\left(\frac{2l+1}{l+1}\right)^{l+1}\frac{V^{l+1}}{d^{2l+1}} \quad (2)$$

where μ_0 is the trap-free mobility, N_c is the effective density of states in the transport level, N_t is the total trap density, and $l = E_b/k_bT$ where E_b is the characteristic energy. A linear relation between log$J$ and log$V$ is found and the slopes are 1.8 and 3.5, respectively, for the ON and OFF states, as shown in Fig. 6b. These findings suggest that both the ON and OFF states current transit from the Schottky emission model at low bias to the trap-limited SCLC model at high bias. Moreover, it should be noted that the threshold voltage of the transition is lower for the OFF state, indicating that charge carriers are more favorable to be trapped in the organic layers at OFF state.

The ON state current in negative voltage before conductivity transition can also be fitted by the trap-limited SCLC model and a linear relation between log$J$ and log $|V|$ is found with a slope of 1.8, as shown in Fig. 7a. Such a finding indicates that the ON state current at negative voltage is not injection limited but bulk transport limited, which is governed by the bulk properties of CuPc and F_{16}CuPc, and/or the interfacial properties of CuPc/F_{16}CuPc. The hole injection barrier at F_{16}CuPc/Al and the electron injection barrier at ITO/CuPc are 1.1 and 1.3 eV, respectively (as shown in Fig. 1). The high injection barriers of hole and electron are contrary to the high conductivity found in the negative bias of Device A, which will be discussed later. Chiguvare et al. [44] have proposed that when the barrier height is larger than k_bT, the current should be dominated by the tunneling model. Thus the OFF state current at negative voltage should follow the tunneling model. At low voltage, the tunnel barrier is trapezoidal and the *J*–*V* follows direct tunneling model [45,46]:

$$J \propto V\exp\left(-\frac{2d\sqrt{2m\phi_b}}{\hbar}\right) \quad (3)$$

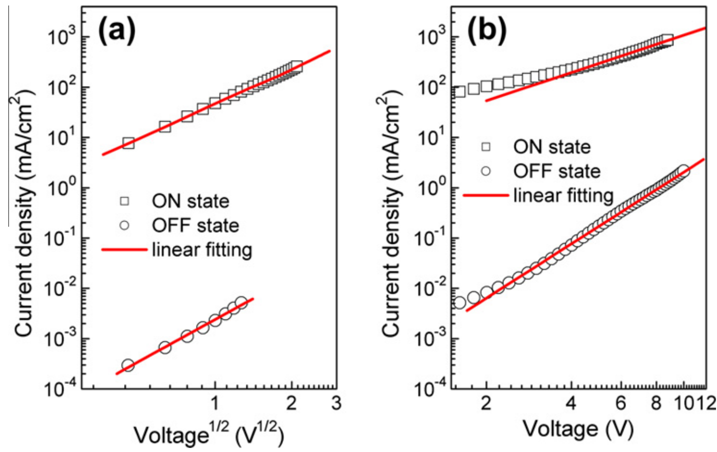

Fig. 6. (a) J versus $V^{1/2}$ plots of the ON and OFF states of Device A: ITO/CuPc/F_{16}CuPc/Al at low positive voltage. (b) Log–log plots of the ON and OFF states current of Device A at high positive voltage. The lines present the linear fitting of the data.

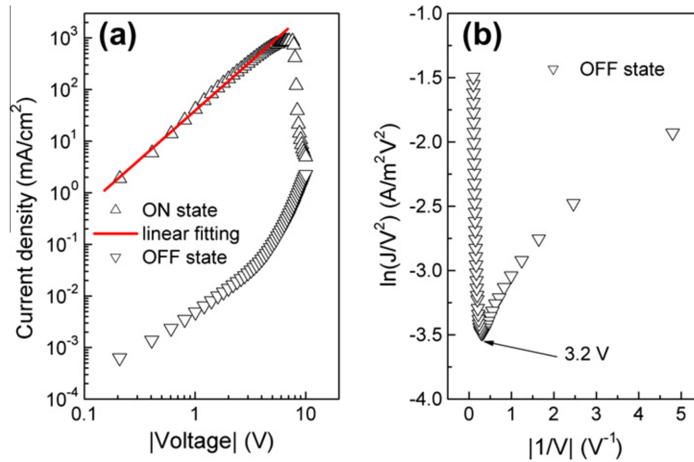

Fig. 7. (a) Log–log plots of the ON and OFF states current of Device A: ITO/CuPc/F_{16}CuPc/Al at negative voltage, the line presents the linear fitting of the data. (b) A ln(J/V^2) versus $|1/V|$ plot of the OFF state current of Device A at negative voltage.

where m is the effective mass of the charge carrier and $\hbar$ is Planck's constant divided by 2π. At high voltage, the tunnel barrier becomes triangular and the J–V follows Fowler–Nordheim (F–N) tunneling model [45,46]:

$$J \propto V^2 \exp\left(-\frac{4d\sqrt{2m\phi_b^3}}{3\hbar qV}\right) \tag{4}$$

The above J–V relations in Eqs. (3) and (4) can be liberalized in a logarithm scale to become Eqs. (5) and (6), respectively:

$$\ln\left(\frac{J}{V^2}\right) \propto \ln\left(\frac{1}{V}\right) - \frac{2d\sqrt{2m\phi_b}}{\hbar} \tag{5}$$

$$\ln\left(\frac{J}{V^2}\right) \propto -\left(\frac{1}{V}\right)\left(\frac{4d\sqrt{2m\phi_b^3}}{3\hbar q}\right) \tag{6}$$

Fig. 7b shows a ln(J/V^2) versus $|1/V|$ plot of the OFF state current at negative voltage. An inflection point at voltage of −3.2 V is observed in the curve. Such a character indicates that the current model transition from a direct tunneling model at low voltage (0 to −3.2 V) to an F–N tunneling model at high voltage (−3.2 to −10 V), corresponding to a change of the sharp of the tunnel barriers from trapezoidal to triangular [46]. If the current could be solely determined by the direct tunneling model at low voltage and the F–N tunneling model at high voltage, a linear relation of ln(J/V^2) against ln($|1/V|$) and ln(J/V^2) against $|1/V|$ should be found, respectively. Fig. 8a and b shows the linear fittings of the current in a ln(J/V^2) versus ln($|1/V|$) plot at low voltage and a ln(J/V^2) versus $|1/V|$ plot at high voltage, respectively. As shown in the figures, small deviations of the current from the linear relationships are found. CuPc and F_{16}CuPc are hole and electron transporting materials, respectively. Thus after electrons and holes have been injected from the electrodes, they will be accumu-

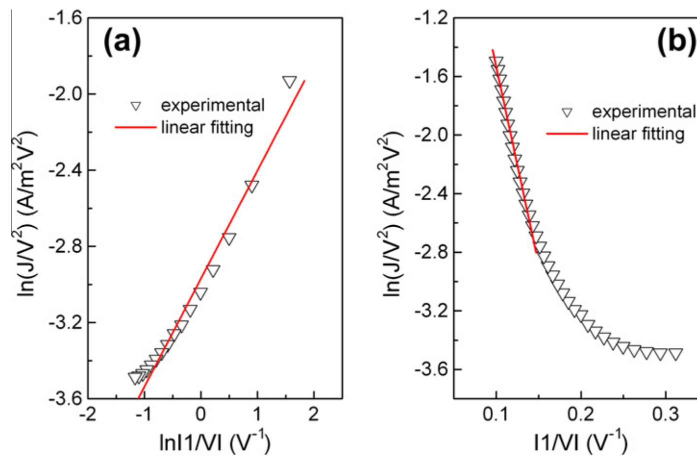

Fig. 8. (a) Experimental and linear fitting curves of the OFF state current of Device A: ITO/CuPc/F_{16}CuPc/Al at low voltage in a $\ln(J/V^2)$ versus $\ln|1/V|$ plot. (b) Experimental and linear fitting curves of the OFF state current of Device A at high voltage in a $\ln(J/V^2)$ versus $|1/V|$ plot.

lated in the bulk of the CuPc and F_{16}CuPc, respectively. In view of that, the deviation of the current from the tunneling models could be reasonable understood as only charge carrier injection at the electrode/organic interfaces is concerned in the tunneling models.

According to the results found above, the mechanism of the p–n junction WORM device can be understood as follows. Under forward bias, holes and electrons are injected from ITO and Al electrodes, respectively, and then recombine at the CuPc/F_{16}CuPc interface. It has been demonstrated that an ohmic contact can be formed in the ITO/CuPc interface for hole injection [47], while there is a 0.4 eV barrier in F_{16}CuPc/Al for electrons injection. Due to the lower charge carrier injection barriers, the as fabricated device remains in the ON state for the first voltage sweep from 0 to 10 V, as shown in Fig. 2. The current at low voltage is predominantly determined by the F_{16}CuPc/Al interface and it should follow a Schottky emission model. With the increasing of the voltage, the electron injection barrier is reduced, and the numbers of the injected charge carriers are increased. When the injected charge carrier densities exceed what the material has in thermal equilibrium state without injection, charge carriers will accumulate in the bulk of the organic materials. Consequently, the current model transits from the injection limited one to the transport limited one. Thus the current follows the trap-limited SCLC model. Under negative bias, holes and electrons are injected from Al and ITO electrodes with a barrier of 1.1 and 1.3 eV, respectively. In view of that, the charge carriers injection efficiency should be lower and the device should remain in a low conductivity state, which is contrary to the phenomena found for the second voltage sweep from 0 to −10 V. It has been demonstrated that band bending and an interfacial dipole layer are observed at the interface of CuPc/F_{16}CuPc, which result in the accumulation of holes and electrons in CuPc and F_{16}CuPc, respectively, which forms a space charge field with the direction orientated from CuPc to F_{16}CuPc [38,40,41]. The space charge field dramatically reduces the electron and hole injection barriers from ITO and Al electrodes, respectively. As a result, the device shows an ON state for the second voltage sweep from 0 to −7.6 V, and the current follows a trap-limited SCLC model. On the other hand, the space charge field will form an additional energy barrier for holes (electrons) injecting from CuPc (F_{16}CuPc) to F_{16}CuPc (CuPc) and hence reduce the current when the device is positive biased. Thus the ON states current of Device A at negative voltage is higher than that at positive voltage at a given voltage, as shown in Fig. 2. However, with increasing voltage, the cation and anion constituents of the interfacial dipole could be neutralized by the injected electrons and holes, respectively [48]. Consequently, the interfacial dipole layer is destructed, which is proved by XRD data shown in Fig. 5. The device is then turned to OFF state due to the increased charge carriers injection barriers. Meanwhile, the destruction of the interfacial dipole is irreversible, thus the device should remain in the OFF state for the latter voltage sweeps. Due to the high charge carrier injection barrier at the respective electrode, the OFF state current at reverse bias should predominantly follow the tunneling model. For the OFF state at positive voltage, as the transition of the device from the ON state to the OFF state does not alter the ITO/CuPc and F_{16}CuPc/Al interfacial prosperities, the OFF state current is injected limited and follows the Schottky emission model at low voltage. The current model transits to the trap-limited SCLC one, and a linear relation between $\log J$ and $\log V$ with a slope of 3.5 is found at high voltage. The large slope that exceeds 2 indicates that there are deep traps presenting in the organic layers [49,50]. It should be noted that the critical voltage for the current model transition from Schottky emission model to the trap-limited SCLC model for the ON state is higher than the OFF state at positive voltage region. These findings suggest that the destruction of the interfacial dipole layer at the CuPC/F_{16}CuPc interface may form an insulating layer by disrupting the molecular stacking, which would introduce deep traps for charge carriers transport. Such an insulating layer restricts holes to recombine with electrons at the interface and hence holes and electrons are more favorable to accumulate in the bulk of

CuPc and F_{16}CuPc, respectively. As a result, a space charge field is formed, which will act as an extra barrier for hole and electron injection from the anode and cathode, respectively. Despite the ON and OFF state current at positive voltage follow the same Schottky emission model, the significantly reduced OFF state current should be attributed to the change of the barrier height according to Eq. (1). Although the interfacial dipole layer formation and destruction have been demonstrated by small angle XRD, substantial future experimental work is required to understand these phenomena and their mechanisms.

4. Conclusion

A simple nonvolatile WORM memory device is demonstrated based on CuPc/F_{16}CuPc p–n junction. The device presents an ON/OFF current ratio of 2.6×10^4. The ON state of the device at forward and reverse bias are attributed to the low charge carrier injection barriers and the reduced charge carrier injection barriers due to the interfacial dipole layer formatted in the CuPc/F_{16}CuPc interface, respectively. The transition from the ON state to the OFF state by applying a reverse bias results from the destruction of the interfacial dipole layer, which forms an insulating layer and restricts charge carrier recombination. Compared with the ITO/F_{16}CuPc/Al single layer WORM memory device [35], the ON/OFF current ratio of the ITO/CuPc/F_{16}CuPc/Al p–n junction memory device increases by one order of magnitude. Besides, it is easier to tailor the interfacial properties and hence the device performance by selecting the p- and n-types materials in the p–n junction WORM memory devices. The present results indicate that the conductivity of the devices can be well controlled by interfacial dipole layer formatted in the p–n junction, and such a novel interfacial dipole layer formation and destruction mechanism holds the promise for potential applications in next-generation nonvolatile WORM memory devices.

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