Applied Physics Express 4 (2011) 052104
DOI: 10.1143/APEX.4.052104

High-Power-Density High-Efficiency Bottom-Emitting Vertical-Cavity Surface-Emitting Laser Array

Di Liu[1,2], Yongqiang Ning[1*], Yugang Zeng[1], Li Qin[1], Yun Liu[1], Xing Zhang[1,2], Lisen Zhang[1,2], Jinsheng Zhang[1,2], Cunzhu Tong[1], and Lijun Wang[1]

[1]*Key Laboratory of Excited State Processes, Changchun Institute of Optics, Fine Mechanics and Physics, The Chinese Academy of Sciences, Changchun, Jilin 130033, P. R. China*
[2]*Graduate School of the Chinese Academy of Science, Beijing 100039, P. R. China*

Received March 14, 2011; accepted April 12, 2011; published online May 6, 2011

We report on the lasing characteristics of a two-dimensional (2D) vertical-cavity surface-emitting laser (VCSEL) array with three $In_{0.2}GaAs/GaAs_{0.92}P$ QWs emitting at 977 nm. The contribution of a large-bandgap barrier material, GaAsP, to improve the output power was investigated. More than 123 W of pulsed peak power at 110 A was achieved, corresponding to 24.6 kW/cm^2 of power density and 1.11 W/A of slope efficiency. The thermal effect dependence of the characteristics of the array was illustrated. Moreover, the device performance was estimated by a functional method using a p-parameter.

High-power vertical-cavity surface-emitting lasers have been of great interest recently for applications in high-speed data transmission, high-resolution printing, and pumping of solid-state and fiber lasers,[1)] for the reasons that they exhibit low threshold current, low divergence angles of the output beam and low cost, compared with edge-emitting semiconductor lasers. In order to increase the overall output power, one way is to enlarge the active area of a single device. However, the limitation of this method is that the power conversion efficiency will be decreased with increasing active area. Alternatively, another way is to integrate elements into two-dimensional (2D) arrays on a single chip. High array density and appropriate heat spreading make it easier to obtain a high output power. Up to now, effort has been given to studies of increasing the output power of VCSEL. For single devices, a maximum output power of 1.95 W for continuous-wave (CW) operation was reported.[2)] A single VCSEL with five InGaAs quantum wells (QWs) emitting over 12.5 W at an injection current of 20 A under short pulsed operation was reported.[3)] For arrays, a device consisting of 19-element emitted more than 1 W of CW power and 10 W of pulsed power with 15 ns pulse width at room temperature.[4)] A 16-element array was operated at around 1.21 W of CW output power at 6 A at room temperature.[2)] In another work,[5)] a 231 W CW output power was achieved at a 320 A drive current at 15 °C heat sink temperature from a $\sim 5 \times 5\,mm^2$ array chip.

In this paper, we report on a high-power-density and high-efficiency VCSEL array with three $In_{0.2}GaAs/GaAs_{0.92}P$ strained QWs operating at 977 nm. The influence of different barrier materials (GaAs and GaAsP) on the output power of a VCSEL device is investigated; then we obtain a higher CW output power and a higher pulsed peak power from a 4×4 VCSEL array with 200 μm active diameter and 250 μm spacing. Furthermore, we study the characteristics such as the threshold current and the slope efficiency depending on thermal effects under CW operation. Finally, the performance of the 4×4 VCSEL array is estimated by a method using a p-parameter, which is very quick while maintaining accuracy.

The schematically drawn layer structure of a processed 4×4 VCSEL array with heat sink is shown in Fig. 1. The DBR mirrors are composed of $Al_{0.9}Ga_{0.1}As/Al_{0.12}Ga_{0.88}As$ quarter-wavelength layers with a graded interface to reduce series resistance; there are 28 periods in the bottom mirror and 30 periods in the top mirror. Current and optical confinements are typically achieved through selective oxidation of an aluminum-rich layer, a 30-nm-thick $Al_{0.98}Ga_{0.02}As$ layer. Additional details of the device and the processing can be found in another article.[6)] In particular, instead of the traditional barrier material (GaAs), $GaAs_{0.92}P$ (10 nm) is used as the barriers of three $In_{0.2}GaAs$ (8 nm) strained quantum wells in the active region.

In order to understand the influence of different barrier materials on the output performance, we compare the band structures of $In_{0.2}GaAs/GaAs_{0.92}P$ and $In_{0.2}GaAs/GaAs$ QWs. The band structure of $In_{0.2}GaAs/GaAs_{0.92}P$ QWs at room temperature is shown in Fig. 2. Based on the formula given by Minch *et al.*,[7)] the value of 1.51 eV of the bandgap in the $GaAs_{0.92}P$ barrier is obtained (the bandgap in the GaAs barrier amounts to 1.42 eV at room temperature). Moreover, we calculate the values of the band offsets (ΔE_c and ΔE_v) of $In_{0.2}GaAs/GaAs_{0.92}P$ and $In_{0.2}GaAs/GaAs$ strained quantum wells, which correspond to the confinement of electrons and holes in an energy potential well. The calculation is on the basis of modal-solid theory[8)] and the material parameters we used are determined in refs. 7, 9, and 10. For $In_{0.2}GaAs/GaAs$ QW, the band offsets are $\Delta E_c = 254$ meV and $\Delta E_v = 44$ meV for the conduction and heavy hole valence bands, respectively. For $In_{0.2}GaAs/GaAs_{0.92}P$ QW, however, the conduction band offset is increased to $\Delta E_c = 313$ meV, which is 23% larger than that in the GaAs barrier QW. Moreover, compared with the GaAs barrier QW, the $GaAs_{0.92}P$ barrier doubles the value of the heavy hole valence band offset to $\Delta E_v = 92$ meV. The remarkable increase in both the conduction and valence band offset not only confine electrons well, but have the ability to prevent hole leakage during laser operation. Thus, compared with GaAs, large-bandgap GaAsP barriers can provide better confinement of carriers in the quantum wells, which is good for improving the output power. In Fig. 3, the simulated output characteristics for the 200-μm-active-diameter single device without thermal effects are shown, where the solid line and dashed line correspond to $In_{0.2}GaAs/GaAs_{0.92}P$ QW and $In_{0.2}GaAs/GaAs$ QW, respectively. It can be seen that using GaAsP barriers causes an increase in the maximum output power of more than 11% at room temperature.

*E-mail address: ningyq@ciomp.ac.cn

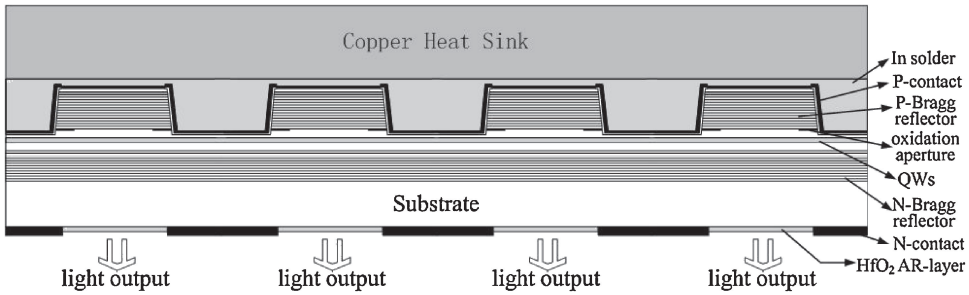

Fig. 1. Schematic cross section of a 4×4 VCSEL array.

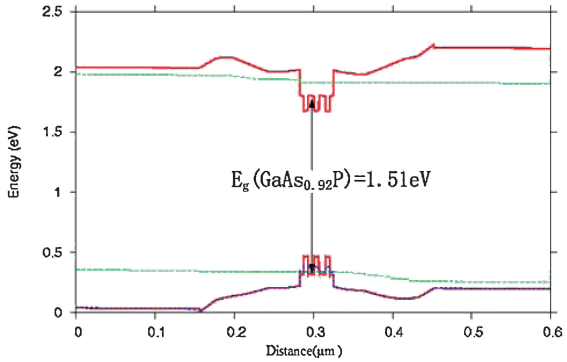

Fig. 2. Energy band diagram of the $In_{0.2}GaAs/GaAs_{0.92}P$ QWs near the active region (green lines: quasi Fermi levels).

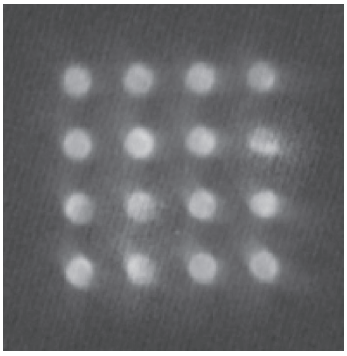

Fig. 4. Subthreshold pattern of the near field of the 4×4 VCSEL array under pulsed operation at room temperature.

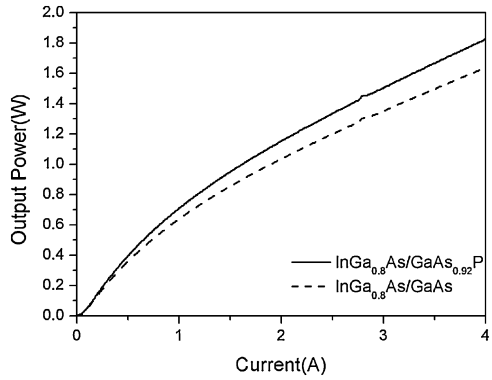

Fig. 3. Output power for $In_{0.2}GaAs/GaAs_{0.92}P$ (solid line) and $In_{0.2}GaAs/GaAs$ (dashed line) QW structures at room temperature.

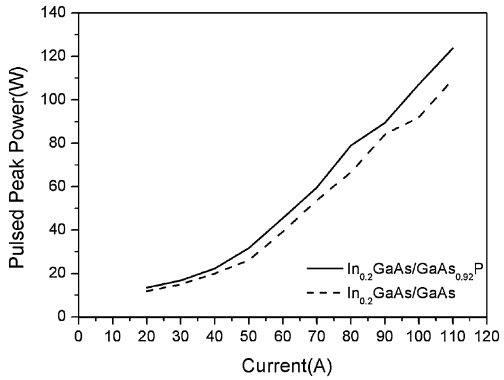

Fig. 5. Peak output power for $In_{0.2}GaAs/GaAs_{0.92}P$ (solid line) and $In_{0.2}GaAs/GaAs$ (dashed line) QW structures under pulsed operation at room temperature, with 60 ns pulses and 0.06‰ duty cycle.

All measurements in this work are made on a 2D 16-element VCSEL array with 200 μm active diameter and 250 μm spacing, corresponding to an emitting area of ~0.005 cm^2. Figure 4 shows the near field emission pattern of the 4×4 VCSEL array at 0.7 A (subthreshold) under pulsed operation at room temperature. We have measured the pulsed peak power for $In_{0.2}GaAs/GaAs_{0.92}P$ and $In_{0.2}GaAs/GaAs$ QW structures under short pulsed (20–100 ns) operation at room temperature for comparison. In the pulsed measurement, the device is operated by short pulses with a pulse width of 60 ns and a duty cycle of 0.06‰. The results are shown in Fig. 5. It can be seen that the device with $In_{0.2}GaAs/GaAs_{0.92}P$ QWs (solid line) delivers over 123 W at a current of 110 A, which is over 13% larger than 109 W for the GaAs barrier QW (dashed line). In addition, the power density and slope efficiency reach 24.6 kW/cm^2 and 1.11 W/A, respectively. The array device has not been measured to a very high pulsed current because of the voltage limitations of the power supply we used. So far, however, the power density and slope efficiency we obtained from a 4×4 VCSEL array are to our knowledge the highest results reported for a 2D VCSEL array.

Then, we investigated the lasing characteristics of the high-power-density 4×4 VCSEL array. The wavelength spectrum and output power–current–voltage (L–I–V) characteristic curves under CW and pulsed operation at room temperature are shown in Fig. 6. The output power of 1.51 W is achieved at 4 A CW current at room temperature, which is almost twice as much as the previous result for an $In_{0.2}GaAs/GaAs$ VCSEL array with the same active diameter (200 μm) at the same pumping level.[2] The array emits at 977.13 nm and the FWHM of the spectrum is 1.0 nm, as shown in the inset of Fig. 6. The

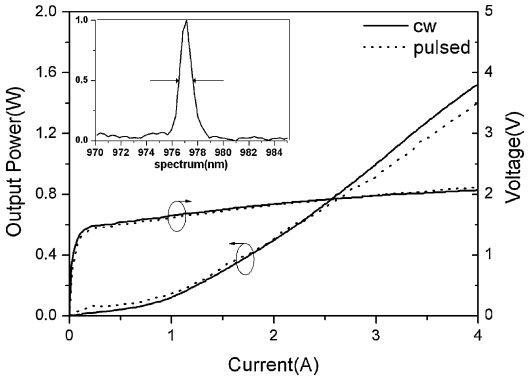

Fig. 6. L–I–V and spectrum characteristics of the 4×4 VCSEL array.

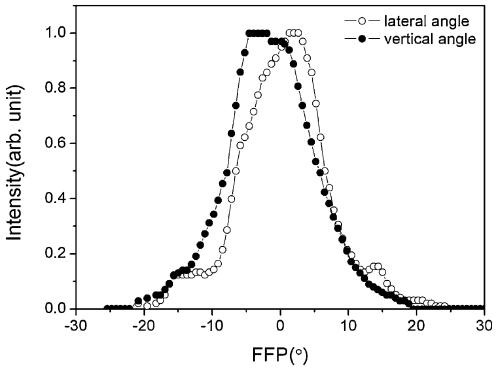

Fig. 7. Far-field pattern of the 4×4 VCSEL array.

threshold current and differential resistance are 0.98 A, 0.1 Ω under CW operation and 0.82 A, 0.14 Ω under pulsed operation, respectively.

From Fig. 6 we can see that the array has a higher threshold current under CW operation, which is different from the situation of small-aperture devices,[11] and has a slightly higher slope efficiency above the threshold under CW operation as well. This can be interpreted as follows. It is believed that the main reason for the higher threshold current is the gain offset caused by temperature rise under CW operation in device. As we know, both of the gain spectrum and the cavity mode shift to longer wavelengths when temperature increases. For VCSEL devices, however, shift velocity of the gain spectrum is much faster than that of the cavity mode. And there is usually only one longitudinal mode in VCSEL. Thus, serious mismatch of the center wavelength between the gain spectrum and the cavity mode brings about a higher threshold current under CW operation. In addition, for the broad-area VCSEL device with strong optical confinement based on its oxidation aperture structure, thermally induced gain suppression leads to the onset of higher-order transverse modes when below the threshold,[12] which also results in a higher threshold current under CW operation. Different from the situation under pulsed operation, there is thermal index guiding (thermal lensing) coming from self-heating under CW operation. With increasing CW currents, thermal lensing gradually becomes stronger. Consequently, it arouses the confinement effect on multitransverse modes, making scattering losses at the edges decrease, which generates a higher slope efficiency under CW operation above the threshold before reaching thermal rollover.

Different from previous research, we apply a useful parameter, p-parameter, to quickly evaluate the device performance. The advantage of this method is that the p-parameter can be obtained directly from the L–I–V characteristic defined as $p = V_0/(I_{th}R_d) = V_0/(J_{th}\rho_d)$ without the need for any further optical measurements.[5] In the above expression, V_0 is the turn-on voltage; I_{th}, J_{th}, R_d, and ρ_d are the threshold current, threshold current density, differential resistance, and resistivity of the VCSEL array considered, respectively. In practice, when $p < 10$, this corresponds to poor performance and when $p > 50$, this corresponds to exceptional performance for a VCSEL device. However, $p > 50$ is rarely achieved for VCSEL. In the case of the 4×4 VCSEL array tested, we obtained values of 15 under CW operation and 13 under pulsed operation (for 980 nm devices, with $V_0 \sim 1.5$ V), indicating that the device has relatively good performance.

Besides, the far-field FWHM divergence angles $\theta_{\parallel}$ (lateral divergence angle) and $\theta_{\perp}$ (vertical divergence angle) at a current of 4 A under CW operation at room temperature are 12.9° and 12.6°, respectively, as demonstrated in Fig. 7, further showing better output beam characteristics.

In summary, we have found that for VCSEL devices, the large-bandgap barrier material, GaAsP, contributes to improving the output power. The highest peak output power of more than 123 W at a current of 110 A is achieved by the 4×4 VCSEL array with an emitting area of ~0.005 cm^2 under short pulsed injection with 60 ns pulse width, corresponding to 24.6 kW/cm^2 of power density and 1.11 W/A of slope efficiency. Moreover, we have found that the threshold current and slope efficiency under pulsed operation are lower than those under CW operation before reaching thermal rollover due to thermally induced gain offset, gain suppression, and thermal lensing for broad-area 2D VCSEL arrays. The relatively high value of the p-parameter and low symmetric angles demonstrate that the 4×4 VCSEL array with three $In_{0.2}GaAs/GaAs_{0.92}P$ QWs has good device performance. Consequently, all these together make it a better candidate for applications such as data transmission and as a pumping source.

Acknowledgments This work is supported by the National Natural Science Foundation of China under Grant No. 60636020, 60706007, 10974012.

1) M. C. Amann, M. Ortsiefer, R. Shau, and J. Rosskopf: Proc. SPIE **4871** (2002) 123.
2) T. Li, Y. Q. Ning, Y. F. Sun, C. Wang, J. Liu, Y. Liu, and L. J. Wang: J. Lumin. **122–123** (2007) 571.
3) N. Otake, K. Abe, H. Yamada, H. Wado, and Y. Takeuchi: Appl. Phys. Express **2** (2009) 052102.
4) M. Miller, M. Grabherr, R. Jäger, and K. J. Ebeling: IEEE Photonics Technol. Lett. **13** (2001) 173.
5) J. F. Seurin, C. L. Ghosh, V. Khalfin, A. Miglo, G. Y. Xu, J. D. Wynn, P. Pradhan, and L. A. D'Asaro: Proc. SPIE **6908** (2008) 690808.
6) J. Cui, Y. Ning, Y. Zhang, P. Kong, G. Liu, X. Zhang, Z. Wang, T. Li, Y. Sun, and L. Wang: Appl. Opt. **48** (2009) 3317.
7) J. Minch, S. H. Park, T. Keating, and S. L. Chuang: IEEE J. Quantum Electron. **35** (1999) 771.
8) C. G. Van de Walle: Phys. Rev. B **39** (1989) 1871.
9) P. Zhang, Y. Song, J. Tian, X. Zhang, and Z. Zhang: J. Appl. Phys. **105** (2009) 053103.
10) I. Vurgaftman, J. R. Meyer, and L. R. Ram-Mohan: J. Appl. Phys. **89** (2001) 5815.
11) M. Brunner, K. Gulden, R. Hövel, and M. Moser: Appl. Phys. Lett. **76** (2000) 7.
12) C. Degen, I. Fischer, and W. Elsäßer: Appl. Phys. Lett. **76** (2000) 3352.