# 1.3-$\mu$m In(Ga)As Quantum-Dot VCSELs Fabricated by Dielectric-Free Approach With Surface-Relief Process

D. W. Xu, S. F. Yoon, Y. Ding, C. Z. Tong, W. J. Fan, and L. J. Zhao

***Abstract*—We present the 1.3-$\mu$m In(Ga)As quantum-dot (QD) vertical-cavity surface-emitting lasers (VCSELs) fabricated by the dielectric-free (DF) approach with the surface-relief (SR) process. Compared with the conventional dielectric-dependent (DD) method, the lower differential resistance and improved output power have been achieved by the DF approach. With the same oxide aperture area, the differential resistance is reduced by 36.47% and output power is improved by 78.32% under continuous-wave operation; it is up to 3.42 mW under pulsed operation with oxide aperture diameter $\sim$15 $\mu$m. The surface-relief technique is also applied, for the first time, in 1.3-$\mu$m QD VCSELs, and it effectively enhances the emission of the fundamental mode. The characteristic of small signal modulation response is also analyzed.**

***Index Terms*—Dielectric-free approach, quantum dot (QD), surface-relief technique, vertical-cavity surface-emitting lasers (VCSELs).**

## I. Introduction

VERTICAL-CAVITY surface-emitting lasers (VCSELs) with In(Ga)As quantum-dot (QD) active region have been regarded as a potentially good candidate for 1.3-$\mu$m optical fiber communication [1]–[4]. In addition, selective oxidation is also used to form optical & electrical confinement aperture [2], whose area is always small to avoid multiple high-order transverse oscillation. However, small-aperture device has rather large differential resistance and current density, which lead to serious self-heating and result in output power deterioration [4]. Therefore, alternative methods are expected to improve self-heating effect or enhance the fundamental-mode emission with larger oxide aperture.

One possible solution is the dielectric-free (DF) approach, which was reported by us in 850-nm quantum-well (QW) VCSELs [5]. In this approach, self-insulation is formed by selective oxidation instead of dielectric-material deposition as conventional VCSELs [2], [3]. This method not only helps to reduce fabrication cost & complexity, but also lower the differential resistance by enlarging the area of contact and current spreading. Less Joule heating is generated, thus resulting in higher output power. Another method is to etch a shallow ring-shape surface-relief (SR) in the top mirror, which reduces the mirror reflectivity and hence increases mirror loss of high-order modes [6]. In this case, the emission of fundamental mode can be enhanced with a larger current aperture, and thus lower self-heating. However, to the best of our knowledge, there is still no report on both dielectric-free approach and surface-relief technique in 1.3-$\mu$m QD VCSELs.

In this letter, we present 1.3-$\mu$m QD VCSELs fabricated by dielectric-free (DF) approach with surface-relief (SR) technique. It should be the first time to report both these two techniques in processing of QD materials. With DF approach, the property of light-current-voltage ($L$-$I$-$V$) and small signal modulation response is investigated and compared with the conventional dielectric-dependent (DD) method. The influence of SR technique on output power and spectrum is also discussed.

## II. Experiment

The QD-VCSEL structure shown in Fig. 1(a) is grown on $n^+$-GaAs (100) substrate by molecular-beam epitaxy (MBE). The device consists of 24 pairs of $p$-doped and 33.5 pairs of $n$-doped $Al_{0.9}Ga_{0.1}As$/GaAs distributed Bragg reflectors (DBR). 17 layers of $p$-doped InAs/GaAs QDs are contained in the $3\lambda$ intercavity region. Each standing wave position coincides with three layers of QDs, and two adjacent QD layers are separated by 32 nm of GaAs. The QDs are grown directly on GaAs and capped by a 6-nm-thick $In_{0.15}Ga_{0.85}$ As layer. The 5-nm-thick $p$-doped GaAs layers are sandwiched between two undoped GaAs layers with thickness of 5 and 12 nm, respectively.

Device processing involves wet etching the mesas followed by wet $N_2$ oxidation of a 12-nm-thick AlAs layer to form current aperture. As shown in Fig. 1(b), one mesa includes laser's main body and bond pad linked by a bridge. The diameter of bond pad ($d_{\mathrm{BP}}$) is 90 $\mu$m and the one of main body ($d_{\mathrm{MB}}$) varies from 105 to 115 $\mu$m, which is much larger than the one with dielectric-dependent (DD) approach ($d_{\mathrm{MB}} \sim 48$ $\mu$m) reported by us previously [3]. If the top DBR stacks are removed after AlAs oxidation, with DD approach (Fig. 1(c)), besides the oxide aperture, there will be another aperture left on bond pad since its area is larger than the main body; therefore dielectric material

Manuscript received July 22, 2010; revised September 28, 2010; accepted October 30, 2010. Date of publication November 09, 2010; date of current version December 30, 2010. This work was supported by the A*STAR Singapore-Poland Bilateral Program under SERC Grant 0621200015.

D. W. Xu, S. F. Yoon, Y. Ding, C. Z. Tong, and W. J. Fan are with the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798, Republic of Singapore (e-mail: n060085@ntu.edu.sg; esfyoon@ntu.edu.sg; YDing@ntu.edu.sg; CZTong@ntu.edu.sg; ewjfan@ntu.edu.sg).

L. J. Zhao is with the Key Laboratory of Semiconductor Materials Science, Institute of Semiconductors, Chinese Academy of Sciences, Beijing 100083, China (e-mail: ljzhao@red.semi.ac.cn).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LPT.2010.2091269

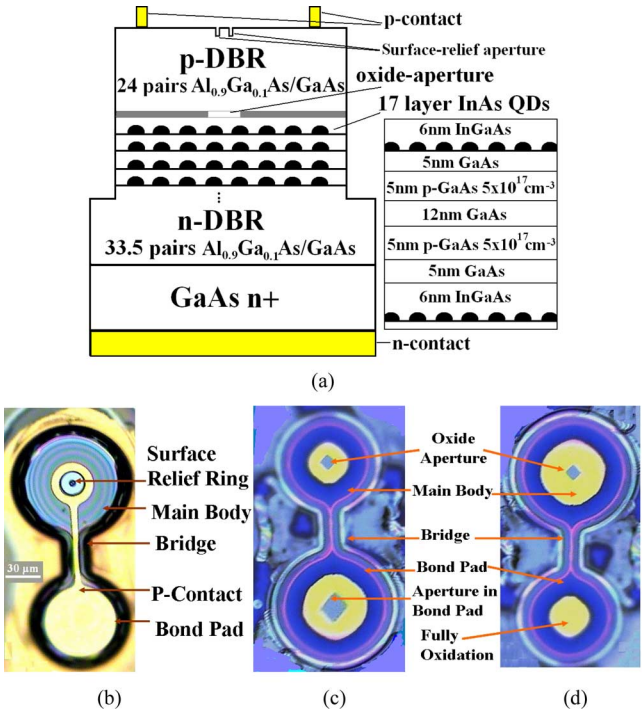


Fig. 1. (a) Schematic cross-section diagram and (b) bird-view of 1.3-$\mu$m QD-VCSELs by dielectric-free (DF) approach with surface-relief (SR) technique; top view of a sample after AlAs oxidation and removing top DBR stacks: (c) dielectric-dependent (DD) and (d) DF approaches.

must be deposited to avoid current leakage. This procedure is not required with DF approach: the area of oxide aperture can be precisely controlled and smaller than the difference between the main body and bond pad; thus self-insulation is fully built after oxidation without additional dielectric material (Fig. 1(d)).

A 3.5-$\mu$m-diameter surface-relief (SR) ring is then formed on the centre of top layer by standard photolithography and wet etching ($H_3PO_4$:$H_2O_2$: DI-Water $=$ 1 : 1 : 10). The etching depth is $\sim$90 nm $(\lambda/4)$ to reach the local maximum of mirror loss for high-order mode [6]. *Ti-Au* and *Au-Ge-Ni* are deposited as the $p$- and $n$-contact, respectively. The fabricated device chips were cleaved and mounted on heat sink for characterization: the performance of light-current-voltage ($L$-$I$-$V$) and spectra were tested by a Keithley $L$-$I$-$V$ test system and an optical spectrum analyzer (Yokogawa, AQ6317C), respectively; while the small signal modulation response was measured by a calibrated vector network analyzer (Agilent 8720D, 50 MHz–20 GHz), combined with a 50-$\mu$m optical fibre coupling and connected to a high-speed O/E converter (HP 11982A, dc-15 GHz).

## III. Results and Discussion

The comparison between dielectric-free (DF) and conventional dielectric-dependent (DD) approaches on the $L$-$I$-$V$ characteristics are illustrated in Fig. 2. The measured devices are based on the same epitaxial wafer, and the measurement is at room temperature (RT) and under continuous-wave (CW) current injection. It can be seen that for same oxide aperture diameter ($d_{OA} \sim 10$ $\mu$m) and without surface relief (SR), by DF approach, the threshold current $(I_{\rm th})$ is 2.15 mA, and the

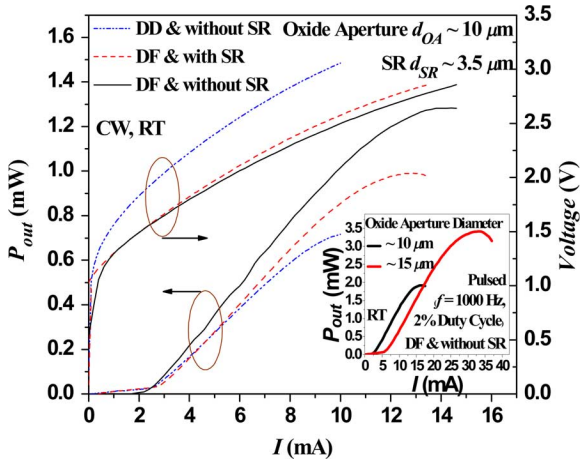


Fig. 2. Comparison of the light-current-voltage $(L-I-V)$ characteristics between dielectric-free (DF) and dielectric-dependent (DD) approaches, as well as the influence of surface-relief (SR) technique; inset shows the $L-I$ properties by DF approach under pulsed operation.

output power $(P_{\rm out})$ is saturated at 14 mA with 1.28 mW, which is 78.32% better than the one by DD approach (0.717 mW at 10 mA). The significant improvement should be attributed to the enlargement in area on contact and current spreading in $p$-DBR layers, which decrease differential resistance and thereby lower Joule heating. In view of the $I$-$V$ curves: for devices by DF approach without SR, the differential resistance is 79.4 $\Omega$ and 36.47% lower than the one by DD approach (125 $\Omega$). High $P_{\rm out}$ is also obtained by DF approach under pulsed injection (inset of Fig. 2). At frequency $(f)$ of 1000 Hz and 2% duty cycle, $P_{\rm out}$ at RT are saturated with 1.92 and 3.42 mW for devices with $d_{\rm OA} \sim 10$ $\mu$m and 15 $\mu$m, respectively.

The influence of surface relief (SR) on the $L$-$I$-$V$ characteristic is also demonstrated in Fig. 2. By dielectric-free (DF) approach, for device with SR (diameter $(d_{\rm SR}) \sim 3.5$ $\mu$m), $I_{\rm th}$ is slightly increased (2.47 mA), and $P_{\rm out}$ is a little lower (0.995 mW) compared with the one without SR. The reason is that by SR technique mirror loss is increased in high-order transverse mode, whose emission is suppressed and thereby more current injection is required for lasing. Furthermore, from the $I$-$V$ curves, it can be seen that the differential resistance of device fabricated by DF approach with SR (87.72 $\Omega$) is a little larger than the one without SR. It should be due to the introduced discontinuity in current channel by the etched SR ring on top surface. Although the $L$-$I$-$V$ characteristics are influenced by SR technique, the lasing of fundamental mode can be strongly favored. Fig. 3 and its inset present the spectra of devices by DF approach with and without SR, respectively. For device with SR, the central wavelength is 1266.64 nm with a full-wave at half-maximum (FWHM) of 0.123 nm. The side-mode suppression-ratio (SMSR) is 7 dB at 5 mA, which indicates the significant enhancement of fundamental mode compared with the one without SR. Improvement on spectra performance for more investigations, such as precise analysis of thermal resistance and carrier dynamics, might be achieved by further optimization in device processing. One suggestion is to use electron-beam lithography and reactive ion-beam etching [7], which can provide much better critical precision on pattern alignment and control of etching depth, respectively. Another recommendation in

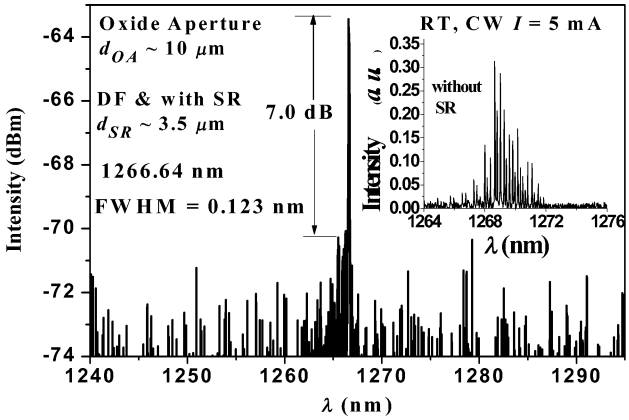


Fig. 3. Lasing spectrum of 1.3-$\mu$m QD VCSELs fabricated by dielectric-free (DF) approach with surface relief (SR); inset shows the one without SR.

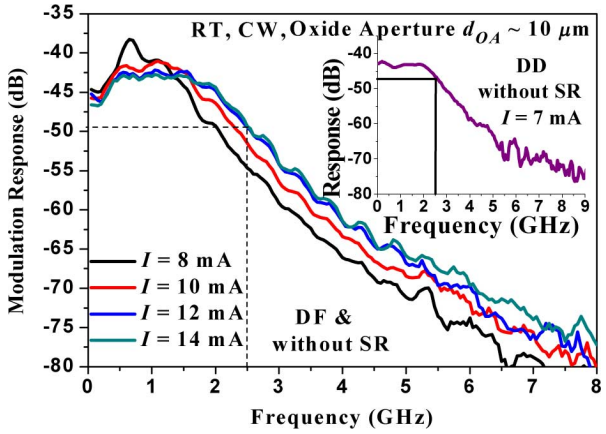


Fig. 4. Small signal modulation response of fabricated QD VCSELs fabricated by dielectric-free (DF) approach. Maximum 3-dB bandwidth of 2.5 GHz is obtained at 14 mA. Inset shows the response in device fabricated by dielectric-dependent (DD) approach at 7 mA.

[7] is inverted surface-relief (ISR), in order to relax the required etch-depth precision in device processing.

The small signal modulation response of devices by dielectric-free (DF) approach (without SR) is shown in Fig. 4. For the device with oxide-aperture diameter of 10 $\mu$m, the 3-dB modulation bandwidth at room temperature (RT) increased from 8 mA and saturated around 12–14 mA at $\sim$2.51 GHz. By fitting analysis based on the three-pole transfer function [3], assuming there is no thermal limitation, the modulation bandwidth by the parasitics only can be calculated ($\sim$8.73 GHz). It is apparent that the 3-dB modulation bandwidth is mainly limited by thermal effect. The serious self-heating results in decrease in carrier lifetime and modulation gain, so that damping rate is suppressed. Besides Joule heating in DBR stacks, another important contribution of self-heating is from QD active region: nonradiative recombination & spontaneous emission. It is caused by the degradation of carrier confinement due to thin wetting layer at high injected current [4].

In Fig. 4, it can be also found that with same oxide-aperture area, the maximum 3-dB bandwidth with DF approach ($\sim$2.51 GHz) is comparable to what we have achieved with dielectric-dependent (DD) approach [3] (inset of Fig. 4), except that the required current in DD approach is only 7 mA. The increase in consumption power by DF approach should be due to the enlarged area of laser pad and current distribution, which increases parasitic capacitance so that affects the modulation bandwidth. By fitting analysis based on the three-pole transfer function [3], the cut-off parasitics frequency of the device with DF approach is $\sim$2.34 GHz. It is smaller than the one with DD approach ($\sim$3 GHz reported in [3]), and thereby the property of modulation should be also affected. Further improvement can be carried out by optimizing the mesa morphology or introducing proton implantation for the present devices [8], [9].

## IV. Conclusion

1.3-$\mu$m In(Ga)As QD VCSELs fabricated by dielectric-free (DF) approach with surface-relief (SR) process is demonstrated. Compared with the conventional dielectric-dependent (DD) approach, by DF approach and with the same oxide aperture diameter (10 $\mu$m), the differential resistance (79.4 $\Omega$) is reduced by 36.47% and the output power (1.28 mW) is improved by 78.32% under continuous-wave (CW) operation at room temperature (RT). The output power is up to 3.42 mW under pulsed operation when oxide aperture diameter is 15 $\mu$m. Surface relief (SR) technique is also first applied in 1.3-$\mu$m QD VCSELs and effectively enhances the emission of fundamental mode. The maximum 3-dB modulation bandwidth is $\sim$2.51 GHz by DF approach, which is comparable with the one in DD approach but more power consumption is required.

## References

[1] P. C. Peng, Y. H. Chang, H. C. Kuo, W. K. Tsai, G. Lin, C. T. Lin, H. C. Yu, H. P. Yang, R. S. Hsiao, K. F. Lin, J. Y. Chi, S. Chi, and S. C. Wang, "1.3 $\mu$m quantum dot vertical-cavity surface-emitting laser with external light injection," *Electron. Lett.*, vol. 41, no. 32, pp. 1222–1223, 2005.

[2] D. W. Xu, S. F. Yoon, C. Z. Tong, L. J. Zhao, Y. Ding, and W. J. Fan, "High-temperature continuous-wave single-mode operation of 1.3-$\mu$m $p$ -doped InAs–GaAs quantum-dot VCSELs," *IEEE Photonics Technol. Lett.*, vol. 21, no. 17, pp. 1211–1213, Sep. 1, 2009.

[3] Y. Ding, W. J. Fan, D. W. Xu, C. Z. Tong, S. F. Yoon, D. H. Zhang, L. J. Zhao, W. Wang, Y. Liu, and N. H. Zhu, "Fabrication and modulation characteristics of 1.3-$\mu$m InAs quantum dot vertical cavity surface emitting lasers," *J. Phys. D*, vol. 42, no. 8, p. 085117, 2009.

[4] D. W. Xu, S. F. Yoon, and C. Z. Tong, "Self-consistent analysis of carrier confinement and output power in 1.3 $\mu$m InAs–GaAs quantum-dot VCSELs," *IEEE J. Quantum Electron.*, vol. 44, no. 9, pp. 879–885, Sep. 2008.

[5] Y. Ding, W. J. Fan, D. W. Xu, C. Z. Tong, Y. Liu, and L. J. Zhao, "Low threshold current density, low resistance oxide-confined VCSEL fabricated by a dielectric-free approach," *Appl. Phys. B*, vol. 98, no. 4, pp. 773–778, 2010.

[6] D. Supper, J. Pfeiffer, M. Ilzhofer, C. Giuliani, C. Degen, A. P. Lima, A. Ramakrishnan, G. Ebbinghaus, and G. Steinle, "Long-wavelength VCSEL with integrated relief for control of singlemode emission," *Opt. Commun. (Netherlands)*, vol. 267, no. 2, pp. 447–450, 2006.

[7] F. M. Lee, C. L. Tsai, C. W. Hu, K. F. Huang, M. C. Wu, and S. C. Ko, "1.3-$\mu$m GaInAsN vertical-cavity surface-emitting lasers by oxide-planarized and surface-relief processes for single-mode operation," *IEEE Electron. Device Lett.*, vol. 28, no. 2, pp. 120–122, Feb. 2007.

[8] Y. H. Chang, F. I. Lai, C. Y. Lu, H. C. Yu, C. P. Sung, H. P. Yang, and S. C. Wang, "High-speed ($>$ 10 Gbps) 850 nm oxide-confined vertical cavity surface emitting lasers (VCSELs) with a planar process and reduced parasitic capacitance," *Semicond. Sci. Technol.*, vol. 19, pp. L74–L77, 2004.

[9] H. C. Yu, S. J. Chang, Y. K. Su, C. P. Sung, H. P. Yang, C. Y. Huang, Y. W. Lin, J. M. Wang, F. I. Lai, and H. C. Kuo, "Improvement of high-speed oxide-confined vertical-cavity surface-emitting lasers," *Jpn. J. Appl. Phys. 1, Pap. Short Notes Rev. Pap. (Japan)*, vol. 43, no. 4B, pp. 1947–1950, 2004.