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Improvements of Bilayer Ambipolar Organic Field-Effect Transistors Based on Pentacene and *N,N′*-Ditridecylperylene-3,4,9,10-tetracarboxylic Di-imide by Changing Growth Rate Method

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The changing growth rate method is adopted for the first time to improve the performance of ambipolar organic field-effect transistors (OFETs). Pentacene and *N,N′*-ditridecylperylene-3,4,9,10-tetracarboxylic di-imide (PTCDI-C13) are chosen as p-type and n-type organic semiconductors, respectively. By modifying the dielectric surface with polystyrene, balanced carrier mobilities as high as 0.41 and 0.40 $cm^2 \cdot V^{-1} \cdot s^{-1}$ for hole and electron, respectively, are achieved through such method, which are the highest values for air-stable ambipolar OFETs. Meanwhile, the devices show negligible hysteresis and air stability for more than one week. © 2012 The Japan Society of Applied Physics

Ambipolar organic field-effect transistors (OFETs) have attracted wide attention in recent years for potential applications in fields such as organic complementary metal oxide semiconductor (CMOS) integrated circuits (ICs), organic light-emitting field-effect transistors (OLEFETs), and organic lasers.[1,2] Thus far, with the rapid advancement of organic semiconductor materials, however, the carrier mobilities and air stability of ambipolar OFETs are far from meeting practical use. Although devices with single-layer architecture show carrier mobilities in the level of 1 $cm^2 \cdot V^{-1} \cdot s^{-1}$, they have poor air stability, especially for electron mobility.[3,4] Devices with bilayer architecture usually have better air stability but poor carrier mobilities due to the restriction of the carrier mobility of each layer material.[1,5,6] The current state-of-the-art carrier mobilities of these devices, to our knowledge, are around 0.1 $cm^2 \cdot V^{-1} \cdot s^{-1}$.[6]

For bilayer architecture devices, methods such as adjusting the thickness of each layer,[7] controlling the substrate or annealing temperature,[8] adopting various modifications[9] and using asymmetrical electrodes[10] have been adopted for optimization. However, these methods are based on a constant film growth rate. Since Wen *et al.*[11] have reported that a proper changing growth rate was able to promote electron mobility and air stability for unipolar OFETs based on *N,N′*-ditridecylperylene-3,4,9,10-tetracarboxylic di-imide (PTCDI-C13), an n-type organic semiconductor material with relatively high electron mobility but poor air stability, we wonder whether this method will benefit ambipolar devices with bilayer architecture.

In this study, we demonstrate high-performance bottom-gate top-contact ambipolar OFETs based on pentacene and PTCDI-C13 working under ambient condition [RH: 40 (±10) %] by changing the growth rate of the PTCDI-C13 film. By further modifying the SiO_2 substrates with PS, the devices show good air stability and remarkable high and balanced carrier mobilities of 0.41 and 0.40 $cm^2 \cdot V^{-1} \cdot s^{-1}$ for hole and electron, respectively, which are the highest for air-stable ambipolar devices to our knowledge.

Pentacene and PTCDI-C13 were purchased from Lumtech and Sigma-Aldrich, respectively. The substrate is heavily doped n-type silicon with 300 nm thermally oxidized SiO_2. The surface of the substrate is either modified with PS (Sigma-Aldrich, M_W 280,000) or not. We use anhydrous toluene as solvent for a solution of 10 mg/ml. After spin-coating at 2000 rpm for 30 s, the substrate is cured in vacuum at 120 °C for 1 h. The resulting thickness of PS is around 40 nm. Subsequently, 12 nm pentacene and 50 nm PTCDI-C13 are thermally evaporated onto the substrate at a base pressure of 1.5×10^{-4} Pa. The deposition rate of pentacene remains at 0.2 Å/s, while for PTCDI-C13, the deposition rate has three modes: Mode 1 is 0.2 Å/s; Mode 2 is 0.5 Å/s; Mode 3 is 0.05 Å/s for the first 5 nm and 0.2 Å/s for the subsequent 15 nm and 0.5 Å/s for the last 30 nm. When changing the growth rate, the samples are removed until the evaporation rate maintains stable. The substrate is kept at room temperature during the deposition. 50 nm Au is evaporated through a shadow mask with channel length and width of 200 and 4000 μm, respectively, which acts as the source and drain electrodes.

A quartz-crystal oscillator placed near the substrate is used to monitor the thickness and deposition rate of the field-effect transistors, which is calibrated *ex situ* using a surface profiler (Ambios XP-1). The electrical characteristics, including the voltage–current and capacitance measurements, are determined with Keithley 4200 SCS at room temperature under air ambient. The atomic force microscopy (AFM) tests are carried out with SPM-9700 (Shimadzu) under the phase mode. The carrier mobility is calculated using the following formula in the saturation regime: $I_{DS} = \mu C_i (W/2L)(V_{GS} - V_T)^2$, where μ is the field-effect mobility, C_i is the gate dielectric capacitance density, V_T is the threshold voltage, W and L are the channel width and length, respectively.

Figures 1(a)–1(b) compare the transfer characteristics of devices with the three growth modes. Due to the shifts of the threshold voltage, we choose those curves with approximately the same gate voltages when the minimum channel currents are reached to facilitate the comparison. Devices with mode 3 have greater electron on-current than those with modes 1 and 2, which indicates that less electrons are lost when transporting in the PTCDI-C13 layer grown by a different evaporation rate than those with a constant evaporation rate. For $V_{DS} = 40$ V, the calculated electron mobility in the saturation regime is 0.10 $cm^2 \cdot V^{-1} \cdot s^{-1}$ (C_i is ~11.5 $nF \cdot cm^{-2}$, which is tested using Keithley 4200 SCS at a frequency of 100 kHz and averaged from several squares with different sizes), which is about 100 and 70% higher than those with modes 1 and 2, respectively. The hole

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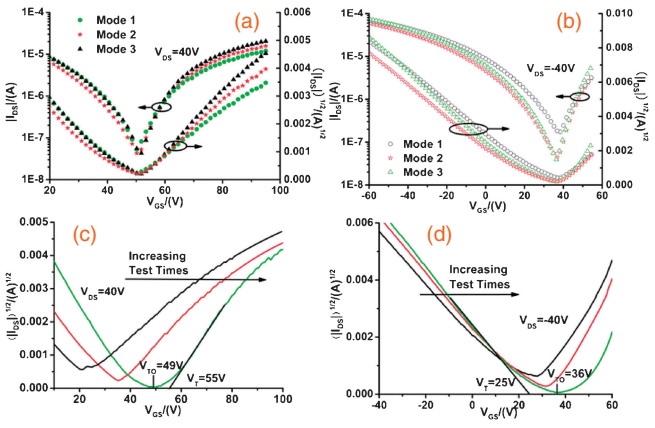

Fig. 1. Transfer characteristics of devices with different growth modes: (a) electron accumulation region, (b) hole accumulation region. Transfer characteristics of devices with mode 3 under different test times: (c) electron accumulation region, (d) hole accumulation region.

Table I. Carrier mobilities ($cm^2 \cdot V^{-1} \cdot s^{-1}$) and air stability of devices with different growth modes.

Device process	Within 2 h		1 day later		7 days later	
	μ_p	μ_n	μ_p	μ_n	μ_p	μ_n
Mode 1	0.09	0.05	0.05	0.009	0.04	—
Mode 2	0.09	0.06	0.08	0.01	0.06	—
Mode 3	0.11	0.10	0.08	0.02	0.06	0.006
Mode 3+PS	0.41	0.40	0.17	0.32	0.12	0.25

mobilities in the three modes are generally the same (see Table I for detail), which is $0.1 \pm 0.01\,cm^2 \cdot V^{-1} \cdot s^{-1}$. The gate voltage when the channel current becomes minimum is much higher than expected when $V_{DS} = 40\,V$, and V_{GS} even becomes positive when $V_{DS} = -40\,V$, which is different from most results in the literature.[12–14] However, the positive shift of V_{GS} is also observed in the PTCDI-C8/quaterrylene heteromolecular layer, which could be explained by the presence of intrinsic hole carriers in the hole-transporting layer.[15] When intrinsic hole carriers exist, more positive V_{GS} is needed to deplete the hole carriers for the electron carrier accumulation and less negative V_{GS} for hole carrier accumulation. The presence of intrinsic hole carriers can be proved on the basis of the hole current when there is no gate bias ($V_{GS} = 0\,V$). The origin of the intrinsic hole carriers could be the impurity of the material, structural defects, and involuntary doping by oxygen.

Large threshold voltage shifts during the electrical tests are observed for all the three growth modes. Figures 1(c)–1(d) are the transfer curves of devices with mode 3 for different test times. The threshold voltage shifts for electron and hole are more than 30 and 5 V, respectively, and the off-state current decreases as the test time increases. This suggests that there are large amounts of charge traps on the surface of SiO_2.[16,17] For $V_{DS} = \pm 40\,V$, we calculate the electron and hole trap densities on the surface of SiO_2 to be 4.3×10^{11} and $7.9 \times 10^{11}\,cm^{-2}$, respectively, using the following equation:[18] $N_{trap} = C_i \times |V_T - V_{TO}|/q$, in which C_i is the gate dielectric capacitance density, q is the electronic charge, V_T is the threshold voltage, and V_{TO} is the turn-on voltage, which is defined as the gate voltage when dI_{DS}/dV_{GS} becomes positive [V_T and V_{TO} are tagged in Figs. 1(c)–1(d)].[19] As for the air stability, devices with the three modes do not seem to be good. The electron mobility drops drastically after one day and almost no field effect is observed after one week of storage in air ambient. However, this is in accordance with the property of PTCDI-C13, since it fails easily in air ambient as we mentioned earlier. It is worth mentioning that devices with mode 3 still show electron mobility of $0.006\,cm^2 \cdot V^{-1} \cdot s^{-1}$, which proves that the changing growth rate method can promote the air stability of ambipolar devices to some degree.

To further understand the influence of the growth rate, we investigate the morphology of the PTCDI-C13 films at different growth stages. Figure 2 shows the AFM topography images, in which A1–A3 are 5, 20, and 50 nm PTCDI-C13 films deposited on 12 nm pentacene under mode 1, while B1–B3 and C1–C3 are those under modes 2 and 3, respectively. The topography images show rod-like grains at the early stage (A1, B1, and C1). The average grain sizes of modes 1 and 2 are generally the same, around 120 nm, and those located at the gaps of pentacene films are even smaller. Although the grain gaps are wider for mode 3 (C1) than those in A1 and B1, the grain sizes are much larger, which are around 200 nm. As can be seen from C2, the grain gaps in C1 are well filled-in, and the grain sizes located at the gaps of pentacene films are much larger compared with those in A2 and B2. It is known that carriers are accumulated and transport in the first several molecular layers, thus, we think that the larger grain sizes at the early stage of mode 3 are attributed to the higher electron carrier mobility. In addition, the grain boundary depth (defined as the vertical distance from upper layer to inner layer along the gap of grain boundary) will reduce the physical adsorption of O_2/H_2O molecules,[11] which is known as the main device failure factor. Judging from A4, B4, and C4, the average grain boundary depth (averaged from measurements of the depths of more than 30 grain boundaries in the corresponding AFM cross-sectional height image) for A3, B3, and C3 are 4.45, 4.83, and 3.14 nm, respectively. We think this may be the reason why devices with mode 3 have better air stability than those with modes 1 and 2.

In order to diminish the shifts of threshold voltage and improve the carrier mobilities, we modify the substrate with PS and fabricate the device using mode 3. The AFM topography images are shown in Fig. 2. The pentacene film on PS (E2) is smoother than that on bare SiO_2, and there are fewer gaps. The average grain sizes of PTCDI-C13 at the early stage (D1) are around 160 nm, which are smaller than those in C1 but with much narrower gaps. The average grain boundary depth is 2.44 nm. Figures 3(a)–3(b) show the output curve and transfer curve of the devices, respectively. The hole threshold voltage shifts negatively for more than 18 V compared with those without modification, and no threshold voltage shifts are observed during the electrical tests, which indicates a sharply reduced number of charge traps. The electron threshold voltage is also obviously reduced, from the typical value of 55 V before modification to 40 V after modification at $V_{DS} = 40\,V$. The calculated electron and hole trap densities are now only 2.4×10^{11} and $2.7 \times 10^{11}\,cm^{-2}$, respectively. Thus, modification of PS on SiO_2 can greatly reduce the charge surface traps, which is the key factor for the carrier mobility enhancement. For

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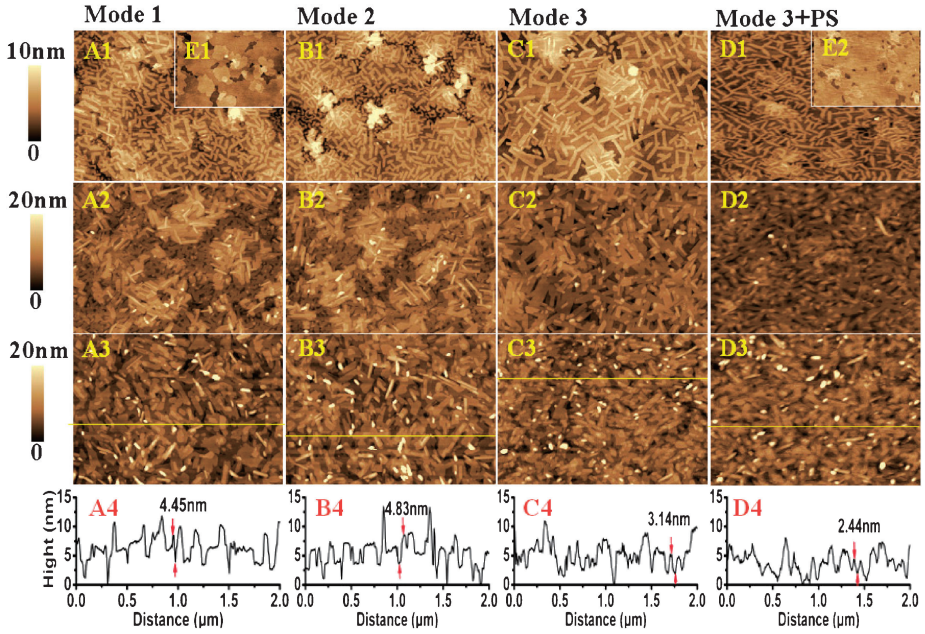

Fig. 2. AFM topography ($2 \times 1.4\,\mu m^2$) and cross-sectional height images of relevant films. A1–A3 are 5, 20, and 50 nm PTCDI-C13, respectively, grown on 12 nm pentacene under mode 1; B1–B3 and C1–C3 are those under modes 2 and 3, respectively; A4–D4 are corresponding cross-sectional height images in A3–D3; E1 and E2 are 12 nm pentacene on bare SiO_2 and PS modified SiO_2, respectively.

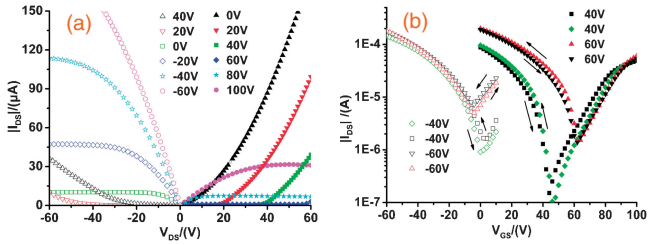

Fig. 3. Characteristics of devices with PS modification of the substrate: (a) output curve; (b) transfer curve.

$V_{DS} = \pm 60$ V, the hysteresis is negligible and the calculated (C_i is determined to be $\sim 9.6\,nF{\cdot}cm^{-2}$ by Keithley 4200 SCS through the same way) hole and electron mobilities in the saturation regime are 0.41 and $0.40\,cm^2{\cdot}V^{-1}{\cdot}s^{-1}$, respectively, which is the highest for air-stable ambipolar OFETs so far. Moreover, the air stability of the devices is also good. For devices stored in air ambient for one week, the electron mobility drops to less than half. It is worth mentioning that the hole mobility drops more drastically than the electron mobility, which is different from p-type OFETs based on pentacene. However, it agrees with what Choi's group[6] observed in their ambipolar OFETs fabricated by the NCBD method. As they state, this may be because of the existence of the relatively larger hole traps than electron traps after the surface modification with PS. The detailed failure mechanism in this situation needs further investigation, which is beyond the scope of this paper.

In conclusion, air-stable ambipolar OFETs based on pentacene and PTCDI-C13 with high and balanced carrier mobilities are demonstrated, which is in favor of high-performance OLEFETs and organic lasers. The changing growth rate of the PTCDI-C13 layer and surface modification of the dielectric layer are proved to contribute to the considerable enhancement.

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