Journal of
Nanoscience and Nanotechnology
Vol. 8, 1234–1237, 2008

Behavior of TiO_2 Thin Film in a Nanocapacitor

Dongdong Jia[1], C. Shaffer[1], S. Pickering[1], A. Goonewardene[1], and Xiao-Jun Wang[2,3,*]

[1] Department of Geology and Physics, Lock Haven University of Pennsylvania, Lock Haven, PA 17745, USA
[2] Department of Physics, Georgia Southern University, Statesboro, GA 30460, USA
[3] Key Laboratory of Excited Processes, CIOMP, Chinese Academy of Sciences, Changchun 130033, China

Gold and platinum nanocapacitors have been fabricated using a magnetron sputtering technique. TiO_2 is used as a dielectric material to separate the metal layers which act as the parallel plates for the capacitors. The thickness for metal films and TiO_2 layer is 80 nm and 400 nm, respectively. Capacitance of the nanocapacitors has been measured and dielectric constant of TiO_2 calculated. Both capacitance and dielectric constant are observed to have strong frequency dependence.

Keywords: TiO_2, Nanocapacitor, Sol–Gel.

1. INTRODUCTION

Electronic devices for a micro electromechanical system (MEMS) are often with a dimension of a couple of micrometers, with which the device structures are close to one made by bulk materials. The low dimension effect is not very obvious at this scale. When the microscale devices are further reduced to nanoscale the size effect strongly exhibits. For a device in a nano electromechanical system (NEMS) the low dimension may induce a dramatic change in its physical properties. For example, a low dimensional conductor presents a tremendous increase of resistivity.[1] Therefore, the research on the physical properties of low dimensional electronic devices is essential.

Recently, there has been an increasing demand for high dielectric constant insulators to make high-density dynamic-memory.[2,3] Among these insulators, titanium dioxide thin films have attracted considerable attention for use in fabricating capacitors in microelectronics devices because of its high dielectric constants.[4] As one of the simplest transition-metal oxides, many methods have been developed to prepare titanium oxide thin films, such as thermal or anodic oxidation of titanium, chemical vapor deposition, sol–gel dip coating, and reactive sputtering.[5,6] Optical, structural and electromagnetic properties of TiO_2 have been intensively studied.[7–9]

TiO_2 has a dielectric constant of 100, which is one of the highest and is ideal for fabrication of electronic devices such as transistors or capacitors. In this work, TiO_2 are used as a dielectric material for fabrication of nanocapacitors. Gold and platinum are used to deposit the two parallel plates for capacitor on silicon and glass substrates using a sputtering technique. A simple masking technique is used to shape the capacitors and associated electrodes. The capacitances of the nanocapacitors have been measured and the frequency dependence of the capacitances and dielectric constants discussed.

2. EXPERIMENTAL DETAILS

The structure of the capacitors that have been fabricated is sandwich structure where two metal thin layers are separated by a TiO_2 layer. The metal layers are 80 nm thick which were deposited using a magnetron sputtering technique. The deposition is done using a Hummer VI sputter coater and the metal sources are gold and platinum. The thickness of the layers is controlled by measuring the deposition time with a known deposition rate. The thickness is measured with an Ambios Technology XP Stylus Profiler which has a resolution of 0.5 Å. A mask with a shape of a 1 cm by 1 cm square plus a 5 mm by 2 mm tail electrode is made with a thin plastic film. A schematic structure of a capacitor is shown in Figure 1.

Between the depositions of the two metal layers, a thin TiO_2 layer is coated using a sol–gel dip coating technique.[6] A TiO_2 sol–gel solution is prepared according the following processes. A 350 cc isopropanol and 25 cc Ti (isopropanol) solution is prepared as a precursor. The precursor is mixed with alcohol and a 0.4 cc 2 M HCl is added drop by drop under stirring with a magnet. The TiO_2 sol suspension is dip-coated onto the metal layer (the electrode was protected). The sol is gelled and is quickly air dried. The TiO_2 film is cured at 120 °C for 1 hour in a furnace. The thickness of the TiO_2 thin-film is 400 nm.

The morphology of the TiO_2 layer has been identified with a Veeco CPII atomic force microscope (AFM). The

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[*] Author to whom correspondence should be addressed.

1533-4880/2008/8/1234/004 doi:10.1166/jnn.2008.315

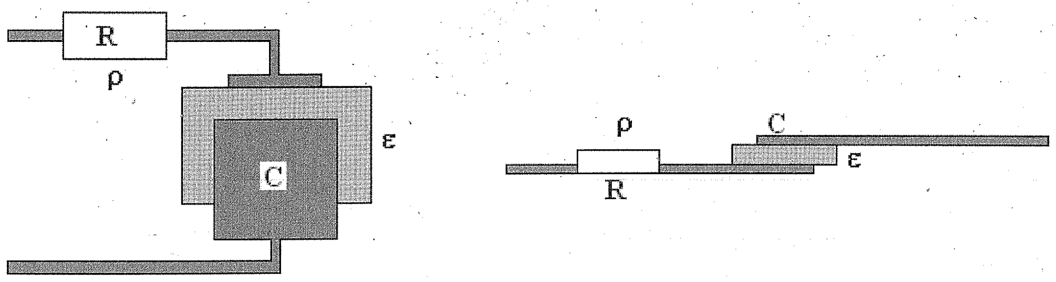

Fig. 1. A sketch of the capacitor structure with capacitance C, dielectric constant ε, and resistance (resistivity) R (ρ).

structure of the capacitor is confirmed using a TESCAN VEGA II SBH scanning electron microscope (SEM). The capacitances of the capacitors are characterized using a HP impedance analyzer. A layer of DuPont conductive paste is painted across each side of the capacitor electrodes to ensure a proper contact between the capacitor and the impedance analyzer.

3. RESULTS AND DISCUSSION

The thicknesses for capacitor metal plates on glass or silicon substrates and TiO_2 layer are measured as shown in Figure 2. The morphology of the TiO_2 thin film is determined using an AFM. The thin-film TiO_2 is smooth and the maximum roughness is less than 8 nm and the average roughness is about 1.5 nm, as shown in Figure 3. A SEM cross sectional view of sandwich structure of the device is presented in Figure 4.

Comparing the total thickness of less than 1 μm for the capacitor, including the metal films and the TiO_2 layer, to its dimensions of 1 cm by 1 cm, the structure can be considered as a perfect infinite plane capacitor with the capacitance given by

$$C = \varepsilon_o \varepsilon_r A/d \tag{1}$$

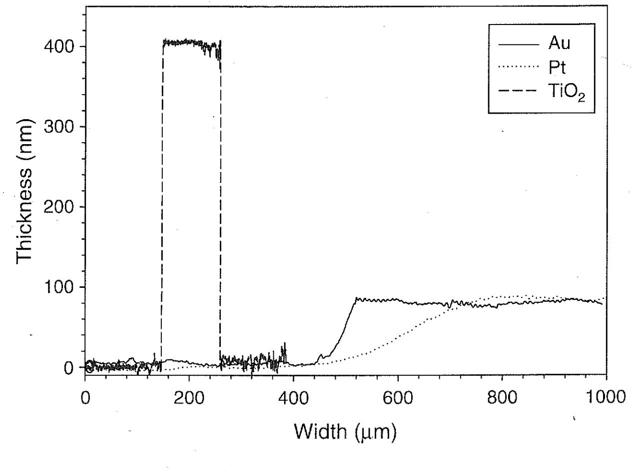

Fig. 2. Thickness as a function of horizontal width for gold metal layer (solid line), platinum metal layer (dotted line), and TiO_2 layer in between the metal layers (dashed line). The background around zero represents the substrate surface.

where C is the capacitance, ε_r the dielectric constant of TiO_2, ε_o the free space permittivity, d the thickness of the TiO_2 layer, and A the area of the plate.

The electrodes designed on both sides are for electrical connections to the capacitor. To obtain a better contact and avoid short circuit, they are coated with conductive paint. The electrodes introduce more resistance because of the low dimension effect of a metal layer. Along the vertical direction, the thickness of the electrodes is less than 100 nm that is significantly smaller than the electron mean-free-path in bulk metal materials. Therefore, the collisions of electrons at the thin-film boundaries (the interface between substrate/metal and metal TiO_2) create similar effect to the collisions with the metal atoms in the lattice. These additional collisions strongly scatter the electrons in the metal, decreasing the mobility of the electrons in the structure so that the resistivity of the metal layers highly increases.

A carrier scattering theory has been developed by Fuchs.[10] It describes that the electrical resistivity ρ of thin metal films increases with decreasing film thickness t. The analysis assumes that every collision between an electron

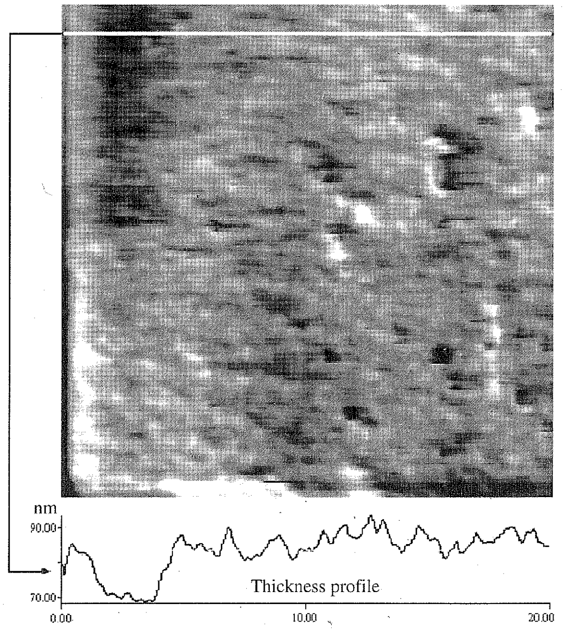

Fig. 3. Morphology of TiO_2 layer and thickness profile.

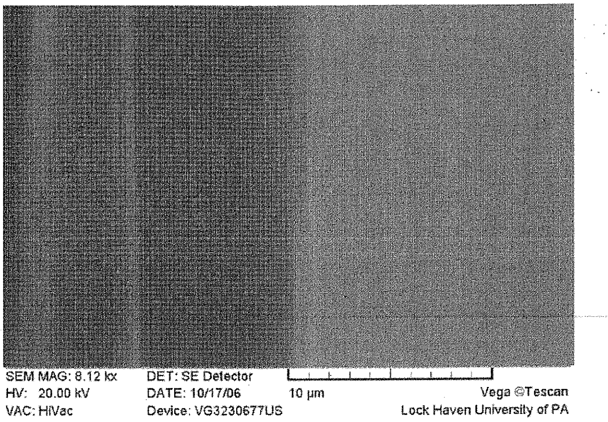

Fig. 4. SEM image of the capacitor cross section. The darkest area represents the Si substrate. The capacitor is fabricated on the right surface of the substrate, where the two stripes depict the metal plates and the darker stripe in between the dielectric material (TiO_2).

and one of the surfaces terminates the free path of the electron so that the scattering is entirely diffusive.[11] The resistivity is therefore given by

$$\rho = \rho_o\left(1 - 3\lambda/2t\int_0^{1/2\pi} \sin^3\theta\cos\theta(1 - e^{-t/\lambda\cos\theta})\,d\theta\right) \quad (2)$$

where ρ_o is the bulk resistivity, t the film thickness, and λ the electron mean-free-path. Once the resistivity is determined the resistance on the electrodes can be readily calculated using the dimensional information,

$$R = \rho L/S \quad (3)$$

where L is the length of the metal electrode and S the cross-section of the metal electrodes. For a film thickness about 100 nm, the resistivity ρ is estimated by Eq. (2) to be $3\times10^{-6}\ \Omega\cdot\text{m}$ for gold. The capacitance is then calculated by Eq. (3) to be a value of tens of Ohms, which is consistent with our measured value using a four probe technique for Au.

The metal-oxide-metal structure of the nanocapacitor fabricated in this work forms a simple RC circuit of itself. The impedance Z of such a structure is given by[12–15]

$$Z = 1/i\omega RC_0\varepsilon^* \quad (4)$$

where ω is the frequency, $C_0 = \varepsilon_0 A/d$ the capacitance of the capacitor with the same structure but without TiO_2 as defined in Eq. (1), and R the resistance on the capacitor. The complex ε^* is given by $\varepsilon' - i\varepsilon''$ which includes both the dielectric constant ε' and the dielectric loss $\varepsilon'' = 1/\omega RC_0$.

As a dielectric material, the dielectric constant of TiO_2 is strongly frequency dependent,[15–17] reflecting the frequency dependence of the capacitance. The capacitances of the devices are measured and presented in Figure 5(a–d). The frequency dependences for Au and Pt are similar in the frequency range from a few Hz to several MHz. It indicates that there exists the same reduction of Ti^{4+} at the boundaries between Au or Pt and TiO_2. The capacitance is slightly higher for the capacitor fabricated on Si substrate than that on glass substrate for both Au and Pt plates. The reason is that the roughness is 10 nm for glass substrate but while 0.2 nm for Si substrate. The greater roughness causes more non-uniform coating of the metal layers. As a result, the capacitance is reduced for the capacitors fabricated on glass.

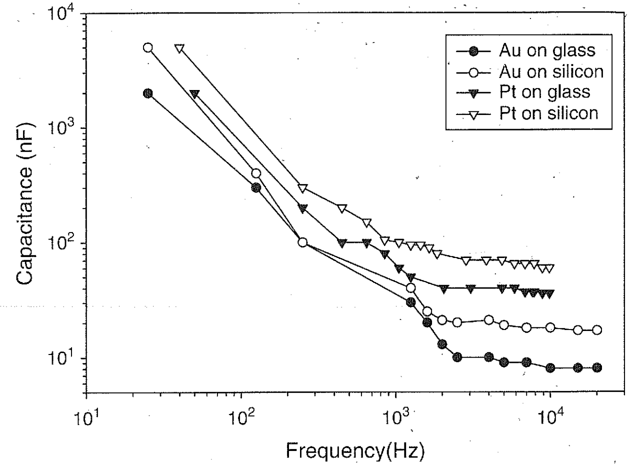

Fig. 5. Frequency dependence of TiO_2 dielectric constant for (a, solid circles) gold capacitor on glass, (b, empty circles) gold capacitor on Si, (c, solid triangles) platinum capacitor on glass, and (d, empty triangles) platinum capacitor on Si.

4. CONCLUSION

Nanocapacitors have been fabricated on glass and Si substrates using Au or Pt as plane plates and TiO_2 as the dielectric materials. Structure and morphology of the nanocapacitors are characterized. An increase of resistivity of the Au and Pt metal layers with a nanoscale dimension is found and analyzed. Frequency dependent dielectric constants of TiO_2 in different nanocapacitors are measured. The results show less effect of metal layers on the dielectric property of thin-film TiO_2. Surface roughness of the substrates reduces the capacitance of the devices.

Acknowledgments: One of the authors Xiao-Jun Wang is grateful for the support from the National Natural Science Foundation of China (No. 10574128) and the MOST of China (No. 2006CB601104).

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Received: 8 February 2007. Accepted: 2 May 2007.