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Bottom-contact organic field-effect transistors having low-dielectric layer under source and drain electrodes

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An organic thin-film transistor (OTFT) having a low-dielectric polymer layer between gate insulator and source/drain electrodes is investigated. Copper phthalocyanine (CuPc), a well-known organic semiconductor, is used as an active layer to test performance of the device. Compared with bottom-contact devices, leakage current is reduced by roughly one order of magnitude, and on-state current is enhanced by almost one order of magnitude. The performance of the device is almost the same as that of a top-contact device. The low-dielectric polymer may play two roles to improve OTFT performance. One is that this structure influences electric-field distribution between source/drain electrodes and semiconductor and enhances charge injection. The other is that the polymer influences growth behavior of CuPc thin films and enhances physical connection between source/drain electrodes and semiconductor channel. Advantages of the OTFT having bottom-contact structure make it useful for integrated plastic electronic devices. © *2003 American Institute of Physics.* [DOI: 10.1063/1.1580646]

Recently organic thin-film transistors (OTFTs) have attracted tremendous attention due to their potential application in low-cost large-area flexible displays and low-end electronics.[1–5] Now, their performance can compare with hydrogenated amorphous silicon thin-film transistors (*a*-Si:H TFT).[6–9] Because organic semiconductors are generally sensitive to solvents and chemicals used in photolithographic processing, OTFT performance is degraded when using traditional patterning methods in device fabrication.[10] Therefore, bottom-contact structure devices, which are fabricated by depositing the active organic material onto patterned source/drain electrodes to avoid or minimize exposure to solvents and chemicals, become ideal structures for organic electronics. However, the performance of OTFTs in a bottom-contact structure is generally lower than that of devices in a top-contact structure since the contact area between accumulated layer and source/drain electrodes is small.[11] Surface modification of source/drain electrodes using a surfactant has recently been used to improve the physical connection between electrode and semiconductor channel, and it can enhance the performance of bottom-contact devices.[12,13]

On the other hand, the operating voltage of OTFTs is often too high for practical use. Metal oxide film, having a relatively high dielectric constant ϵ as the gate insulator, can be used to overcome this shortcoming.[14] However, high-dielectric-constant materials usually have the disadvantage of high gate leakage currents.

In this letter, a specific structure of an OTFT device [shown in Fig. 1(a)] is presented to improve the performance of bottom-contact devices. The concept is based on a bottom-contact-structure OTFT having high-dielectric-constant Ta_2O_5 as an insulator. A low-dielectric insulating layer, poly(methylmethacrylate) (PMMA), is located between gate insulator and source/drain electrodes to reduce leakage current. For comparison, bottom-contact and top-contact devices [shown in Figs. 1(b) and 1(c)] have been fabricated under the same conditions.

Corning7059 glass is used as a substrate, and magnetron-sputtered metal Ta is used as a gate electrode. The Ta_2O_5 film, which has a capacitance of 66 nF/cm^2, is deposited as a gate insulator using magnetron reactive sputtering. A 150-nm PMMA layer is coated on top of the Ta_2O_5 gate insulator as additional insulator layer. Gold source and drain electrodes (a 20-nm-thick Al layer is used under a 60-nm-thick Au layer for adhesion between the Au layer and insulator) are thermally evaporated on top of the insulator layer through a shadow mask with a defined channel width and length of 1200 and 80 μm, respectively. The unwanted part of the polymer is removed by a self-alignment dry etch in O_2 plasma using source and drain electrodes as a mask. Finally, the organic semiconductor of 200-nm CuPc is deposited at room temperature. Before deposition of the active layer, the device is annealed at 70 °C under a vacuum of 10^{-5} Pa in order to remove O_2 absorbed during dry etching. Current–voltage measurements are carried out in air and at room temperature using KEITHLEY 236 voltage source units.

Figures 2(a) and 2(b) show output and transfer characteristics of an OTFT device in bottom-contact structure. From the curve of square root of drain current versus gate voltage at constant -50 V drain–source voltage, carrier mobility is estimated to be 7.3×10^{-4} cm^2 V^{-1} s^{-1}, which is similar to the value reported by Bao *et al.* for a room-temperature CuPc TFT device.[15] Threshold voltage is about

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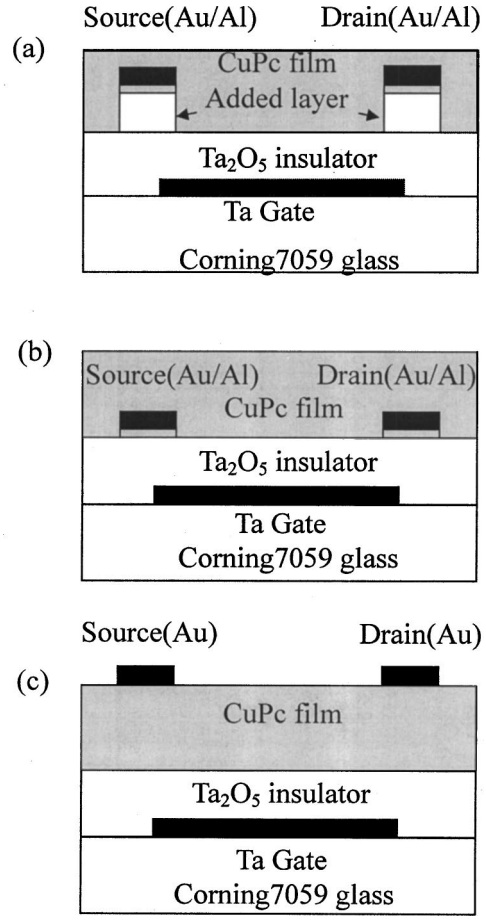

FIG. 1. Schematic structures of OTFT devices: (a) our structure, (b) bottom-contact structure, and (c) top-contact structure.

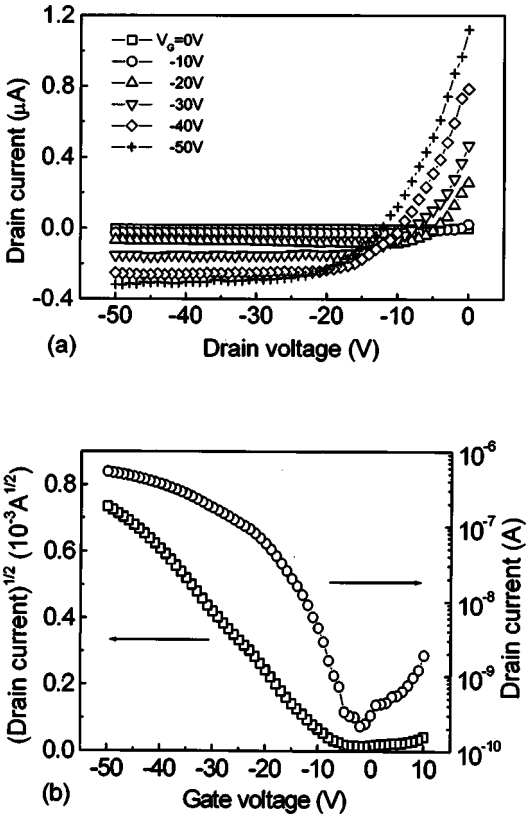

FIG. 2. Output and transfer characteristics of the bottom-contact structure device: (a) I_D vs V_D for a series of gate voltages and (b) I_D and $I_D^{1/2}$ vs V_G for a fixed drain–source voltage of -50 V.

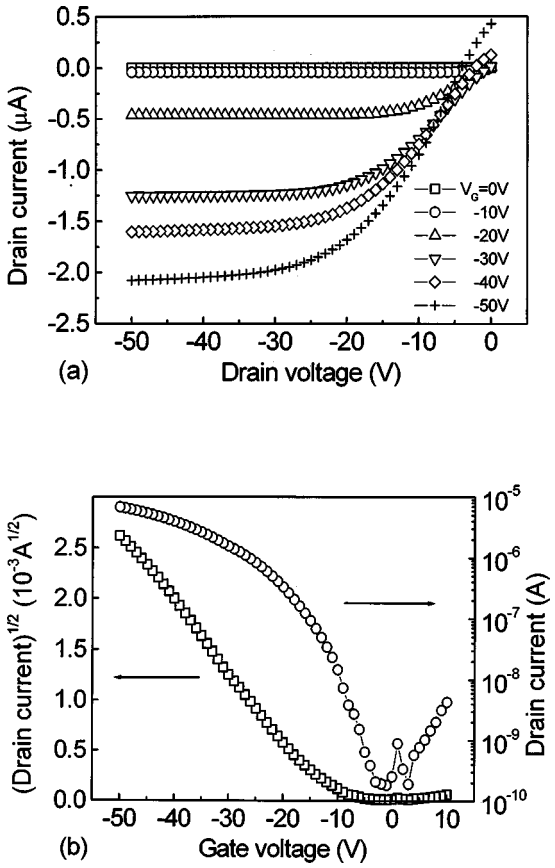

FIG. 3. Output and transfer characteristics of the top-contact structure device: (a) I_D vs V_D for a series of gate voltages and (b) I_D and $I_D^{1/2}$ vs V_G for a fixed drain–source voltage of -50 V.

-7.5 V, and on-state current is 3×10^{-7} A. The positive current near $V_{DS}=0$, increasing with V_{GS}, is due to leakage between source/drain and gate electrodes through the gate insulating layer. The field-effect mobility is estimated in the saturation regime using Eq. (1):

$$I_D = W/2L\mu_{EF}C_i(V_G - V_T)^2. \tag{1}$$

Figures 3(a) and 3(b) show output and transfer characteristics of an OTFT device in top-contact structure. From the curve of square root of drain current versus gate voltage at constant -50 V drain–source voltage, carrier mobility is estimated to be 0.01 $cm^2\,V^{-1}\,s^{-1}$. Threshold voltage is about -12 V, and on-state current is 2.1×10^{-6} A. It can be seen that the properties of the top-contact device are much better than those of the bottom-contact device.

Figures 4(a) and 4(b) show output and transfer characteristics of an OTFT device in our structure. From the curve of the square root of the drain current versus gate voltage at a constant -50 V drain–source voltage, carrier mobility is estimated to be 0.01 $cm^2\,V^{-1}\,s^{-1}$, which is more than one order of magnitude higher than that of the normal bottom-contact device and is almost the same as that of the top-contact device. It has threshold voltage of -12.5 V. At a gate–source voltage of -50 V, the device has an on-state current of 2.36×10^{-6} A, which is almost one order of magnitude higher than that of the normal bottom-contact device. Leakage currents between source/drain and gate electrodes through the gate insulating layer are greatly reduced (from 1.1×10^{-6} to 3.5×10^{-7} A, at $V_G=-50$ V).

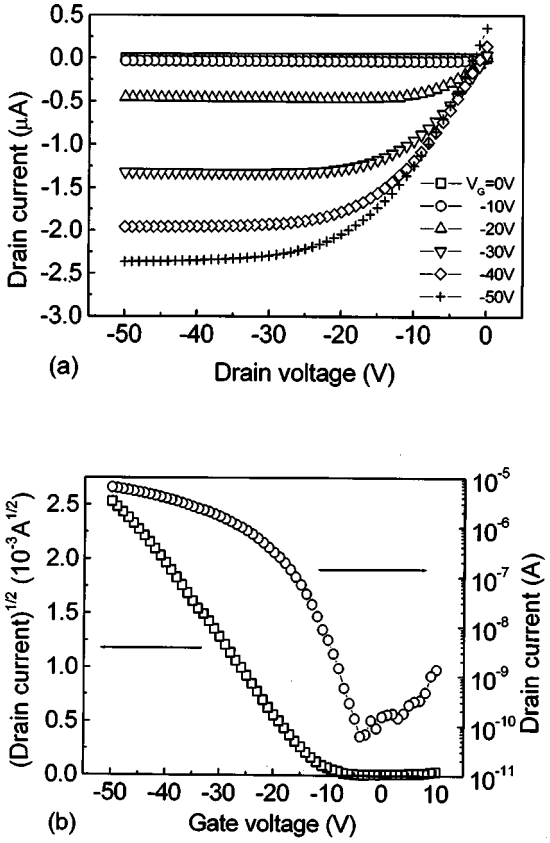

FIG. 4. Output and transfer characteristics of structure device: (a) I_D vs V_D for a series of gate voltages and (b) I_D and $I_D^{1/2}$ vs V_G for a fixed drain–source voltage of −50 V.

Morphology of CuPc thin films is observed using a SPI3800N atomic force microscope (AFM). An area near the source/drain electrode is shown in Fig. 5. CuPc thin films on the top of Ta_2O_5 layer are polycrystalline. Grain sizes near electrodes are larger than that of crystals in the middle of channel. The growth of the semiconductor layer is modified in the channel area, either the polymer layer has not been removed completely or the Ta_2O_5 surface is chemically modified by exposure to O_2 plasma.

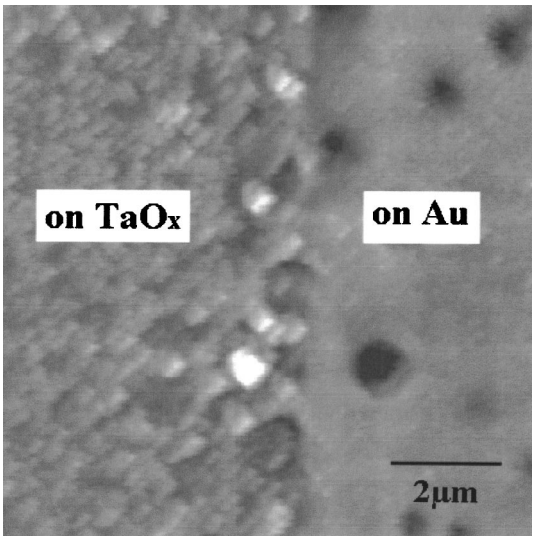

FIG. 5. An AFM image of CuPc thin film near the source/drain electrode. The grain size in the CuPc layer varies across the channel.

The low-dielectric polymer may play two roles to improve OTFT performance. One is modification of electric-field distribution between source/drain electrodes and the semiconductor channel and thereby enhanced charge injection. The additional layer has a low-dielectric constant similar to organic semiconductor, and redistributes the electric field to fall on the semiconductor near the area connecting to the electrode. The other reason confirmed by AFM observation is that the polymer influences the growth behavior of CuPc thin films and enhances the physical connection between source/drain electrodes and semiconductor channel.

Our OTFT structure dramatically improves electronic properties of the OTFT device, such as mobility and on-state current. Moreover, the additional insulating layer can depress leakage current derived from overlap of gate/source and gate/drain, and it can reduce parasitic capacitance derived from gate/source and gate/drain overlap. Those qualities are also very valuable when this structure is used in integrated circuits and active matrix displays. Combining its advantage in fabrication, our OTFT in a bottom-contact structure is suitable for application in integrated plastic electronic devices.

In summary, a bottom-contact organic thin-film transistor having a low-dielectric layer under source and drain electrodes is demonstrated. It has the advantages of a bottom-contact device for easy integration, and has the high performance of a top-contact device. The low-dielectric insulating layer reduces leakage current and parasitic capacitances derived from gate/source and gate/drain overlap.

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[1] C. J. Drury, C. M. J. Mutsaers, C. M. Hart, M. Matters, and D. M. de Leeuw, Appl. Phys. Lett. **73**, 108 (1998).
[2] H. Klauk, D. J. Gundlach, J. A. Nichols, and T. N. Jackson, IEEE Trans. Electron Devices **46**, 1258 (1999).
[3] M. Matters, D. M. de Leeuw, M. J. C. M. Vissenberg, C. M. Hart, P. T. Herwig, T. Geuns, C. M. J. Mutsaers, and C. J. Drury, Opt. Mater. **12**, 189 (1999).
[4] B. Crone, A. Dodabalapur, Y. Y. Lin, R. W. Filas, Z. Bao, R. Sarpeshkar, H. E. Katz, and W. Li, Nature (London) **403**, 521 (2000).
[5] C. D. Sheraw, L. Zhou, J. R. Huang, D. J. Gundlach, T. N. Jackson, M. G. Kane, I. G. Hill, M. S. Hammond, J. Campi, B. K. Greening, J. Francl, and J. West, Appl. Phys. Lett. **80**, 1088 (2002).
[6] Y. Y. Lin, D. J. Gundlach, S. Nelson, and T. N. Jackson, IEEE Electron Device Lett. **18**, 606 (1997).
[7] D. J. Gundlach, Y. Y. Lin, T. N. Jackson, S. F. Nelson, and D. G. Schlom, IEEE Electron Device Lett. **18**, 87 (1997).
[8] S. F. Nelson, Y. Y. Lin, D. J. Gundlach, and T. N. Jackson, Appl. Phys. Lett. **72**, 1854 (1998).
[9] C. D. Dimitrakopoulos and P. R. L. Malenfant, Adv. Mater. (Weinheim, Ger.) **14**, 99 (2000).
[10] D. J. Gundlach, T. N. Jackson, D. G. Schlom, and S. F. Nelson, Appl. Phys. Lett. **74**, 3302 (1999).
[11] Y. Y. Lin, D. J. Gundlach, and T. N. Jackson, *54th Device Research Conference Digest*, 1996, p. 80.
[12] J. Wang, D. J. Gundlach, C. C. Kuo, and T. N. Jackson, *41st Electronic Materials Conference Digest*, June 1999, p. 16.
[13] C. D. Dimitrakopoulos and D. J. Mascaro, IBM J. Res. Dev. **45**, 11 (2001).
[14] C. Dimitrakopoulos, S. Purushothaman, J. Kymissis, A. Callegari, and J. M. Shaw, Science (Washington, DC, U.S.) **283**, 822 (1999).
[15] Z. Bao, A. J. Lovinger, and A. Dodabalapur, Appl. Phys. Lett. **69**, 3066 (1996).