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High-power InGaAs VCSEL's single devices and 2-D arrays

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Abstract

Single devices and 2-D arrays of bottom-emitting vertical-cavity surface-emitting lasers operating in the 980 nm wavelength regime, have been fabricated for high continuous-wave optical output power. Single devices with active diameters of 500 μm show high output powers of 1.95 W at room temperature. Its threshold current is 510 mA, and the maximum spatially averaged optical power density is 0.93 kW/cm^2. Arrays consisting of 16 elements of 200 μm active diameters arranged in a square structure achieve output powers of 1.21 W corresponding to a power density of 1 kW/cm^2 spatially averaged over the effective array chip size. The device threshold current is 1.1 A.

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Keywords: VCSELs; 2-D arrays; Quantum well; High power; 980 nm

1. Introduction

The growing demand for high-power laser diodes in industrial applications has already lead to edge-emitting semiconductor lasers with high output power and improved beam profile and reliability [1]. Similarly, various studies on vertical-cavity surface-emitting lasers (VCSELs) aim at the increase of the optical output power [2]. Improvements of the epitaxial material, optimized processing like wet oxidation of the current aperture, improved device design, and an established mounting technique for heat removal have lead to VCSELs that emit watt regime for single devices as well as for arrays [3]. The 2-D scaling capability is also interesting in high-power applications like laser diode pumped solid-state laser. The VCSELs emitting at 980 nm are desirable for pumping solid-state lasers [4] and Er-doped optical amplifier. To increase the overall optical output power, the total lasing area of VCSELs has to be enlarged. This can be done by increasing the active area of single devices [5] or arranging devices in 2-D arrays [6,7].

In this paper, we report on a high-power bottom-emitting $In_{0.2}Ga_{0.8}As/GaAs$ vertical-cavity surface-emitting laser and 4×4 2-D laser array which provide high output powers in the 980 wavelength regime. Both the single devices and 2-D arrays have been fabricated by using oxidation confinement technology. The maximum output power of the single device with a large aperture (500 μm diameter) is as high as 1.95 W at room temperature. The active region diameter of the individual element, which makes up of 2-D VCSEL array, is 200 μm. The spacing between the adjacent elements is 50 μm. The maximum continuous wave optical output power at room temperature is as high as 1.21 W. The size-dependent characteristics of output power is discussed.

2. Device structure and processing

The structure of the bottom-emitting VCSEL is shown in Fig. 1. The inner cavity contains three 8 nm-thick $In_{0.2}Ga_{0.8}As$ quantum wells embedded in 10 nm-thick GaAs barriers. $Al_xGa_{1-x}As$ cladding layers are used to

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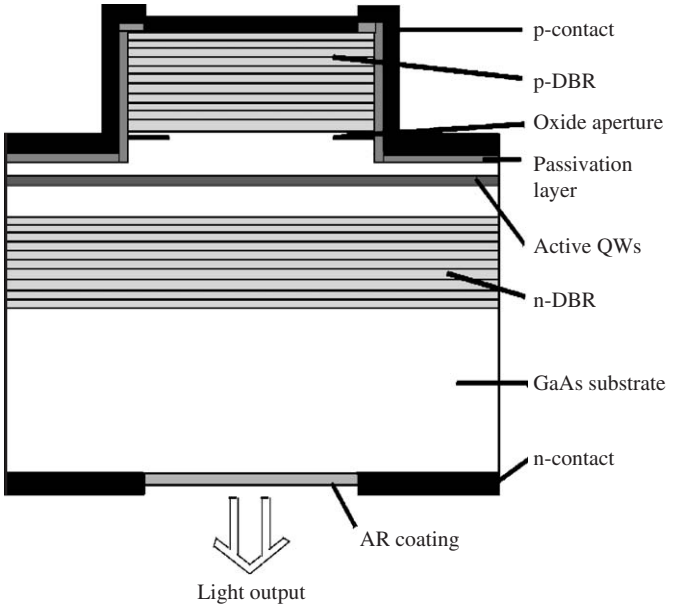

Fig. 1. Schematic layer structure of a bottom-emitting VCSEL.

form 1λ cavity. The carbon-doped p-type distributed Bragg reflector consists of 30 pairs of $Al_{0.9}Ga_{0.1}As/GaAs$ with graded interface to reduce series resistance. The top 40 nm GaAs contact layer is doped to a concentration of 1×10^{19} /cm^3 to achieve a good ohmic contact. There is a 30 nm-thick AlAs layer located between the active region and the top p-type mirror. This layer is oxidized and converted to Al_xO_y later in the fabrication process for current confinement and determining the active diameter of the device. The silicon-doped n-type distributed Bragg reflector (DBR) has only 20 pairs of the same material for bottom emission through the GaAs substrate. The device structure is grown by metal organic chemical vapor deposition (MOCVD). Wet chemical etching is used to define a circular mesa, with a depth down to the AlAs layer. The exposed AlAs layer is laterally oxidized at 420 °C with nitrogen carrier gas bubbled through water at 90 °C. After oxidation, the surface is passivated with Al_2O_3 and a circular window on top of the mesa is opened for evaporating a full size p-type contact consisting of Ti–Au–Pt–Au to provide a homogeneous current distribution and serve as a metal pad for soldering. The contact is annealed and thick gold is plated over the pillar to facilitate heat sinking and future bonding. The GaAs substrate is mechanically thinned and chemically polished down to about 180 μm to decrease the substrate contribution to series resistance, and an antireflection coating of HfO_2 with quarter-wavelength thickness is deposited on the polished substrate. Ge–Au–Ni–Au is evaporated around the HfO_2 window to form the large-area electrical contact. The whole chip is annealed at 380 °C in nitrogen environment condition for 60 s. Finally, the device is simply soldered upon a small copper heat sink with indium solder.

3. Characterization of devices

Fig. 2 shows the *L–I* characteristics for a 500 μm active diameter single device. The VCSELs exhibit a threshold current, threshold voltage, and differential resistance of 0.88 A, 1.9 V and 0.05 Ω, respectively. A maximum CW operation output power of 1.95 W is achieved at room temperature. The slope efficiency shows a slight decrease due to the internal heating while working at high current. The inset shows the lasing spectrum measured at a current of 6 A. The peak wavelength is 985.5 nm and the FWHM of the spectrum is 1.0 nm.

The 2-D arrays with 16 individual elements arranged in a square structure have been fabricated and soldered junction side down with In onto copper submounts for proper heat sinking. Fig. 3 shows the size-dependent *L–I* curves corresponding to array devices with 50, 100 and 200 μm diameter elements. The maximum output powers are 0.7, 1.01 and 1.21 W, respectively, which are limited by thermal rollover. Fig. 4 shows the emission spectrum of a 200 μm aperture size 4×4 arrays at 6 A CW laser current. The peak wavelength is 981.9 nm and the FWHM of the spectrum is 0.7 nm.

In order to understand the size dependence of the output characteristic, we developed a simplified model. The light–current characteristics are calculated from the stationary solutions of the rate equation [8], and temperature-dependent effects are taken into account by an empirical injection efficiency factor ($1\text{-}\Delta T/\Delta T_{\text{off}}$). Thus, the output power of the array is written as [9]

$$P_{\text{opt}}=\sum_{j=1}^{n}\frac{\hbar\omega}{q}(i_j-i_{\text{th}})\eta_{\text{d}}\left(1-\frac{\Delta T}{\Delta T_{\text{off}}}\right), \tag{1}$$

where the intrinsic temperature rise ΔT is calculated from

$$\Delta T=\sum_{m=1}^{n}R_{\text{th},jm}((v_k+i_mR_{\text{d}})i_m-P_{\text{opt},m}), \tag{2}$$

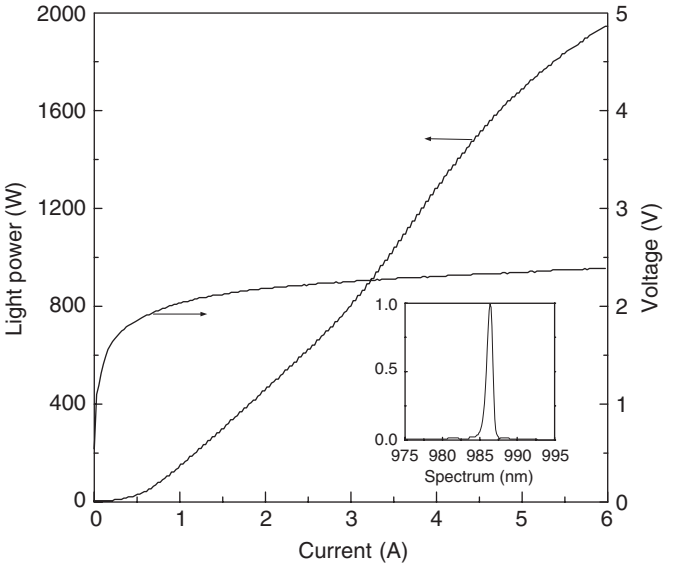

Fig. 2. *L–I* curves for a 500 μm active diameter single device.

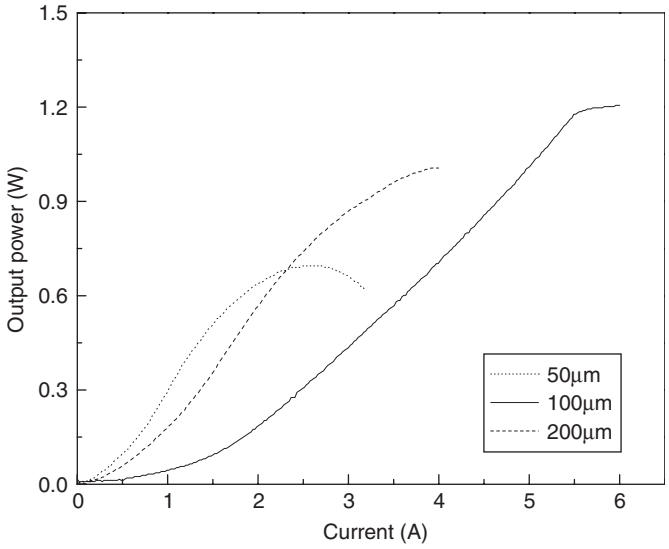

Fig. 3. Size-dependent L–I curves for array of various sizes.

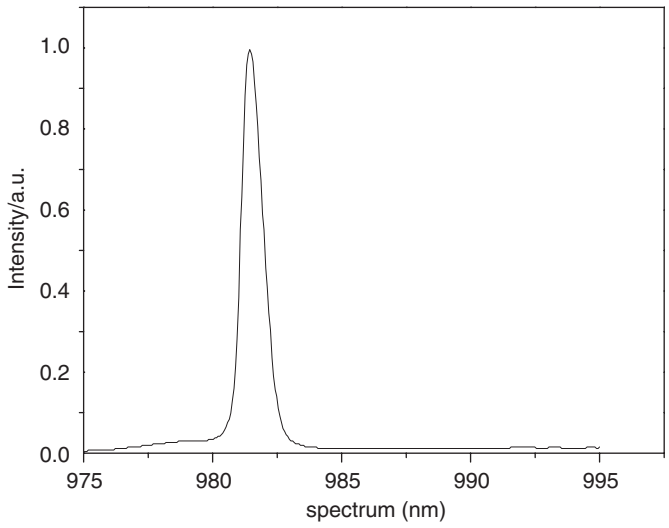

Fig. 4. Emission spectrum of a 200 μm aperture size 4×4 arrays at 6 A CW laser current.

where $\hbar\omega$ denotes the photon energy, q is the elementary charge, and η_d is the maximum differential quantum efficiency. ΔT_{off} is the turn-off temperature increase. $R_{th,jm}$, to which the thermal crosstalk conductivities between arbitrary ith and jth lasers add, is the effective thermal resistance [10]. v_k is the kink voltage and i_m, $P_{opt,m}$, are current and output power of the mth laser, respectively. In Fig. 5 the output characteristics for the 200 μm aperture-size 4×4 arrays are shown. The dashed line corresponds to simulations including thermal crosstalk, whereas the solid line describes the measured output power. A comparison shows good agreement in both absolute values and curvature of the L–I curves.

4. Conclusion

In conclusion, we have fabricated high-power VCSELs, single devices as well as 2-D arrays with proven potential for applications requiring output power in the watt regime. Single devices with active diameters of 500 μm show a high output powers of 1.95 W. Arrays consisting of 16 elements of 200 μm active diameters arranged in a 250 μm pitch square pattern achieve output powers of 1.21 W corresponding to a power density of 1 kW/cm^2 spatially averaged over the effective array chip size.

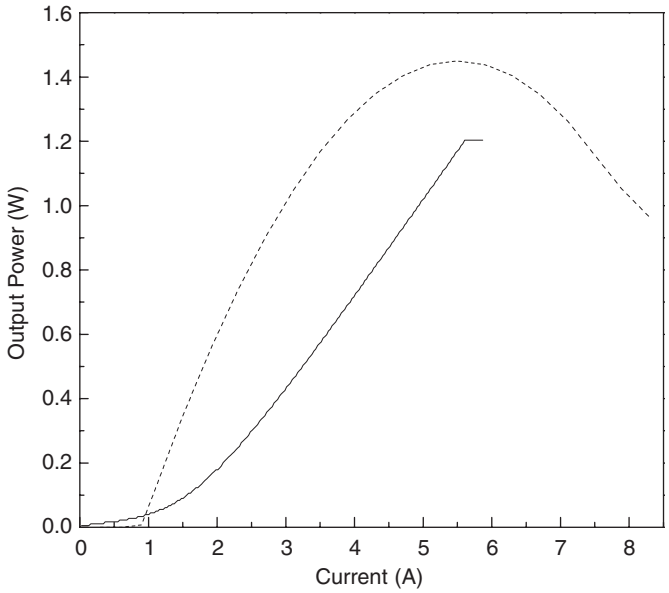

Fig. 5. Simulation and measured output characteristics of a 200 μm aperture size 4×4 arrays.

Acknowledgments

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