Simulation of Active-Matrix Electrophoretic Display Response Time Optimization by Dual-Gate a-Si:H TFT With a Common Gate Structure

Shu Yang and Hai Jing

***Abstract*—Large off-state drain–source current of the thin-film transistor (TFT) in active-matrix electrophoretic display (AMEPD) pixel leads to dramatic data voltage degradation, which causes severe crosstalk and undesired large response time. In this paper, the leakage current influence on response time is investigated and simulated. A compact model of response time t versus off-state drain–source current $I_{\rm off}$ is established. The simulation result induces that by reducing $I_{\rm off}$, the response time can be efficiently shorted. In order to reduce the off-state current, dual-gate amorphous silicon (a-Si:H) TFT with a common gate structure is discussed. Its current regulation mechanism is illustrated, and its fitness for driving the AMEPD pixel is explained. The SPICE simulation results prove that except reducing the crosstalk, dual-gate a-Si TFT can also significantly short the response time by cutting down the off-state current under the operation conditions of AMEPD application, while insignificantly reduces the on-state current.**

***Index Terms*—Active-matrix electrophoretic display (AMEPD), amorphous silicon thin-film transistor (a-Si:H TFT), common gate structure, dual-gate, response time.**

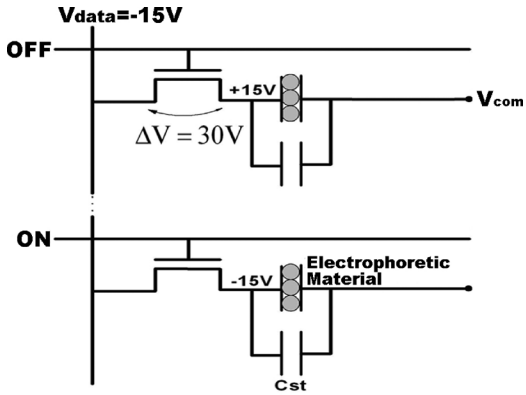

Fig. 1. Large drain–source voltage caused by common data line.

I. Introduction

As ONE OF the most promising electronic paper technologies, electrophoretic display still encounters several issues, one of which is the relatively long response time. Because of the proportional relationship between electrophoretic particle-moving velocity and applied voltage, the most convenient way to shorten the response time (i.e., particle's electrophoresis time from one electrode to the other) is to increase the voltage between the two electrodes. However, a large voltage is neither power saving nor compatible with the active-matrix display. Along with the improvements of electrophoretic materials and device structures, efforts were exerted to reduce the electrophoretic display (EPD) driving voltage from $\pm$100's or $\pm$10's volts [1], [2] in the early age to about $\pm$15 V today [3], [4] to meet the large scale display requirement, and the image update time has been controlled into the range of 10–100 ms [5], [6].

However, even when the driving voltage is down to $\pm$15 V, it is still relatively large. Consider two vertically arranged pixels with a common data line, as shown in Fig. 1. When the upper pixel is "off," holding a $+$15-V driving voltage, and the lower pixel is "on" while a $-$15-V data is being offered through the common data line, then the upper TFT would suffer a drain–source voltage as large as 30 V. Such a high voltage can cause an unbearable large off-state leakage current in the TFT, which will lead to severe crosstalk, and let the driving voltage decrease dramatically during the holding time. As mentioned above, since the particle-moving velocity is proportional to the applied voltage, such degradation would intensively increase the pixel's response time. In some reported EPDs, high frame rate (50 Hz) [6] is used. Thus, with a full image update cost of several frame cycles, the voltage degradation induced by large leakage current would be well compensated. However, in some other applications [7], slow or even occasional frame update is adopted to meet the requirements of ultralow power consumption or long lifetime backplane, where each pixel transistor operates only for one row time in each image update. For those applications, off-state leakage current becomes crucial for display response time.

In this paper, a $t - I_{\rm off}$ model is established to evaluate the leakage current's impact on the response time. In order to minimize $I_{\rm off}$ as much as possible, dual-gate a-Si TFT with a common gate structure is illustrated, and the current reduction mechanism is discussed. According to the analysis and SPICE simulations, this structure is proved to be effective and especially suitable for optimizing EPD's response feature by suppressing $I_{\rm off}$ without obvious on-state current $I_{\rm on}$ reduction.

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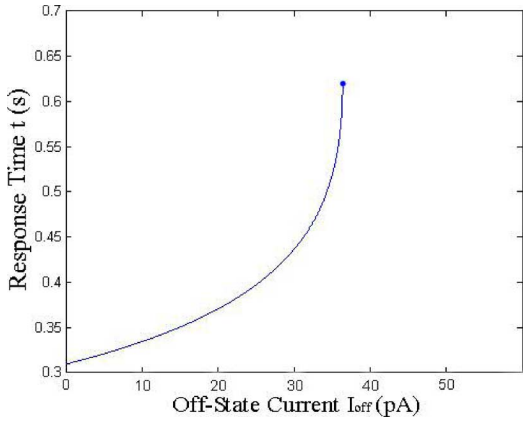

Fig. 2. Response time t as a function of off-state current $I_{\rm off}$.

II. Response Time Model

In order to evaluate the leakage current's impact on the response time, a compact mathematical model is necessary. We assume that: 1) $I_{\rm off}$ is constant and 2) each particle moves completely from one electrode to the other within the response time.

The voltage between the two electrodes is given by

$$U = U_0 - \frac{I_{\rm off} t}{C_{\rm st}}$$

where U_0 is the initial voltage, t is the response time, and $C_{\rm st}$ is the capacitance of the storage capacitor.

According to the STOKES equation, the particle velocity in the electrophoresis solvent can be written as

$$v = \frac{qU}{6\pi r\eta d} = \frac{q}{6\pi r\eta d}\left(U_0 - \frac{I_{\rm off} t}{C_{\rm st}}\right) \tag{1}$$

where q is the particle charge, r is the particle radius,η is the viscosity of the solvent, and d is the space between two electrodes. Within the response time, particles migrate from one electrode to the other, which could be expressed as

$$d = \int_0^t v dt. \tag{2}$$

By solving (2) with (1), the response time is given as

$$t = C_{\rm st} U_0 \frac{\left(1 - \sqrt{1 - \frac{2k}{U_0^2 C_{\rm st}} I_{\rm off}}\right)}{I_{\rm off}}, \qquad k = 6\pi r\eta d^2/q.$$

In order to numerically evaluate the $t - I_{\rm off}$ dependence, electrophoresis material parameters reported by Comiskey *et al.* [8] is adopted. The initial voltage is set to be 15 V, and a relatively large storage capacitor, $C_{\rm st} = 1.5$ pF, is used here. The simulation result is shown in Fig. 2.

One can conclude that: 1) an over-range $I_{\rm off}$ (> 37 pA) would lead to display failure, because the particles fail to reach the opposite electrode; 2) the larger $I_{\rm off}$, the more significant the response time reduction by suppressing $I_{\rm off}$; and 3) in the ideal situation where $I_{\rm off}$ is zero, a minimum response time $t_{\rm min}$ exists, which is related with the electrophoresis material parameters only.

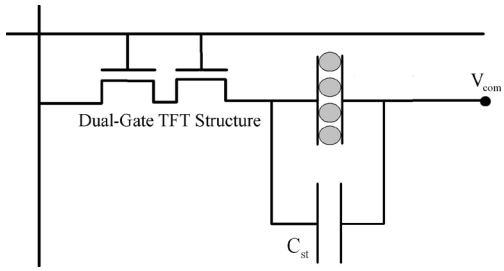

Fig. 3. Schematic dual-gate structure.

III. Dual-Gate A-Si TFT With a Common Gate

Because of its better off-state current performance comparing with polysilicon thin film transistor (p-Si TFT), a-Si TFT is chosen as the EPD pixel switch. However, because of different manufacturing conditions, sometimes a-Si TFTs may still fail to meet with the small off-state current requirement of EPD. Especially, as the most competitive electronic paper technology, EPD back panels are tried to be fabricated on various flexible plastic substrates, where the a-Si layer has to be formed under a low temperature typically at 150 °C, leading to a poor off-state current performance of the TFTs [9]. Thus, a technically simple amelioration of the a-Si TFT structure is expected for further off-state current reduction.

Dual-gate structure (Fig. 3) is a common practice in p-Si TFT technology to reduce the leakage current [10]. It could be simply considered as a series of connected TFTs sharing a common gate voltage. Leakage current reduction of over an order of magnitude in p-Si TFT had been achieved by this series-connected structure at an expense of some on-state current [11]. Dual-gate structures, used for a-Si TFTs, have been reported in EPDs applications [12], [13] for crosstalk control. This structure is exclusively meaningful for EPD, because, unlike most active-matrix devices (such as liquid crystal display) whose driving voltage is relatively low, EPDs encounter much higher $V_{\rm DS}$ (maximum 30 V). According to the SPICE simulation results shown in Fig. 4, one can see that if $V_{\rm DS}$ is in a low range, the leakage current can be ignored, and would not be significantly reduced by dual-gate structure, sometimes even higher than its single gate counterpart. This is because of the highly nonlinear device behavior of dual-gate structure. But the leakage current grows dramatically as the drain–source voltage rises, and the reduction effect is much more significant under a high $V_{\rm DS}$. Thus, dual-gate structure is very suitable for leakage current reduction of a-Si TFTs in EPDs driven by high voltages.

The dual-gate a-Si TFT can also be considered as two series-connected single a-Si TFTs. However, unlike simply adding a TFT to create the dual-gate structure as usual, here we discuss the structure by dividing the original TFT into two TFTs with equal channel length. While an added TFT will cause a half reduction in on-state current, the "dividing" method can keep it almost unchanged. This could be explained by considering the "ON" state TFTs as series-connected resistances. The "added"

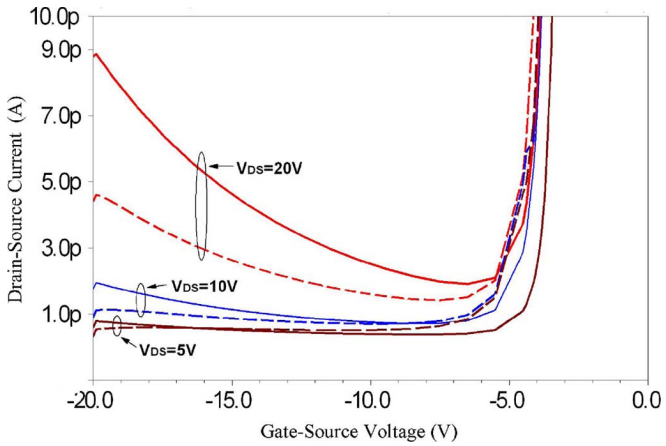

Fig. 4. Leakage currents of a dual-gate a-Si TFT (dashed lines) comparing with that of its single-gate a-Si TFT counterparts (solid lines) under different drain–source voltages.

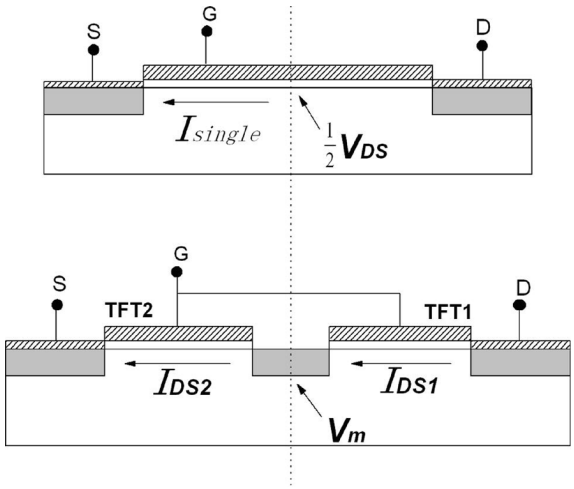

Fig. 5. Schematic dual-gate structure and its single-gate structure counterpart.

TFT would double the resistance, hence, cutting the on-current to a half, while the "divided" dual-gate structure with unchanged total channel length would not significantly affect it. However, both methods lead to the same off-state leakage, and the mechanisms could be analyzed very similarly. The mechanism of drain–source current $I_{\rm DS}$ behavior of dual-gate TFT can be explained according to the single TFT I–V characters and the $V_{\rm DS}$ distribution between them.

Consider a single gate TFT with a channel length L, and a dual-gate TFT with a channel length $l = (1/2)L$ of each sub-TFT, as shown in Fig. 5. Both of them are n-type and have the same $V_{\rm DS}$.

When the gate voltage V_G is positively biased, TFT works in the saturation region. The gate–source voltage of TFT1 and TFT2 are

$$V_{GS1} = V_G - V_m$$

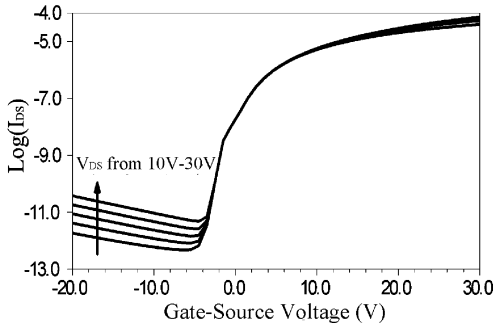

Fig. 6. $I-V$ curves of a single-gate a-Si TFT.

and $V_{GS2} = V_G$, respectively, where V_m is the middle point voltage between them. One can find

$$V_{GS1} < V_{GS2}.$$

In order to keep the current uniformity

$$I_{DS1} = I_{DS2}$$

where I_{DS1}, I_{DS2} are the drain–source currents in TFT1 and TFT2, respectively, the distribution of $V_{\rm DS}$ must meet

$$V_{DS1} > V_{DS2} \text{ and } V_{DS1} + V_{DS2} = V_{\rm DS}.$$

One can find

$$V_{DS2} < \frac{1}{2} V_{\rm DS}.$$

The left part of the single TFT can be considered as a single TFT with a channel length l, which has a drain–source voltage of $(1/2)V_{\rm DS}$, and a gate voltage of V_G. Comparing with TFT2, one can find

$$I_{DS2} = I_{\rm dual} < I_{\rm single},$$

where $I_{\rm dual}$ is dual-gate TFT current, and $I_{\rm single}$ is single gate TFT current.

Noticing that in the saturation region, the magnitude of current is almost independent of $V_{\rm DS}$, as shown in Fig. 6, $I_{\rm dual}$ should be just a little less than $I_{\rm single}$, which means the dual-gate structure seldom reduces the on-state current.

When the gate voltage is negatively biased, V_{GS1} is much more negative than V_{GS2}. Considering the current uniformity condition, we have

$$V_{DS1} < V_{DS2}, \quad V_{DS1} + V_{DS2} = V_{\rm DS}.$$

The middle point voltage can be written as

$$V_m = \frac{1}{2} V_{\rm DS} + \Delta V, \qquad \Delta V > 0.$$

Thus, comparing with the right part of the single gate TFT, the amplitude of V_{GS1} is ΔV larger, while V_{DS1} is ΔV smaller. For a-Si TFTs in the deep negatively biased region, $I_{\rm DS}$ increases appreciably as $V_{\rm GS}$ goes more negative, while decreases dramatically as $V_{\rm DS}$ decreases (as shown in Fig. 4). The result is

$$I_{DS1} = I_{\rm dual} \ll I_{\rm single}$$

which means the dual-gate TFT structure cuts down the off-state current effectively.

IV. SPICE Simulation Results

Using the AIM-SPICE and Level 15 a-Si TFT model, the current regulation effects of dual-gate structure in a-Si TFT is illustrated in Fig. 7. Considering the possible EPD driving situations, drain–source voltage of 15 and 30 V are simulated in the $V_{\rm DS} = -20 \sim 30$ V region. The device scales are $W/L = 80/5$ μm for the single-gate, and $W/L = 80/(2.5 + 2.5)$ μm for the dual-gate.

The simulation results firmly support the theoretical analysis. Dual-gate a-Si TFT cuts down about half of the leakage current [Fig. 7(b)], while keeps the on-state current basically unchanged [Fig. 7(c)]. In the EPD application, gate voltage could be set to ± 15 V, the same as driving voltage. When the drain–source voltage reaches to ± 30 V, the dual-gate structure would reduce the leakage current from 20 to 10 pA, largely improving the EPD response speed, as discussed below.

V. Discussion

For low frame rate EPDs with a frame time at the order of $\sim$ 100 ms, adapting the data from Fig. 2, which indicates a least response time of 300 ms, one can find the response time is the key factor to decide the display speed. In the worst case consideration, in which the first line of certain frame displays "white" (data voltage $=$ 15 V), while other lines display "black" (-15 V) in the rest of frame time, then during almost the whole frame time, the TFTs in the first line will suffer drain–source voltages as large as 30 V. According to SPICE simulation results, the leakage current under this condition is 20 pA, and the response time is 370 ms; If the dual-gate structure is adopted, the leakage current could be reduced to 10 pA, and the response time is shorted down to 320 ms.

In the practical devices, the leakage current may reach a higher level because of the various fabrication conditions, processes, device structures or driving voltages. For example, in the flexible substrate situation, low temperature a-Si TFTs may have much larger leakage currents. In these situations, the function of dual-gate structure is much more notable. For example, a 35-pA leakage current could be suppressed to about 18 pA, the response time would be shorted from 530 to 360 ms. If this EPD is designed to occupy only one frame refreshing per image update in order to ensure ultra low power consuming, long lifetime backplane or simple electronics, the fastest image refresh rate would be raised from about 2 to 3 Hz. In this design, the dual-gate structure also acts as over-ranged leakage current protector. As shown in Fig. 2, If the leakage current is too huge ($>$ 37 pA), the particles would fail to reach the counter electrode, and thus lead to display failure. However, with a dual-gate structure the over-ranged current can be drag back into the tolerable region, maintaining the display uniformity.

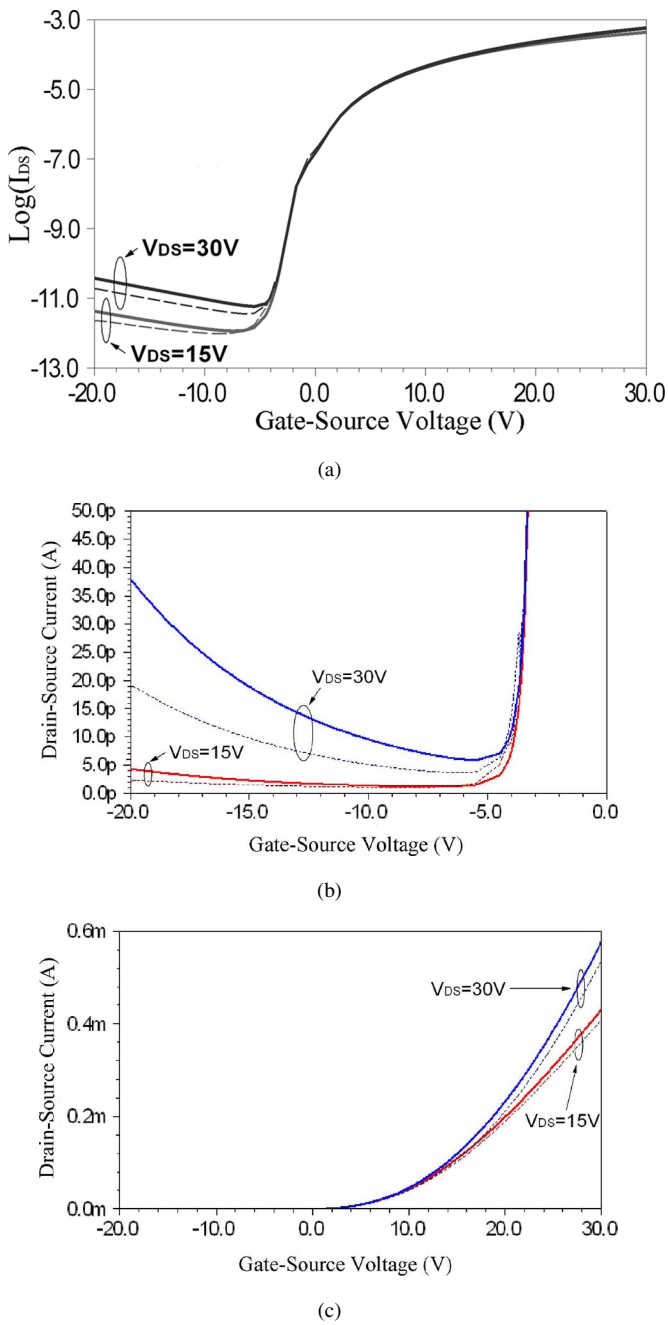

Fig. 7. (a) Simulated leakage currents in single-gate TFT (solid lines) and dual-gate TFT (dashed lines). (b) The off-state leakage currents under large drain–source voltages are dramatically shorted (c) The dual-gate structure insignificantly reduces the on-state leakages.

There are three items should be specified here. 1) $I_{\rm off}$ is not a constant in real device. It decreases as the drain–source voltage decreases, which will make the response time shorter. In a more accurate model, this change should not be ignored. 2) Although the particle's electrophoresis velocity is not completely linear with the electrode voltage because of the Van der Waals forces

between particles and electrodes, electric forces among particles, and so on [15], the STOKES equation is proper for the first-order approximation. 3) Other forms of leakage current are ignored in this model. In fact, the photo-current is believed to be rather small, because EPD is completely reflective display that does not have any backlight and the incidence lights would be well shielded by the front panel; as high resistance material, the front panel leakage of EPD is $\sim$ pA, which is ignorable comparing with drain–source leakage; And the gate–source bias stress induced leakage is considerably smaller than the drain–source leakage with good performance gate dielectrics. In practical designs, all the three leakages may be taken into account pending on different TFT layer and front panel material choices.

However, one should realize that reducing the leakage current's effect on response time by adopting dual-gate structure is only one of the many methods. It could also be achieved by other TFT structures, better device fabrications, enlarging storage capacitors, and high frame rate compensations. One should also realize that the long response time is actually an intrinsic characteristic of electrophoretic materials. The ultimate solution towards high-rate display lies in the material optimization. Our simulations indicate that the best way is to dramatically reduce the particle radius.

VI. Conclusion

The off-state drain–source leakage current is a big issue in the AMEPD application because of its large driving voltage. The leakage current may lead to severe crosstalk. In addition, it may also cause undesired long response time, even display failure. A compact $t - I_{\text{off}}$ model is established in this paper to evaluate the impact of leakage current on the display performance. The model indicates that the response time can be shorted dramatically by reducing the leakage current.

In order to achieve a small leakage current, dual-gate a-Si TFT with a common gate is adopted and analyzed. The dual-gate structure can be considered as two series-connected TFTs. Because of the nonlinear I–V behavior of TFT and the voltage distribution mechanism, off-state leakage current can be effectively reduced without significant on-state current loss. According to the SPICE simulation results, dual-gate a-Si TFT is very suitable for reducing the leakage current under the AMEPD's relatively high driving voltage. It dramatically shorts the response time and keeps the display uniformity by regulating the over-ranged leakage current. This structure is especially useful for flexible and very low frame rate EPDs, where huge off-state current may appear, and the image update rate largely depends on the response time. The simulation results also indicate that the long response time would be basically solved by electrophoretic material optimization.

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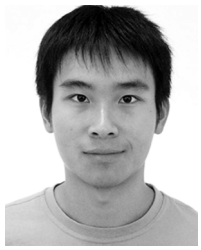

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