Predicting Method of Leakage Current in Multiple-Gate Amorphous Silicon TFTs for Active-Matrix Electrophoretic Displays

Shu Yang and Hai Jing

***Abstract*—The large off-state drain–source leakage current of the thin-film transistor (TFT) in active-matrix electrophoretic display (AMEPD) may cause severe crosstalk and long pixel refresh time. Multiple-gate amorphous silicon TFT (a-Si TFT) is a common use to overcome this issue. In this paper, we show that the leakage current of multiple-gate a-Si TFT can be computed from the I–V characteristics of a single TFT by an analytical current model. The predicted leakage currents show good agreement with the expected values in SPICE simulation. This model is also applicable for the multiple-gate a-Si TFTs used in other high voltage driven devices.**

***Index Terms*—Active-matrix electrophoretic display (AMEPD), amorphous silicon thin-film transistor (a-Si TFT), leakage current, multiple-gate.**

I. Introduction

Electrophoretic display (EPD) is one of the most promising flexible display technologies and has attracted much attention recently. However, the intrinsic physical properties of the electrophoresis material have defined a rather high pixel driving voltage in active-matrix electrophoretic display (AMEPD), which may lead to undesired large thin-film transistor (TFT) off-state leakage current, and hence causes severe crosstalk and long pixel response time. In some EPD prototypes toward commercial use, several approaches have been adopted to overcome this issue. For example, high refresh rate is employed to compensate for the fast voltage degradation [1]; and the size of storage capacitor is greatly enlarged to ensure the stability of driving voltage during one frame time [2]. However, both methods will compromise EPD's major benefits of ultra low power consumption and possible low cost. Therefore, the multiple-gate structure, which is a common use in polysilicon TFTs (p-Si TFTs) in active-matrix liquid crystal display (AMLCD) technology for leakage current control [3], [4], is applied to a-Si TFTs for AMEPD driving [2], [5]. Although the leakage current computing method for multiple-gate p-Si TFTs in AMLCD has already been proposed by *Sturm et al.* [6], there is no proper counterpart for a-Si TFTs till now.

The purpose of this paper is to show that the leakage currents of the multiple-gate a-Si TFTs can be calculated by a precise current model derived form the I–V curves of a single TFT. According to our SPICE simulation, this method is proved to be of good accuracy for at least 5-gate a-Si TFT under the AMEPD's driving conditions. This method is also applicable for the multiple-gate a-Si TFTs used in other high voltage driven devices.

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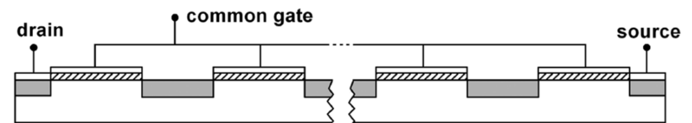


Fig. 1. Multiple-gate TFT.

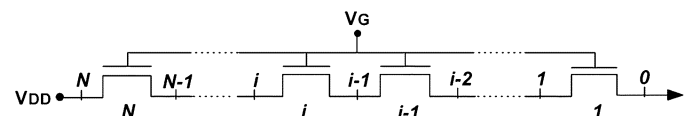


Fig. 2. Schematic diagram of N-gate TFT.

II. Current Model and Calculating Method

The multiple-gate TFT, as shown in Fig. 1, can be considered as arbitrary number of transistors placed in series and connected to a common gate (see Fig. 2). When the drain bias is applied, the TFTs will obtain different source voltages but share the same gate bias. Therefore, because the drain currents must be equal, the total drain–source voltage has to re-distribute itself between the cascade transistors. Based on this analysis, *Sturm et al.*. have presented a quick computing method to predict the leakage currents in the multiple-gate p-Si TFTs.

In this method, for sufficiently negative gate voltages, the drain current I_D is assumed to be exponentially dependent on both drain–source voltage $V_{\rm DS}$ and gate–source voltage $V_{\rm GS}$, written as

$$I_D = Ce^{aV_{\rm DS} - bV_{\rm GS}} \tag{1}$$

where C is an arbitrary constant, and parameters a and b can be directly extracted from the I–V curves of a single TFT. Applying the currents uniformity condition, the fraction of the total drain voltage dropped over the lowest transistor can be written as

$$\frac{V_{D,1}}{V_{\rm DD}} = \frac{a^{N-1}b}{a^N - (a-b)^N} \tag{2}$$

where N is the number of gates and $V_{D,1}$ is the drain–source voltage of the lowest transistor. Since the I–V curves of a single TFT is already known, for a given gate bias V_G, now one can

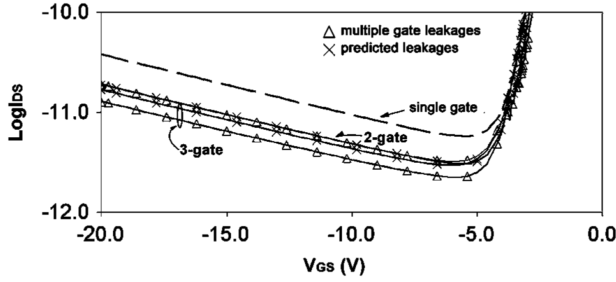


Fig. 3. Leakages in 2- and 3-gate TFTs comparing with the predicted values by the linear model.

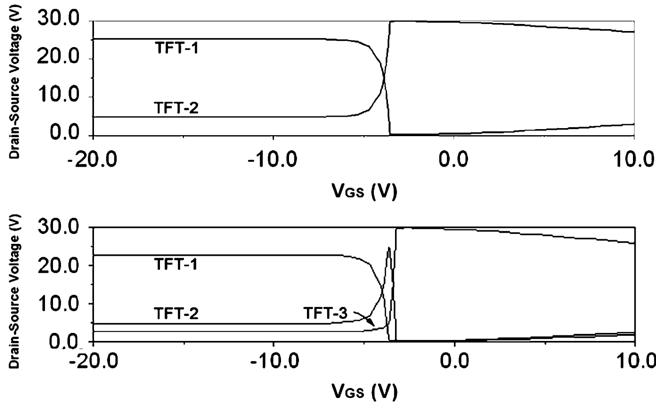


Fig. 4. Drain–source voltages of each cascade transistor in 2-gate (above) and 3-gate (below) structures.

easily get the drain current of the lowest transistor, which is also the current of the N-gate TFT. This computing method is reported to be effective for 3- or 4-gate p-Si TFTs while $V_{\rm DS}$ is in the range of 10–20 V.

However, this model is not suitable for multiple-gate a-Si TFTs. The SPICE simulation (AIM-SPICE Version 5.0; in this paper, the width/length ratios of the single and cascade transistors are 80 μm/5 μm) shows that, it will fail when the number of gates is higher than two, with obviously larger predicted leakages than expected (see Fig. 3). This failure can be explained by an investigation of the drain–source voltage of each cascade transistor in the multiple-gate structure.

In SPICE simulation, $V_{\rm DD}$ is set to 30 V as the huge leakage current appears in AMEPDs. The drain–source voltage of each cascade transistor (labeled as TFT-n, $n = 1, 2, 3$) in 2-gate and 3-gate structures are plotted in Fig. 4. One can see the lowest $V_{\rm DS}$ of each cascade transistor is about 5 V in the 2-gate structure, but less than 3 V when the number of gates grows to 3. From the $\log I_{\rm DS}$–$V_{\rm DS}$ curves of a single a-Si TFT (Fig. 5) it can be concluded that, if $V_{\rm DS}$ is too small (< 5 V), $\log I_{\rm DS}$ will degrade dramatically as $V_{\rm DS}$ goes smaller. As a result, this current model, which is based on the assumption that $\log I_{\rm DS}$ is linearly dependent on both $V_{\rm DS}$ and $V_{\rm GS}$, will be invalid when the number of gates is higher than 2, and leads to obviously larger predicted currents than expected, but still applicable for the 2-gate structure. Note that the physical foundation of the "linear model" is the field-enhanced generation by virtue of the *Poole–Frenkel* effect. In p-Si TFTs, this conduction mechanism dominates in most part of the leakage regime [7], hence makes the linear model applicable in a very wide range of $V_{\rm GS}$; Whereas in a-Si TFTs, until the high field condition is acquired, the back channel conduction induced by the electrons accumulated at the silicon/insulator back interface works as the major leakage path [8]. Leakages in this regime are much smaller than that caused by the field-enhanced generation. That is why a dramatic $\log I_{\rm DS}$ degradation is observed when $V_{\rm DS}$ goes below 5 V, and hence causes the failure of the "linear model" in a-Si TFTs.

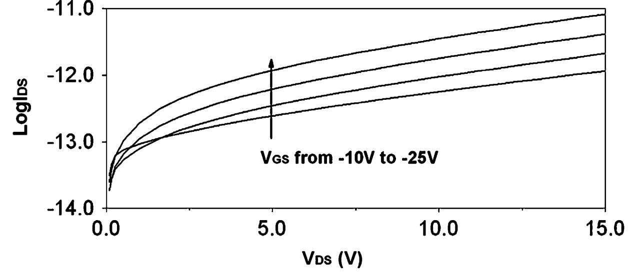


Fig. 5. $\log I_{\rm DS}$–$V_{\rm DS}$curves of a single transistor ($W/L = 80/5$).

Now a modified current model involving the back channel conduction regime is required to meet the appearance of low $V_{\rm DS}$ on the highest transistor in multiple gate structure. The shape of the $\log I_{\rm DS}$–$V_{\rm DS}$ curves indicates that $\log I_{\rm DS}$ may be considered as linearly dependent on $\sqrt{V_{\rm DS}}$. Hence we assume

$$I_{\rm DS} = C \cdot 10^{a\sqrt{V_{\rm DS}} - bV_{\rm GS}} \tag{3}$$

where C is a constant, parameters a and b can be extracted from the I–V curves of an individual TFT.

Using the currents uniformity condition, written as

$$I_{\rm DS}^{i} = I_{\rm DS}^{i-1} \tag{4}$$

where $I_{\rm DS}^{i}$ is the drain current of the *No.i* cascade transistor (TFT-i), we have

$$\begin{aligned} &a\sqrt{V_i^{(N)} - V_{i-1}^{(N)}} - b\left[V_G - V_{i-1}^{(N)}\right] \\ &\quad = a\sqrt{V_{i-1}^{(N)} - V_{i-2}^{(N)}} - b\left[V_G - V_{i-2}^{(N)}\right], \qquad i = 2 \sim N \end{aligned} \tag{5}$$

where $V_i^{(N)}$ refers to the voltage on *node i* in the N-gate structure. One can solve the recursive equations to yield

$$a\left[\sqrt{V_i^{(N)} - V_{i-1}^{(N)}} - \sqrt{V_1^{(N)}}\right] + bV_{i-1}^{(N)} = 0. \tag{6}$$

To make (6) calculable, one more condition is needed. Hence we plot the drain–source voltages of the second and the third cascade transistors when the number of gates varies from 2 to 5, as shown in Fig. 6. Here $V_{\rm DD}$ is set to 15 V for a better view of the tendency. It is easy to find that $V_{\rm DS}$ of each intermediate cascade seems almost unchanged as the number of gates varies. This phenomenon can be explained as followed:

Assuming another transistor is added to the drain terminal of the multiple-gate structure as the highest cascade, V_1 (the voltage on *node 1*, as shown in Fig. 2) will decrease as $V_{\rm DD}$

TABLE. I
DRAIN–SOURCE VOLTAGES OF THE FIRST TRANSISTOR WITH INCREASING NUMBER OF GATES

Number of Gates	2	3	4	5
$V_1^{(N)}$ (V)	25.3	22.6	20.7	19.4

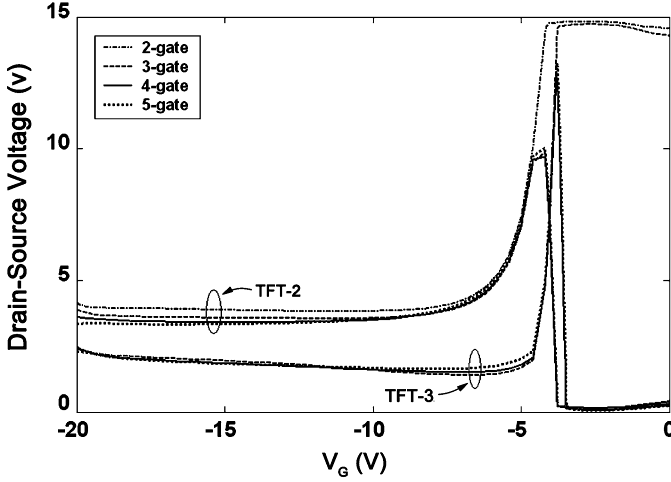


Fig. 6. Drain–source voltages on the second and the third cascaded transistors in different multiple-gate structures.

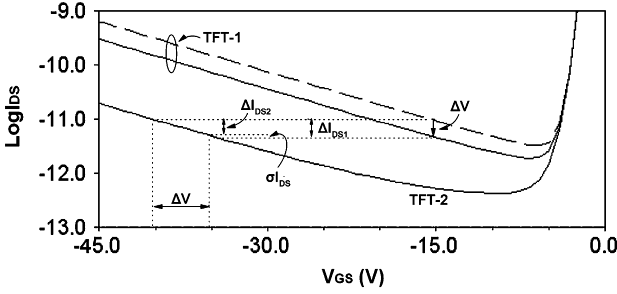


Fig. 7. Schematic diagram of $\sigma I_{\rm DS}$.

re-divides itself to meet the currents uniformity condition. In the reversed bias region, the decrease of V_1 will cause a reduction (labeled as ΔV) in $V_{\rm DS1}$ (drain–source voltage of TFT-1) and a quantitatively equal reduction in negative $V_{\rm GS2}$ (the gate–source voltage of TFT-2), both of which will lead to a drop of $I_{\rm DS}$ (labeled as $\Delta I_{\rm DS1}$ and $\Delta I_{\rm DS2}$, respectively). Because $I_{\rm DS}$ has a relatively weaker dependence on $V_{\rm GS}$ comparing with $V_{\rm DS}$, a differential value $\sigma I_{\rm DS}$ exists between $\Delta I_{\rm DS1}$ *and* $\Delta I_{\rm DS2}$. Now, since $V_{\rm GS1}$ is a constant, the only way to keep the currents uniformity of the two transistors is to reduce $V_{\rm DS2}$. However, because the differential value $\sigma I_{\rm DS}$ is not significant in a-Si TFTs (as shown in Fig. 7), only a very small decrease of $V_{\rm DS2}$ is expected to accommodate for it. Therefore, $V_{\rm DS2}$ can be considered as constant as the number of gates changes. Further, since $V_{\rm DS2}$ is a constant, and thus *node 1* and *node 2* have the same variations in voltage, $V_{\rm DS3}$ can also be considered as constant. Situations in other cascades except the highest can be analyzed similarly. Finally, it is reasonable to assume that, when the number of gates changes in multiple-gate a-Si TFT, the drain–source voltages of the intermediate cascade transistors will not be affected, which means the total voltage re-dividing happens only between the lowest and the highest transistors. Polysilicon TFTs do not have this property simply because their drain currents are much more sensitive to $V_{\rm DS}$ rather than $V_{\rm GS}$.

With this assumption, the drain–source voltage of TFT-N, labeled as $V_{{\rm DS},N}^{(N)}$, can be expressed as the difference of the voltages on *node 1* in N-gate and $(N-1)$-gate TFTs as

$$V_{{\rm DS},N}^{(N)} = V_1^{(N-1)} - V_1^{(N)}. \tag{7}$$

The voltage on *node* $(N-1)$ can be written as

$$V_{N-1}^{(N)} = V_1^{(N)} + V_{\rm DS,2}^{(N)} + V_{\rm DS,3}^{(N)} + \cdots + V_{{\rm DS},N-1}^{(N)} \tag{8}$$

where $V_{{\rm DS},n}^{(N)} (n = 2 - N - 1)$ refers to the drain–source voltage of TFT-n.

Applying the boundary condition $V_1^{(1)} = V_{\rm DD}$, (7) and (8) reduce to

$$V_{i-1}^{(N)} = V_1^{(N)} + V_{\rm DD} - V_1^{(N-1)}. \tag{9}$$

Substituting (9) into (6), one can find the relationship between the drain–source voltages of the lowest transistors in N-gate and $(N-1)$-gate structures as

$$a\left[\sqrt{V_1^{(N-1)} - V_1^{(N)}} - \sqrt{V_1^{(N)}}\right] + b\left[V_{\rm DD} - V_1^{(N-1)} + V_1^{(N)}\right] = 0, \qquad N \geq 2. \tag{10}$$

Solving the equations with the boundary condition $V_1^{(1)} = V_{\rm DD}$, all $V_1^{(N)}$ can be calculated one by one. Since the I-V characteristics of a single a-Si TFT is known, one can easily calculate the leakage current for a given drain–source voltage $V_1^{(N)}$ and a gate–source voltage V_G, which is exactly the leakage current in N-gate a-Si TFT with a total drain–source voltage $V_{\rm DD}$.

III. SIMULATION AND DISCUSSION

Parameters a and b are extracted from the I–V curves of an individual transistor with $\mathrm{width/length} = 80\ \mu$m/5 μm. Considering the situation when large leakage current appears in AMEPD, $a = 0.53$ is extracted as $\sqrt{V_{\rm DS}}$ ranges from $1V^{1/2}$ to $5V^{1/2}$; and $b = 0.06$ is extracted when $V_{\rm GS} < -15$ V. $V_1^{(N)} (N = 1 - 5)$ are computed and listed in Table I. In the SPICE simulation, good agreements between multiple-gate leakages and the predicted results are obtained, as shown in Fig. 8. Simulations for more than 5-gate structures are not given in this paper considering the practical applications. However,

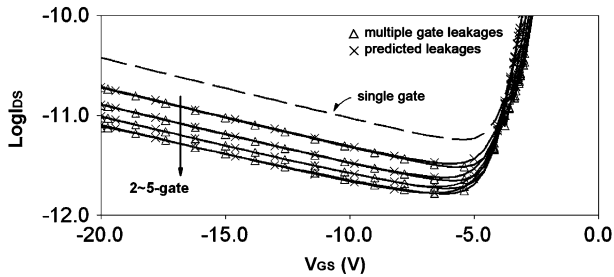


Fig. 8. Predicting results in different multiple-gate structures.

it is believed that this model is also effective even when the number of gates is larger.

In this paper, the multiple-gate is constructed by placing single-gate transistors in series. Noticing that in the highly reversed regime, the field enhanced emission acts as the major conducting mechanism, the leakage currents will not be influenced by the channel width/length ratio. Therefore, this predicting method is also valid in the situation where the multiple-gate is formed by evenly "dividing" the original single TFT into sub-TFTs, as illustrated in our previous work [9].

However, one should keep it in mind that this calculating method is only suitable for high field case (high $V_{\rm DD}$ and high negative V_G). For example, using the parameters a and b illustrated above, if $V_{\rm DS}$ is reduced down to 15 V in the 3-gate structure, a predicting error of $\sim$13% will occur at $V_G=-15$, which will grow dramatically to $\sim$19% as V_G goes down further to -10 V. Therefore, if this calculating method is applied to other a-Si TFT devices, high field condition should be firstly satisfied with, and the parameters a and b should be extracted from the corresponding voltage regimes.

IV. Conclusion

The large off-state TFT drain–source leakage current caused by high driving voltage is a critical issue in active matrix electrophoretic displays. Multiple-gate a-Si TFT is one of the common approaches to suppress the leakage without compromising EPDs' most important benefits of ultra low power consuming and low cost. In this paper, we show that the leakage currents in the multiple-gate a-Si TFTs for AMEPD driving can be precisely calculated from an analytical current model based on the I-V characteristics of a single TFT. The drain–source voltages of the intermediate transistors are assumed to be constants in our current model when the number of gates varies, whose causing mechanism is graphically illustrated. The predicted and expected leakages show good agreement for at least 5-gate structure in SPICE simulation. This method is also applicable for the multiple-gate a-Si TFTs used in other high voltage driven devices.

References

[1] G. H. Gelinck, H. E. A. Huitema, M. van Mil, E. van Veenendaal, P. J. G. van Lieshout, and F. J. Touwslager, "Rollable QVGA active-matrix display based on organic electronics," in *SID'05 Dig.*, vol. 36, no. 1, pp. 6–9.

[2] A. Henzen, J. van de Kamer, T. Nakamura, T. Tsuji, M. Yasui, M. Pitt, G. Duthaler, K. Amundson, H. Gates, and R. Zehner, "Development of active matrix electronic ink displays for handheld devices," in *SID'03 Dig.*, vol. 34, no. 1, pp. 176–179.

[3] Y. Matueda, M. Ashizawa, S. Aruga, H. Ohshima, and S. Morozumi, "New technologies for compact TFT LCDs with high-aperture ratio," in *Soc. Inf. Display Dig.*, 1990, pp. 315–318.

[4] I.-W. Wu, "High-definition displays and technology trends in TFT LED's," *J. Soc. Inf. Display*, vol. 2, no. 1, pp. 1–14, 1994.

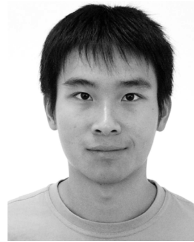
[5] S. Paek, K. L. Kim, H. S. Seo, Y. S. Jeong, S. Y. Yi, S. Y. Lee, N. B. Choi, S. H. Kim, C. D. Kim, and I. J. Chung,, "10.1 inch SVGA Ultra thin and flexible active matrix electrophoretic display," in *SID'06 Symp. Dig. Tech. Papers*, vol. 37, no. 2, pp. 1834–1837.

[6] J. C. Sturm, I.-W. Wu, and M. Hack, "Leakage current modeling of series-connected thin film transistors," *IEEE Trans. Electron Devices*, vol. 42, no. 8, pp. 1561–1563, Aug. 1995.

[7] S. K. Madan and D. A. Antoniadis, "Leakage current mechanisms in hydrogen-passivated fine-grain polycrystalline silicon on insulator MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-33, no. 10, pp. 1518–1528, Oct. 1986.

[8] P. Servati and A. Nathan, "Modeling of the reverse characteristics of a-Si:H TFTs," *IEEE Trans. Electron Devices*, vol. 49, no. 5, pp. 812–819, May 2002.

[9] S. Yang and H. Jing, "Simulation of active matrix electrophoretic display response time optimazation by dual-gate a-Si TFT with common gate structure," *J. Display Technol.*, vol. 4, no. 2, Jun. 2008.



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