

Optoelectronic butterfly interconnection architecture of modified signed-digit arithmetic systems: fully parallel adder and subtracter

De-Gui Sun, Li-Ming He, Na-Xin Wang, and Zhao-Heng Weng

The carry-free property of modified signed-digit addition is discussed, and a space-position–logic-encoding scheme is proposed, which not only makes best use of the convenience of binary (0, 1) logic operation but is also suitable for the trinary (1, 0, $\bar{1}$) property of modified signed-digit digits. Based on the space-position–logic-encoding scheme, a fully parallel modified signed-digit adder and subtracter is built by use of optoelectronic switch modules and butterfly interconnections; thus an effective combination of a parallel algorithm and a parallel architecture is implemented. The effectiveness of this architecture is verified by both simulation and experimental results.

Key words: Butterfly interconnection, space position–logic encoding, fully parallel modified signed-digit adder and subtracter.

1. Introduction

There are two options to develop parallel digital optical computing systems: one is to research the carry-free parallel algorithm, the other is to research the optical implementing architecture. Of course, the best selection is an effective combination of these two options. In algorithm research, binary, residue, and modified signed-digit (MSD) algorithms have been researched as possible selections, but they all have their own advantages and limitations.^{1–7} In digital optical computing, the main optical interconnections include butterfly,^{2,3,8,9} crossover,¹⁰ and perfect shuffle,¹¹ which can be implemented with fiber interconnection technology as well as free-space optical interconnections such as grating interconnections. Among the optical interconnections, the butterfly has been demonstrated to be the most regular and the easiest to implement by parallel optical approaches.^{2,3,12} In our previous research we have proposed the butterfly interconnection systems for

optical parallel addition and subtraction based on the binary algorithm. However, because of the carry of the binary algorithm, these parallel structures are really partially parallel systems; i.e., their computing speed is still dependent on the number of operand bits. Thus fully parallel computing systems require parallelism in both the algorithm and the architecture, and they require effective combination of the parallel algorithm and the parallel architecture, which requires an effective encoding scheme.

The MSD algorithm is an effective carry-free algorithm, and symbolic substitution is an optical parallel implementing approach; thus an optical MSD parallel computing system based on symbolic substitution is a typical example of a combination of a parallel algorithm and a parallel implementing approach.^{6,7,13–15} However, in the parallel optical computing systems, in terms of the proposed optical pattern encoding and optical polarization encoding for symbolic substitution, the space size taken by each operand bit cannot be made very small, which limits the miniaturization and integration of MSD computing systems. In addition, both substitution rules and optical approaches for implementing the rules are generally difficult, which limits the further development of multibit parallel MSD optical computing systems. The purpose of this paper is to discuss the implementation of fully parallel optical addition and subtraction based on the effective combination of the MSD algorithm and the butterfly interconnection architecture by use of a space-position–logic-encoding (SPLE)

D.-G. Sun, N.-X. Wang, and Z.-H. Weng are with the Changchun Institute of Optics and Fine Mechanics, Academia Sinica, State Laboratory of Applied Optics, P.O. Box 1024, Changchun 130022, China. L.-M. He is with the Department of Electronic Engineering, Jilin University of Technology, Changchun 130025, China.

Received 16 April 1993; revised manuscript received 14 January 1994.

0003-6935/94/296755-07\$06.00/0.

© 1994 Optical Society of America.

T			
1	1	1	0
0	1	0	$\bar{1}$
$\bar{1}$	0	$\bar{1}$	$\bar{1}$
	1	0	$\bar{1}$

W			
1	0	$\bar{1}$	0
0	$\bar{1}$	0	1
$\bar{1}$	0	1	0
	1	0	$\bar{1}$

Fig. 1. Truth tables of the first-step operation of MSD addition: (a) for transfer T , (b) for weight W .

scheme, which exploits both the carry-free property of the MSD algorithm and the convenience of binary logic operation with optoelectronic logic technology. In Section 2 the advantages of the MSD algorithm are discussed. In Section 3 a SPLE scheme is proposed and studied, and the truth tables of MSD addition based on the SPLE are given and discussed. On this basis the butterfly interconnection architecture of the MSD adder and subtracter is studied in detail, and its effectiveness is verified by both the simulation results and the experimental results in Section 4. Finally, in Section 5 a summary and conclusions are given.

2. Advantages of the Modified Signed-Digit Algorithm

In this section we briefly review the key concepts of the MSD addition and subtraction and demonstrate the carry-free property of MSD addition. A more detailed discussion may be found in Refs. 6, 7, and 13–15. A MSD number is a special state of a signed digit. For example, when the radix is 2, the MSD number D_{MSD} can be written as

$$D_{MSD} = [1, 0, \bar{1}], \quad (1)$$

where $\bar{1}$ represents -1 . Then each decimal number can be represented in the MSD number system by the coefficients of the polynomial:

$$D_{10} = [1, 0, \bar{1}]2^{n-1} + \dots + [1, 0, \bar{1}]2^i + \dots + [1, 0, \bar{1}]2^0. \quad (2)$$

For two MSD numbers, $X_{MSD} (=X_{n-1}, \dots, X_i, \dots, X_0)$ and $Y_{MSD} (=Y_{n-1}, \dots, Y_i, \dots, Y_0)$, the addition can be performed through a three-step operation. At the first step, $X_i + Y_i = 2T_{i+1} + W_i$ is performed at the i th digit for $i = 0, 1, \dots, n - 1$, where W_i and T_{i+1} are called the weight digit and the transfer digit, respec-

T'			
1	1	0	0
0	0	0	0
$\bar{1}$	0	0	$\bar{1}$
	1	0	$\bar{1}$

W'			
1	0	1	0
0	1	0	$\bar{1}$
$\bar{1}$	0	$\bar{1}$	0
	1	0	$\bar{1}$

Fig. 2. Truth tables of the second-step operation of MSD addition: (a) for transfer T' , (b) for weight W' .

S (=T)			
1	1	1	0
0	1	0	$\bar{1}$
$\bar{1}$	0	$\bar{1}$	$\bar{1}$
	1	0	$\bar{1}$

Fig. 3. Truth tables of the third-step operation of MSD addition for producing the final sum S .

tively. These digits assume the values

$$W_i = \begin{cases} 1 & \text{for } X_i + Y_i = \bar{1} \\ 0 & \text{for } |X_i + Y_i| \neq 1, \\ \bar{1} & \text{for } X_i + Y_i = 1 \end{cases}$$

$$T_{i+1} = \begin{cases} 1 & \text{for } X_i + Y_i \geq 1 \\ 0 & \text{for } X_i + Y_i = 0 \\ \bar{1} & \text{for } X_i + Y_i \leq \bar{1} \end{cases} \quad (3)$$

At the second step, $W_i + T_i = 2T'_{i+1} + W'_i$ is performed to produce another pair of weight and transfer digits W'_i and T'_{i+1} :

$$W'_i = \begin{cases} 1 & \text{for } W_i + T_i = 1 \\ 0 & \text{for } |W_i + T_i| \neq 1, \\ \bar{1} & \text{for } W_i + T_i = \bar{1} \end{cases}$$

$$T'_{i+1} = \begin{cases} 1 & \text{for } W_i + T_i = 2 \\ 0 & \text{for } |W_i + T_i| \neq 2 \\ \bar{1} & \text{for } W_i + T_i = -2 \end{cases} \quad (4)$$

The third step generates the final sum digit S_i :

$$S_i = W'_i + T'_i = \begin{cases} 1 & \text{for } W'_i + T'_i \geq 1 \\ 0 & \text{for } W'_i + T'_i = 0 \\ \bar{1} & \text{for } W'_i + T'_i \leq \bar{1} \end{cases} \quad (5)$$

To demonstrate the carry-free property of MSD addition, we perform the derivation as follows. In terms of the third step and Eq. (5) it can be noted that

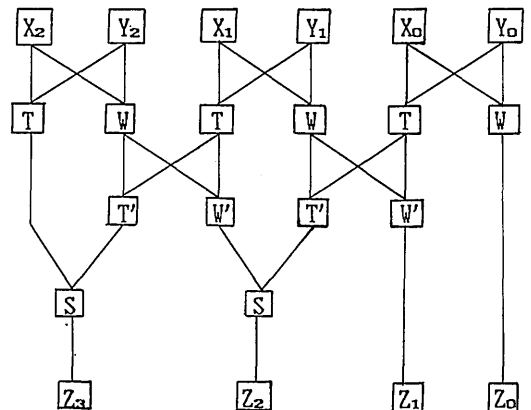


Fig. 4. Butterfly interconnection architecture for implementing the three step operations of MSD addition of two 3-bit digits.

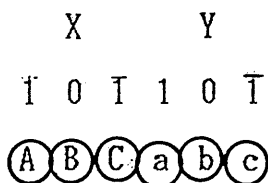


Fig. 5. Space-position-logic-encoding (SPLE) scheme in which three space position codes, A, B, and C (or a, b, and c), stand for 1, 0, and $\bar{1}$, respectively.

the sum S_i is a function of only W'_1 and T'_i :

$$S_i = f(W'_i, T'_i). \quad (6)$$

In terms of the second step we can obtain

$$W_{i-1} + T_{i-1} = 2T'_i + W'_{i-1}. \quad (7)$$

In terms of the second step and Eq. (4), W'_i is a function of only W_i and T_i ; in terms of Eq. (7), T'_i is a function of only W_{i-1} and T_{i-1} ; then according to Eq. (6), we have

$$S_i = f(W_i, T_i; W_{i-1}, T_{i-1}). \quad (8)$$

In terms of the first step we have

$$X_{i-1} + Y_{i-1} = 2T_i + W_{i-1}, \quad (9a)$$

$$X_{i-2} + Y_{i-2} = 2T_{i-1} + W_{i-2}. \quad (9b)$$

Then according to Eq. (3), W_i is a function of only X_i and Y_i ; according to Eq. (9a), both T_i and W_{i-1} are the functions of X_{i-1} and Y_{i-1} ; according to Eq. (9b), T_{i-1} is a function of only X_{i-2} and Y_{i-2} . Thus according to Eq. (8), we have

$$S_i = f(X_i, Y_i; X_{i-1}, Y_{i-1}; X_{i-2}, Y_{i-2}). \quad (10)$$

Namely, the sum at the i th bit S_i is related only to the operand bits of the i th bit, the $(i-1)$ th bit, and the $(i-2)$ th bit, and the carriers are limited within these three operand bits.

In terms of Eqs. (3), (4), and (5) we can obtain the truth tables for the three step operations of MSD addition as shown in Figs. 1, 2, and 3, respectively. In terms of the three step operations of MSD addition, the MSD addition of two 3-bit digits can be depicted in the butterfly interconnection architecture as shown in Fig. 4, where $X (= X_2X_1X_0)$ and Y

	T			W			
a	a	a	b	a	B	C	B
b	a	b	c	b	C	B	A
c	b	c	c	c	B	A	B
	A	B	C		A	B	C
	(a)			(b)			

Fig. 6. Truth tables of the first-step operation of MSD addition represented by the SPLE scheme: (a) for transfer T , (b) for weight W .

	T'			W'			
a	a	b	b	a	B	A	B
b	b	b	b	b	A	B	C
c	b	b	c	c	B	C	B
	A	B	C		A	B	C
	(a)			(b)			

Fig. 7. Truth tables of the second-step operation of MSD addition represented by the SPLE scheme: (a) for transfer T' , (b) for weight W' .

($= Y_2Y_1Y_0$) are augend and addend, respectively, and $Z (= Z_3Z_2Z_1Z_0)$ is the final addition result.

3. Space-Position-Logic-Encoding Scheme

As described above, the MSD algorithm is different from the binary algorithm in form. The binary algorithm has only the two digits of 0 and 1; thus in an electronic computer the higher and the lower voltages are represented by 1 and 0, respectively, which is a successful encoding scheme. In the same manner, in optical computing the higher and the lower light powers or a light signal and a nonlight signal generally are represented by 1 and 0, respectively.¹⁶⁻¹⁸ At the same time, because of optical properties and the symbolic substitution theorem, pattern encoding, polarization encoding,^{7,13,14,19} and other encoding schemes^{20,21} occur successively. The MSD algorithm is emphasized since has been proposed as an important algorithm,⁶ and both pattern encoding and polarization encoding are selected and studied for implementing MSD systems.²² These two encoding schemes have their own limitations in implementing multibit calculations. In this section we propose a SPLE scheme as shown in Fig. 5, in which three different space positions, A, B, and C (or a, b, and c), are used to represent 1, 0, and $\bar{1}$ of MSD digits in which three light-emitting diodes (LED's) or laser diodes (LD's) are placed at A, B, and C (or a, b, and c), respectively. Thus these three LED's or LD's at A, B, and C (or a, b, and c) represent only one MSD bit; namely, only one LED or LD has a light signal, and a light signal at a different position of the i th bit represents a different value. For example, the light signal of the LED or the LD at position A of the X_i bit represents $X_i = 1$, and at the same time, the LED's or the LD's at positions B and C of the X_i bit have no light signals; the light signal of the LED or the LD at position B of X_i bit represents $X_i = 0$, and at the same time, the LED's or the LD's at positions A and C of the X_i bit have no light signals; the light signal of the LED or the LD at position C of X_i bit represents $X_i =$

	S (=T)		
a	a	a	b
b	a	b	c
c	b	c	c
	A	B	C

Fig. 8. Truth tables of the third-step operation of MSD addition represented by the SPLE scheme for the final sum S .

a	G_1	G_2	G_3
b	G_4	G_5	G_6
c	G_7	G_8	G_9
	A	B	C

Fig. 9. Unitary detecting array to stand for all the truth tables of MSD addition, where G_1, G_2, \dots, G_9 are nine detecting elements.

$\bar{1}$, and at the same time, the LED's or the LD's at positions A and B of the X_i bit have no light signals. Thus each space position has two states, either having a light signal or having no light signal, which is similar to the logic operations of the binary algorithm. Therefore we call the encoding scheme a space-position-logic-encoding (SPLE) scheme. Then with the SPLE scheme the truth tables for the three operations of MSD additions as shown in Figs. 1, 2, and 3 become the new forms as shown in Figs. 6, 7, and 8, respectively. In terms of the truth tables as shown in Figs. 6, 7, and 8, any table has nine states, i.e., the nine combinations of the three digits (A, B, and C) of augend X_i and the three digits (a, b, and c) of addend Y_i , A, B, and C are arranged in a row, and a, b, and c are arranged in a column, as shown in Figs. 6, 7, and 8. Of course, each state is an AND result of two digits.

4. Butterfly Architecture

In terms of all the truth tables of MSD addition expressed in the SPLE scheme, any table has nine states, and each state is an AND result of two digits from a row and a column, respectively. Thus we can use a unitary switch module including nine detecting elements to stand for all the truth tables of MSD addition, as shown in Fig. 9, in which all the detecting elements (G_1, \dots, G_9) can be used for the nine states of any truth table. It can be noted that G_1 is the detecting element for the AND operation of A and a, G_2 is the detecting element for the AND operation of A and b, G_3 is the detecting element for the AND operation of A and c, and so forth, until G_9 is the detecting element for the AND operation of C and c. To construct a corresponding interconnection architecture, we change a standard butterfly interconnect unit, as shown in Fig. 10(a), into a new butterfly interconnect unit, as shown in Fig. 10(b). It can

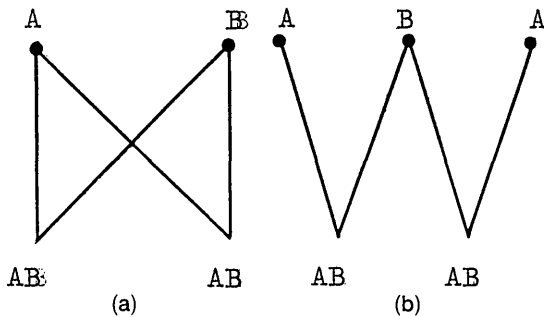


Fig. 10. Comparison of (a) a standard butterfly unit and (b) a trimmed butterfly unit.

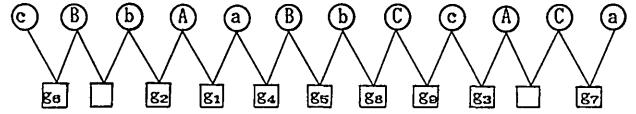


Fig. 11. Corresponding architecture of operands (A, B, and C; a, b, and c) represented by a new butterfly interconnection.

easily be noted from Fig. 10 that, although the new butterfly interconnection is different from the standard butterfly interconnection in form, interconnection rules of these two forms of butterfly are equivalent. Namely, the new butterfly form as shown in Fig. 10(b) but only holds the same advantages, i.e., all the lines in the same angle are parallel, but can also implement all the functions that the standard form as shown in Fig. 10(a) can implement, with the addition of one input node. Thus in the new butterfly form the input end has one more node than the output end. In addition, using the new butterfly form, we can achieve the corresponding interconnection architecture of operands (A, B, and C; a, b, and c), as shown in Fig. 11. It can be noted with ease that the new interconnection architecture can implement all nine state combinations of AND operations of augend X_i (A, B, and C) and addend Y_i (a, b, and c); i.e., the nine combinations come from 11 pairwise combinations of 12 operand digits (double of A, B, C and a, b, c). This new butterfly interconnection architecture is both regular and convenient for optical interconnection

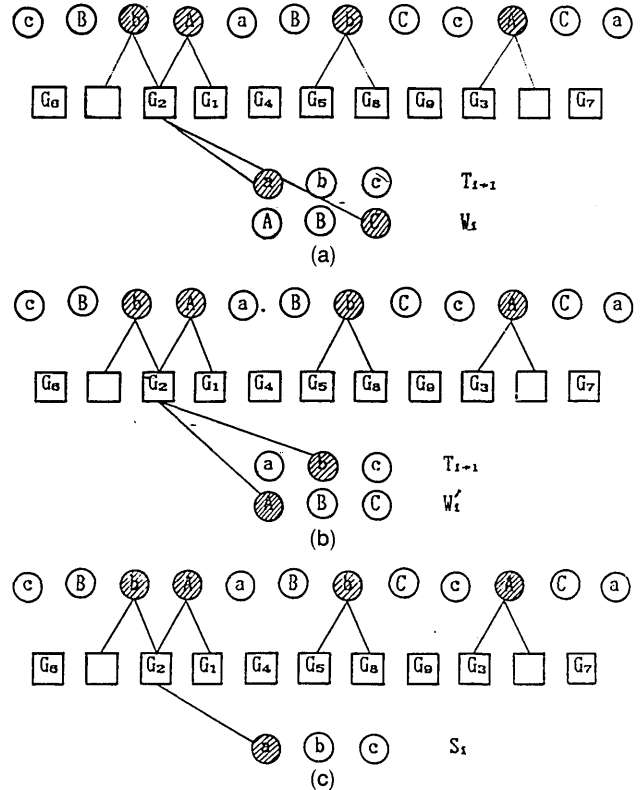


Fig. 12. Operation examples of a MSD adder and subtractor constituted by trimmed butterfly interconnection: (a) $X_i = 1, Y_i = 0$; (b) $W_i = 1, T_i = 0$; (c) $W' = 1, T_i = 0$. Hatched circles indicate having light signals, and hollow circles indicate having no light signals.

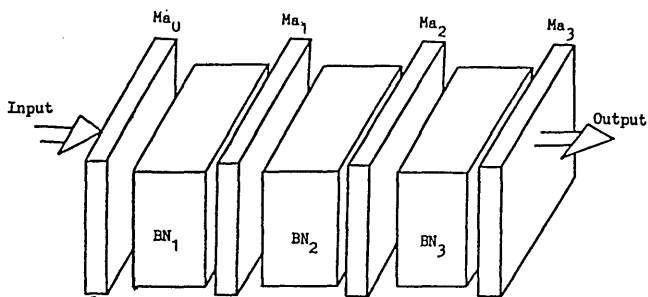


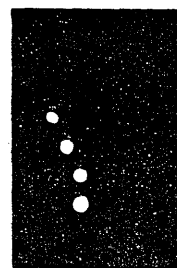
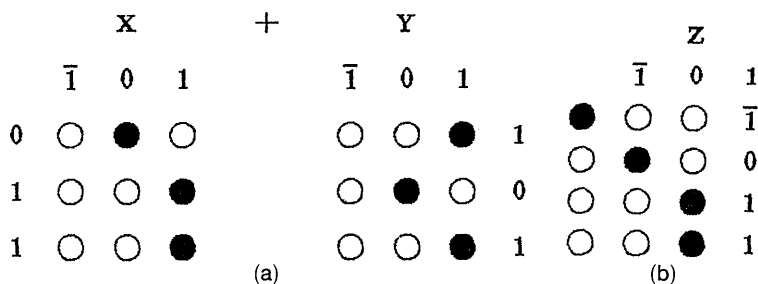
Fig. 13. Optoelectronic butterfly interconnection system for MSD addition and subtraction, where Ma_0 , Ma_1 , Ma_2 , and Ma_3 are four switch modules for implementing logic operations and optical signal arrangements; BN_1 , BN_2 , and BN_3 represent three stages of multilayer butterfly interconnections, as in Fig. 11.

implementations such as fiber and grating interconnections because all the interconnection operations are performed between two adjacent nodes.

The AND results from the nine detecting elements on the detecting planes of modules can drive several LED's or LD's on the light-emitting planes, which give light signals for the next operations. The arrangement of all the possible light signals (A, B, and C; a, b, and c) on the light-emitting planes of modules is the same as that in Fig. 11, but only the detecting elements receiving two light signals can perform AND operations and make their LED's or LD's produce light signals at the corresponding positions. Figures 12(a), 12(b), and 12(c) represent the operating examples of $X_i = 1$ and $Y_i = 0$, $W_i = 1$ and $T_i = 0$, and $W'_i = 1$ and $T'_i = 0$, respectively. Obviously each MSD bit addition is completed through three stages of the new butterfly interconnections and three operations, as shown in Fig. 12, where hatched circles indicate having light signals and hollow circles indicate having no light signals. For the first stage of operations, as shown in Fig. 12(a), if $X_i = 1$ and $Y_i = 0$, i.e., A_i and b_i have light signals, then only the detecting element G_2 can receive two light signals and perform AND operations and can drive its next-stage LED's or LD's a of T'_{i+1} and C of W_i for the next stage of operations according to Figs. 6(a) and 6(b), respectively. For the second stage of operations, as shown in Fig. 12(b), if $W_i = 1$ and $T_i = 0$, i.e., A_i and b_i have light signals, then only the detecting element G_2 can receive two light signals and perform AND operations and can drive its next-stage LED's or LD's b of T'_{i+1}

and A of W'_i for the next stage of operations according to Figs. 7(a) and 7(b), respectively. For the third stage of operations, as shown in Fig. 12(c), if $W'_i = 1$ and $T'_i = 0$, i.e., A_i and b_i have light signals, then only the detecting element G_2 can receive two light signals and perform AND operations and can drive its next-stage LED's or LD's a of S_i of the i th bit according to Fig. 8. The interconnections among all the operand bits can be performed according to the standard butterfly structure as shown in Fig. 4, which can be implemented by use of electrical interconnection within the switch modules. Therefore with the SPLE scheme and two types of butterfly interconnections a fully parallel MSD adder can be constructed by use of three stages of optical butterfly interconnection and four switch modules, Ma_0 , Ma_1 , Ma_2 , and Ma_3 , which can complete logic operations and signal arrangements, as shown in Fig. 13. With the SPLE scheme the MSD subtraction can also be performed as MSD addition by use of the complement of the subtrahend, i.e., with 1 as $\bar{1}$, $\bar{1}$ as 1, and 0 as 0 in the subtrahend. Therefore the MSD architecture in this paper is really a fully parallel optoelectronic MSD adder and subtractor.

For example, for the addition of 6 and 5, $(6)_{10} + (5)_{10} = (11)_{10}$ can also be written as $(110)_{MSD} + (101)_{MSD}$; the simulation input signals, the simulation addition results, and their experimental results are obtained as shown in Figs. 14(a), 14(b), and 14(c), respectively, where filled circles indicate having light signals and hollow circles indicate having no light signals: Fig. 14(a) shows the pattern of input signals, Fig. 14(b) shows their addition results, and Fig. 14(c) shows their experimental results. It can be noted from Figs. 14(b) and Fig. 14(c) that both simulation and experimental results are $(1\ 1\ 0\ \bar{1})_{MSD} = (11)_{10}$, which are obviously correct. For the subtraction of 7 and 5, $(7)_{10} - (5)_{10} = (2)_{10}$ can also be written as $(111)_{MSD} - (101)_{MSD}$; the simulation input signals, the simulation subtraction results, and their experimental results are obtained as shown in Figs. 15(a), 15(b), and 15(c), respectively, where filled circles indicate having light signals and hollow circles indicate having no light signals: Fig. 15(a) shows the pattern of input signals, Fig. 15(b) shows their subtraction results, and Fig. 15(c) shows their experimental results. It can also be noted from Figs. 15(b) and



(c)

Fig. 14. Simulation and experimental example of an MSD addition, $(6)_{10} + (5)_{10} = (110)_{MSD} + (101)_{MSD}$, where filled circles indicate having light signals and hollow circles indicate having no light signals: (a) input signals, (b) addition results, and (c) experimental results.

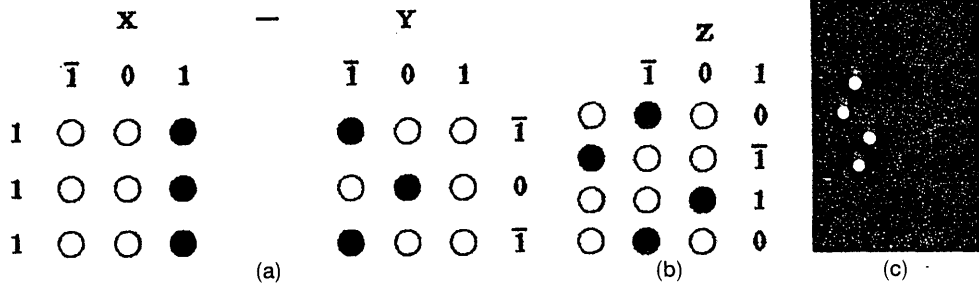


Fig. 15. Simulation and experimental example of an MSD subtraction, $(7)_{10} - (5)_{10} = (110)_{MSD} + (101)_{MSD}$, where filled circles indicate having light signals and hollow circles indicate having no light signals: (a) input signals, (b) subtraction results, and (c) experimental results.

15(c) that both simulation and experimental results are $(0\ 1\ \bar{1}\ 0)_{MSD} = (2)_{10}$, which are obviously correct.

5. Summary and Conclusions

Development of fast computing systems could utilize two approaches: one would research fast logic devices, the other would arrange all the logic gates or devices and make them perform in parallel. Because the former is limited by materials of devices, the latter is an important approach to developing optical computing. The parallel systems including two elements: one is a parallel algorithm, the other is a parallel implementing architecture. In this paper we have studied the MSD algorithm, which is a carry-free parallel algorithm, and we have discussed the characteristics of three stages of operations of MSD addition. Thus we propose a space-position-logic-encoding (SPLE) scheme that not only makes best use of the convenience of binary logic operation but is also suitable for the trinary property of 1, 0, and $\bar{1}$ in MSD digits. According to the truth tables of all the operations of MSD addition, we propose a unitary optoelectronic switch module including nine detecting elements (G_1, \dots, G_9) to implement nine AND operations of any truth table. To produce nine combinations of two groups of MSD operands in each bit, we change a standard butterfly interconnection into a new form, and on this basis we build a butterfly architecture of an optically fully parallel MSD adder and subtracter. This butterfly network is two dimensional; one dimension is a standard form for implementing the interconnection among operand bits, which is completed electrically within switch modules, and the other dimension is a new butterfly form for implementing the interconnection of two groups of operand digits in one bit, which is completed optically. Finally, the simulation and the experimental results of MSD addition and subtraction are given. Therefore we have implemented the effective combination of a parallel carry-free algorithm (MSD) and a parallel implementing architecture (optical butterfly interconnection), which is a new approach of digital optical computing. In the future we will study the butterfly architectures of an optical MSD multiplier and divider; furthermore, we will build a unitary

optical parallel MSD computing system to implement addition, subtraction, multiplication, and division.

This research was supported by the Chinese Foundation of Science.

References

1. M. J. Murdochca, A. Huang, J. Jahns, and N. Streibl, "Optical design of programmable logic arrays," *Appl. Opt.* **27**, 1651-1660 (1988).
2. D. G. Sun and Z. H. Weng, "Butterfly interconnection implementation for an n -bit parallel ripple carry full-adder," *Appl. Opt.* **30**, 1781-1785 (1991).
3. D. G. Sun, Q. Xiang, N. X. Wang, and Z. H. Weng, "Butterfly interconnection implementation for an n -bit parallel full-adder/subtractor," *Opt. Eng.* **31**, 1568-1575 (1992).
4. A. Huang, Y. Tsunoda, J. W. Goodman, and S. I. Shihara, "Optical computation using residue arithmetic," *Appl. Opt.* **18**, 149-162 (1979).
5. D. Psaltis and D. Casasent, "Optical residue arithmetic: a correlation approach," *Appl. Opt.* **18**, 163-171 (1979).
6. B. L. Drake, R. P. Bocker, M. E. Lasher, R. H. Patterson, and W. J. Miceli, "Photonic computing using the modified-digit number representation," *Opt. Eng.* **25**, 38-43 (1986).
7. K. Hwang and A. Louri, "Optical multiplication and division using modified-signed-digit symbolic substitution," *Opt. Eng.* **28**, 364-372 (1989).
8. F. B. McCormick and M. E. Prise, "Optical circuitry for free-space interconnections," *Appl. Opt.* **29**, 2013-2018 (1990).
9. J. Jahns, "Optical implementation of the Banyan network," *Opt. Commun.* **76**, 321-324 (1990).
10. J. Jahns and M. J. Murdochca, "Crossover networks and their optical implementation," *Appl. Opt.* **27**, 3155-3160 (1988).
11. K. H. Brenner and A. Huang, "Optical implementation of the perfect shuffle interconnection," *Appl. Opt.* **27**, 135-137 (1988).
12. D. G. Sun, N. X. Wang, Z. W. Lu, and Z. H. Weng, "Optical implementation of butterfly interconnection and digital logic operation by grating," *Chin. J. Lasers* **1**, 549-554 (1992).
13. Y. Li and G. Eichmann, "Conditional symbolic modified signed-digit content-addressable memory logic elements," *Appl. Opt.* **26**, 2328-2333 (1987).
14. A. K. Cherri and M. A. Karim, "Modified-signed digit arithmetic using an efficient symbolic substitution," *Appl. Opt.* **27**, 3824-3827 (1988).
15. G. Eichmann, A. Kostrzewski, D. H. Kim, and Y. Li, "Optical higher-order symbolic recognition," *Appl. Opt.* **29**, 2135-2147 (1990).
16. A. C. Walker, "Application of bistable parallel optical gate arrays to all-optical parallel processing," *Appl. Opt.* **25**, 1578-1585 (1986).

17. R. A. Craig, "Two-input programmable optical processing units," *Appl. Opt.* **31**, 6840–6851 (1992).
18. M. E. Prise, "A module for optical logic circuits using symmetric self-electro-optic effect devices," *Appl. Opt.* **29**, 2164–2170 (1990).
19. M. A. Habli and K. Leonik, "Polarization-coded optical logic gates for N -inputs," *Optik* **91**, 100–102 (1992).
20. A. M. Khaw and U. R. Nejjib, "Optical logic gates employing liquid crystal optical switches," *Appl. Opt.* **26**, 270–273 (1987).
21. D. Sanger and E. Wihardjo, "Parallel optical logic gates using one-dimensional spatial encoding," *Opt. Eng.* **29**, 690–695 (1990).
22. S. Barua, "Single-stage optical adder/subtractor," *Opt. Eng.* **30**, 265–270 (1991).