Demonstration of an optoelectronic interconnect architecture for a parallel modified signed-digit adder and subtracter

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Abstract. A space-position-logic-encoding scheme is proposed and demonstrated. This encoding scheme not only makes the best use of the convenience of binary logic operation, but is also suitable for the trinary property of modified signed-digit (MSD) numbers. Based on the space-position-logic-encoding scheme, a fully parallel modified signed-digit adder and subtracter is built using optoelectronic switch technologies in conjunction with fiber-multistage 3-D optoelectronic interconnects. Thus an effective combination of a parallel algorithm and a parallel architecture is implemented. In addition, the performance of the optoelectronic switches used in this system is experimentally studied and verified. Both the 3-bit experimental model and the experimental results of a parallel addition and a parallel subtraction are provided and discussed. Finally, the speed ratio between the MSD adder and binary adders is discussed and the advantage of the MSD in operating speed is demonstrated. © 1996 Society of Photo-Optical Instrumentation Engineers.

Subject terms: parallel algorithm; parallel architecture; space-position-logic-encoding; optoelectronic switch and interconnect technologies; modified-signed-digit adder and subtractor.

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1 Introduction

There are two options for developing parallel digital optical computing systems: one is to research the carry-free or carry-limited parallel algorithm, the other is to research the optical implementing architecture. Of course, the best selection is an effective combination of these two options. The modified signed-digit (MSD) algorithm is an effective carry-free or carry-limited algorithm, and symbolic substitution is an optical parallel implementing approach. Thus, an optical MSD parallel computing system based on symbolic substitution is a typical example of a combination of a parallel algorithm and a parallel implementation approach. Especially in recent years, new MSD architectures have been proposed and studied. In fact, the important factor for the realization of the conversion from the algorithm to the hardware structure is having an effective encoding scheme, so the research on encoding schemes has received more attention as an important content in digital optical computing. At the same time, improved encoding methods have been proposed and studied.

These improved encoding schemes, especially space-variant encoding, not only expand encoding theory but also make best use of the parallelisms of both optics and the MSD algorithm, thus playing an important role in parallel digital optical computing. However, in the proposed space encodings, because some patterns are required to represent operand bits, the space size taken by each operand bit cannot be made very small, which limits the miniaturization and integration of MSD optical computing systems. Multilayer and multistage optical interconnection is another important parallel implementation approach in digital optical computing that can help the switches to complete logic operations as well as implement data transportation and switching.

Optoelectronic interconnects have shown a promising future as the hardware approach of digital optical computing because they can be compatible with microstructure optoelectronic switch technologies. In addition, multilayer and multistage optoelectronic interconnects, as the hardware approach of parallel digital optical computing, are suitable for controlling the digitized signal connections and operations as well as for exploiting some optical advantages such as higher bandwidth and lower crosstalk. In digital optical computing, perfect shuffle, crossover, and butterfly are three typical interconnect networks.
among which the butterfly has been proved to have some advantages over the others in optical computing. Addi-
tion and subtraction are the most primitive arithmetic op-
erations in digital computation. Almost all of the other
arithmetic operations such as multiplication, division, and
some special functions must be performed based on addi-
tion and subtraction. The purpose of this paper is to pre-
sent the implementation of a fully parallel MSD adder and sub-
tracer based on the effective combination of the MSD al-
gorithm and the butterfly interconnection architecture by
use of a space-position-logic-encoding (SPLE) scheme that
exploits both the carry-free property of the MSD algorithm
and the convenience of binary logic operation with opto-
electronic logic technology. A 3-bit experimental model of
a parallel adder and subtractor based on the MSD algo-
rithm and fiber interconnect technology is built, and correct
experimental results are provided. To interface the parallel
optoelectronic adder architecture with the conventional
electronic computers in the near future, the conversion and
brief comparison between the MSD and binary additions
are carried out, and the advantage of our MSD adder in
speed is demonstrated.

2 MSD Algorithm Review

An MSD bit can be written as

$$D_{MSD} = [1, 0, \bar{T}]$$

where \(\bar{T}\) represents \(-1\). Each MSD bit has three values for
selection (i.e., 1, 0, and \(-1\)). These three possible values 1,
0, and \(\bar{T}\) of each MSD bit are called digits. Then each
decimal number can be represented in the MSD number
system by the coefficients of the polynomial:

$$D_{10} = [1, 0, \bar{T}] 2^0 + [1, 0, \bar{T}] 2^1 + \ldots + [1, 0, \bar{T}] 2^n.$$  

For example, a decimal number 27 would be written as:

$$D_{10} = 1 \cdot 2^4 + 1 \cdot 2^3 + 0 \cdot 2^2 + 1 \cdot 2^1 + 1 \cdot 2^0 = [11011]_{MSD},$$

$$D_{10} = 1 \cdot 2^4 + 1 \cdot 2^3 + 1 \cdot 2^2 + (\bar{T}) \cdot 2^1 + 1 \cdot 2^0 = [\bar{1}111\bar{1}]_{MSD},$$

where the selection \(0, \bar{T}\) of each MSD bit are called digits. Then each
decimal number can be represented in the MSD number
system by the coefficients of the polynomial:

$$D_{10} = [1, 0, \bar{T}] 2^0 + [1, 0, \bar{T}] 2^1 + \ldots + [1, 0, \bar{T}] 2^n.$$  

For example, a decimal number 27 would be written as:

$$(27)_D = 1 \cdot 2^4 + 1 \cdot 2^3 + 0 \cdot 2^2 + 1 \cdot 2^1 + 1 \cdot 2^0 = [11011]_{MSD},$$

Note that the first selection \(11011\) is the same as a
binary number, so it can be said that the binary number is
only a special form of the MSD number. This feature is a
basis for the conversion from an MSD number to a binary
one, as discussed in Sec. 6.

For two MSD numbers, \(X_{MSD}[X_{n-1}, \ldots, X_1, \ldots, X_0]\) and
\(Y_{MSD}[Y_{n-1}, \ldots, Y_1, \ldots, Y_0]\), the addition can be performed
through a three-step operation. At the first step, a weight
digit \(W_i\) and a transfer digit \(T_{i+1}\), which are MSD bits, are
produced by

$$X_i + Y_i = 2T_{i+1} + W_i,$$  

where all the values of \(T_{i+1}\) and \(W_i\) are only related to \(X_i\)
and \(Y_i\), and determined by their truth tables, as shown as
Figs. 1(a) and 1(b), respectively.

At the second step, another pair of weight digit \(W_i'\) and
transfer digit \(T_{i+1}'\) is produced by

$$W_i + T_i = 2T_{i+1} + W_i',$$  

where all the values of \(T_{i+1}'\) and \(W_i'\) are related only to \(W_i\)
and \(T_i\) and are determined by their truth tables, as shown as
Figs. 2(a) and 2(b), respectively.

The third step generates the final sum digit \(S_i\):

$$S_i = W_i' + T_i',$$  

where all the values of \(S_i\) are related only to \(W_i'\) and \(T_i'\) and
are given by the truth table, as shown in Fig. 3, which is the
same as Fig. 1(a). In the same step of operations, all the operations
are among the different bits are the same, thus Figs. 1, 2, and 3 all indicate only the 1-bit operations. In terms
of the three-step operations of MSD addition, the MSD addi-
tion of two 3-bit numbers can be depicted in the butterfly
interconnection architecture as shown in Fig. 4, where
\(X(=X_0X_1X_2X_3)\) and \(Y(=Y_0Y_1Y_2Y_3)\) are augend and addend,
respectively, and \(Z(=Z_0Z_1Z_2Z_3Z_4)\) is the final addition
result.

3 Space-Position-Logic-Encoding Scheme

As described, the difference between the MSD bit and the
binary bit is that the binary bit has only two selections, 1
and 0, while the MSD bit has three selections, 1, 0, and \(\bar{T}\),
respectively. Therefore, it is unlike the binary bit, which
uses higher and lower voltages as an encoding scheme. In
digital optical computing, because of optical properties and
the symbolic substitution theorem, pattern encoding, polar-
ization encoding, and other encoding schemes occur successively. According to the characteristics of the MSD numbers and the optical
properties, we propose an SPLE scheme, as shown in Fig. 5(a),
in which three different space positions, A, B, and C (or a,
b, and c), are used to represent 1, 0, and 1 of MSD bits in
which three light-emitting diodes (LEDs) or laser diodes
(LDs) at A, B, and C (or a, b, and c) represent only one
MSD bit; namely, only one LED or LD has a light signal,
and a light signal at a different position of the \(i^{th}\) bit

Fig. 1 Truth tables of the first-step operation of MSD addition: (a) for transfer digits \(T_{i+1}\), and (b) for weight digits \(W_i\).
represents a different value. The combination of all their work states is shown in Fig. 5(b). For example, the light signal of the LED or the LD at position A of the $X_i$ bit represents $X_i = 1$, and at the same time, the LEDs or LDs at positions B and C of the $X_i$ bit have no light signals. Thus each space position has two states, either having a light signal or having no light signal, which is similar to the logic operations of the binary algorithm. Therefore it is an SPLE scheme. Then with the SPLE scheme, the truth tables for the three operations of MSD additions, as shown in Figs. 1, 2, and 3, become the new forms, as shown in Figs. 6, 7, and 8, where any table has nine states, i.e., the nine combinations of the three digits $A$, $B$, and $C$ of augend $X_i$, and the three digits $a$, $b$, and $c$ of addend $Y_i$. The three digits of the augend are arranged in a column and the three digits of the addend are arranged in a row, as shown in Figs. 6, 7, and 8. Of course, each state is an AND result of two digits.

**4 Butterfly Interconnect Architecture**

In terms of all the truth tables of MSD addition expressed in the SPLE scheme, any table has nine states, and each state is an AND result of two digits from a row and a column, respectively. Thus we can use a unitary detecting array including nine detecting elements to stand for all the truth tables of MSD addition, as shown in Fig. 9, in which
all the detecting elements \( (G_1, \ldots, G_9) \) can be used for the nine states of any truth table. Note that \( G_1 \) is the detecting element for the AND operation of \( A \) and \( a \), \( G_2 \) is the detecting element for the AND operation of \( A \) and \( b \), and so forth, until \( G_9 \) is the detecting element for the AND operation of \( C \) and \( c \). To build a multilayer butterfly interconnection architecture corresponding to the multibit computing, for every step operation of any bit computation, we use the most basic butterfly to represent the nine AND operations, as shown in Fig. 11. Where hatched circles indicate having light signals, and hollow circles indicate having no light signals. For the first stage of operations, as shown in Fig. 11(a), if \( T_i = 1 \) and \( W_i = 1 \) (i.e., \( A_i \) and \( a_i \) have light signals), then only the detecting element \( G_1 \) can receive two light signals and perform AND operations and can drive its next-stage LEDs or LDs \( a \) of \( T_{i+1} \) and \( B \) of \( W_i \) for the next stage of operations according to Figs. 6(a) and 6(b), respectively. For the second stage of operations, as shown in Fig. 11(b), if \( W_i = 1 \) and \( T_i = 0 \) (i.e., \( A_i \) and \( b_i \) have light signals), then only the detecting element \( G_2 \) can receive two light signals and perform AND operations and can drive its next-stage LEDs or LDs \( b \) of \( T_{i+1} \) and \( A \) of \( W_i \) for the next stage of operations according to Figs. 7(a) and 7(b), respectively. For the third stage of operations, as shown in Fig. 11(c), if \( W_i = 0 \) and \( T_i = 0 \) (i.e., \( B_i \) and \( b_i \) have light signals), then only the detecting element \( G_5 \) can receive two light signals and perform AND operations and can drive its next-stage LEDs or LDs \( b \) of \( T_{i+1} \) of the \( i \)th bit according to Fig. 8. The interconnections among all the operand bits can be performed according to the standard butterfly structure as shown in Fig. 4, which can be implemented by use of electrical interconnection or optical guided-wave interconnection within the switch modules. The interconnections among the 12 positions of two groups of operand digits can be completed by use of optical interconnections such as gratings and fibers. Therefore with the SPLE scheme and the simplest butterfly interconnections, a fully parallel MSD adder can be constructed by use of three stages of optical butterfly
interconnection and four switch modules, \( M_0, M_1, M_2, \) and \( M_3 \), which can complete logic operations and signal arrangements, as shown in Fig. 12, where Fig. 12(a) is the schematic construction of a 3-bit optoelectronic MSD adder, and Fig. 12(b) is the circuit of each switch cell of optoelectronic switch modules. The circuit is constituted by using photosensitive diodes, LEDs, bipolar transistors, and their associated electronic devices to implement the AND operations. Because all the switch cells are required to perform AND operations of two adjacent nodes, the whole switch module has many of the same circuits as shown in Fig. 12 and can reliably work. This can be verified by the experimental results of the logic performance of this optoelectronic switch as shown in Fig. 13, where Fig. 13(a) is the state of one-signal forcing, and Fig. 13(b) is the state of two-signal forcing. Because the two input signals are the same, only one input signal curve is shown in both Figs. 13(a) and 13(b). In either figure, the upper curve is the input signal, and the lower curve is the AND operation result of two input signals. With the SPLE scheme, the MSD subtraction can also be performed as MSD addition by use of the complement of the subtrahend (i.e., with 1 as 1, 1 as 1, and 0 as 0 in the subtrahend). Therefore, the MSD architecture in this paper is really a 3-bit parallel optoelectronic MSD adder and subtracter.

5 Experiments

With optoelectronic and fiber interconnect technologies, an experimental model of 3-bit optoelectronic parallel MSD adder and subtracter was built by us, as shown in Fig. 14, and the correct experimental results were obtained.

For example, the addition of 6 and 5, \((6)_{10} + (5)_{10} = (11)_{10}\), is the addition of two 3-bit MSD numbers. As described in Sec. 2, one decimal number can have several MSD forms for selection. For convenience, we just select the form which is the same as binary representation, so the addition of 6 and 5 can also be written as \((110)_{\text{MSD}} + (101)_{\text{MSD}}\). The signal pattern and experimental result of the input signals are shown as in Figs. 15(a) and 15(b), respectively, and both the simulation and experimental results of their addition are obtained, as shown in Figs. 16(a) and 16(b), respectively, where filled circles indicate having light signals and hollow circles indicate having no light signals. It can be noted from Figs. 16(a) and 16(b) that both simulation and experimental results are \((1101)_{\text{MSD}} = (11)_{10}\), which are obviously correct. For the subtraction of 7 and 2, \((7)_{10} - (2)_{10} = (0)_{10}\), can also be written as \((111)_{\text{MSD}} + (111)_{\text{MSD}}\); the signal pattern and experimental result of input signals are shown as Figs. 17(a) and 17(b), respectively, and both the simulation and experimental results of their subtraction are obtained as shown in Figs. 18(a) and 18(b), respectively, where filled circles indicate having light signals and hollow circles indicate having no light signals. It can be noted from Figs. 18(a) and 18(b) that both simulation and experimental results are \((0000)_{\text{MSD}} = (0)_{10}\), which are obviously correct.

6 Conversion Between the MSD Adder and Binary Ones

We know from the preceding demonstrations that results of these MSD additions are generally MSD digits. Thus it is
necessary to convert the MSD digits into binary ones to interface this parallel MSD adder with current electronic computers. At the same time, we can also compare the MSD adder with binary ones in operating speed. In fact, this work has been started by Hwang and Louri.3

We assume an output result from the MSD adder is $Z_m$. To convert it into the binary form $Z_b$, we can separate $Z_m$ into two parts $Z_m^+$ and $Z_m^-$. Because the $Z_b$ comes from the

![Fig. 13 Experimental results of logic performance of an optoelectronic switch module: (a) the state of one-signal forcing and (b) the state of two-signal forcing, where the upper curve is the input signal, and the lower curve is the AND operation result.](image13)

![Fig. 14 Experimental model of 3-bit MSD adder and subtracter by use of optoelectronic logic and fiber interconnection technologies.](image14)

![Fig. 15 Signal pattern and experimental result of an MSD addition—$(6)_{10} + (5)_{10} = (110)_{MSD} + (101)_{MSD}$: (a) signal pattern and (b) experimental result.](image15)

![Fig. 16 Simulation and experimental results of an MSD addition—$(6)_{10} + (5)_{10} = (110)_{MSD} + (101)_{MSD}$: (a) simulation result and (b) experimental result.](image16)

![Fig. 17 Signal pattern and experimental result of an MSD subtraction—$(7)_{10} - (7)_{10} = (111)_{MSD} - (111)_{MSD}$: (a) signal pattern and (b) experimental result.](image17)

![Fig. 18 Simulation and experimental results of an MSD subtraction—$(7)_{10} - (7)_{10} = (111)_{MSD} - (111)_{MSD}$: (a) simulation result and (b) experimental result.](image18)
original $Z_m$, their values should be equal to each other, but their representations are different, so the MSD addition can be depicted in Eq. (6):

$$Z_b = Z_m = Z_m^\dagger + Z_m = Z_m^\dagger,$$

(6)

where $Z_m^\dagger$ can be obtained by replacing $\overline{1}$ with 0 and keeping all the 0 and 1 unchanged in $Z_m$, while $Z_m$ can be obtained by replacing 1 with 0 and keeping all the 0 and 1 unchanged in $Z_m$. For a positive $Z_m$, its most significant bit $Z_m(n)$ must be 1, so the most significant bit of $Z_m^\dagger$, $Z_m^\dagger(n)$, must be 1 also, while the most significant bit of $Z_m$, $Z_m(n)$, must be 0. In terms of the truth table for the first operation of MSD addition, as shown in Fig. 1(a), $T_{n+1}$ must be 1. Furthermore, in terms of operation relation as shown in Fig. 4, the final addition result, $S_{n+1}$ comes from the operations between $T_{n+1}$ and $T_n'$. The operations are performed in accordance with third-operation rules of MSD addition, as shown in Fig. 3, in that no matter what value $T_{n+1}'$ is, $S_{n+1}$ is always 1 because $T_{n+1}=1$. Therefore, each MSD addition as defined in Eq. (6) always makes the number of 1s reduced. In the same manner, for a negative $Z_m$, its most significant bit, $Z_m(n)$, must be 1, so the most significant bit of $Z_m^\dagger$, $Z_m^\dagger(n)$, must be 1 and the most significant bit of $Z_m$, $Z_m(n)$, must be 0. In terms of the truth table for the third operation of MSD addition as shown in Fig. 3, no matter what value $T_{n+1}'$ is, $S_{n+1}$ is always 1 because $T_{n+1}=1$. Therefore, each MSD addition as defined in Eq. (6) always makes the number of 1s reduced. In terms of the symmetry of 1 and $\overline{1}$ in the three operations of MSD addition, we can only consider the case for a positive $Z_m$.

In terms of the conversion method as defined in Eq. (6), we can conclude that no matter how many bits $Z_m$ has, there are not the operations of 1 and 1, 1 and 1, and 1 and 1 during the addition between $Z_m^\dagger$ and $Z_m^\dagger$; there are only the operations of 1 and 0, 1 and 0, and 0 and 0. Thus, the possibilities for $T_{i+1}$ to be 0, 1, and 1 are all reduced to 2/3 of general cases in accordance with Fig. 1(a), and the possibilities for $W_i$ to be 1 and 0 do not change, while the possibility to be 0 is reduced to 1/5 of general cases in accordance with Fig. 1(b). So, the possibilities for $T_{i+1}$ to be 1 and $\overline{1}$ are reduced to 2/3 of general cases; while according to Fig. 2(a), the possibility to be 0 is

$$\frac{\frac{3}{7} \times \frac{1}{2} \times 2 + \frac{1}{2} \times 2 + \frac{1}{2} \times \frac{1}{2}}{7} = \frac{31}{105} < \frac{3}{10}.$$  

(7)

According to Fig. 2(b), the possibilities for $W_i$ to be 1 and 1 are

$$\frac{\frac{3}{7} \times \frac{1}{2} + \frac{1}{2}}{2} = \frac{7}{30} < \frac{3}{10},$$

(8)

and the possibility to be 0 is

$$\frac{\frac{3}{5} \times 4 + \frac{1}{2} \times \frac{1}{2}}{5} = \frac{41}{75} < \frac{6}{10}.$$  

(9)

Finally, according to Fig. 3, the possibility for $S_i$ to be $\overline{1}$ is

$$\frac{\frac{1}{3} \times \frac{1}{2} \times \frac{1}{2} + \frac{1}{2} \times \frac{1}{2} + \frac{1}{2} \times \frac{1}{2} + \frac{1}{2} \times \frac{1}{2}}{3} = \frac{69}{300} < \frac{7}{30} < \frac{4}{10}.$$  

(10)

Therefore, each MSD addition makes the number of $\overline{1}$ in $Z_m$ reduced to 1/4 of the original case at least.

With the assumption that an $N$-bit $Z_m$ requires the conversions of $n$ times, in terms of Eq. (10), we have

$$N' < \frac{N}{4^n},$$

(11)

where $N'$ is the number of $\overline{1}$. Of course, if $N' < 1$ is required, only the following relation is required:

$$\frac{N}{4^n} \approx 1,$$

(12)

namely,

$$N \approx 4^n \text{ or } n = \log_4 N.$$  

(13)

In the binary addition, an $N$-bit addition generally requires the delay time that $N$ carries, while each bit addition also requires about three logic operations such as AND, OR, and so on. Therefore, for the $N$-bit addition, the speed ratio between the MSD adder and binary ones is about

$$\beta \approx \frac{N}{n} \approx \frac{N}{\log_4 N}.$$

(14)

A plot of $\beta$ versus $N$ is shown in Fig. 19. It can be found from Fig. 19 that the more operand bits (i.e., data width), the higher the speed ratio between the MSD adder and binary ones, namely, the more obvious the advantage of the MSD system we presented herein. For a 32-bit $Z_m$, we perform the three times of conversion additions, then get a binary form as shown in Fig. 20, which agrees well with the approximate theoretical formula, Eq. (13). However, this parallel architecture of optoelectronic MSD adder and subtractor based on the SPLD scheme really has its own disadvantages. One important disadvantage is that it requires three times more hardware than the binary adder.
A 32-bit MSD number:
\[ Z = 101110111011100111111110110 \]

After the first conversion addition:
\[ Z_1 = 1101010011010010010011010 \]

After the second conversion addition:
\[ Z_2 = 101010100111110001001100010 \]

After the third conversion addition:
\[ Z_3 = 1010111010010100100110100010 \]

Fig. 20 Thirty-two bit conversion example from MSD digits and binary ones.

7 Summary and Conclusions

In this paper, we discussed the characteristics of three stages of operations of MSD addition, and on this basis we proposed an SPLIE scheme that not only makes best use of the convenience of binary logic operation but is also suitable for the trinary property of 1, 0, and 1 in MSD numbers. According to the truth tables of all the operations of MSD addition, we proposed a unitary optoelectronic switch module including nine detecting elements \((G_1, \ldots, G_9)\) to implement nine AND operations of any truth table, and on this basis we built the simplest butterfly architecture of an optically fully parallel MSD adder and subtractor. This butterfly network is two dimensional: one dimension is for implementing the interconnection among operand bits, which is completed electrically within switch modules now and will be completed optically in our next work, and other dimension is the simplest butterfly form for implementing the interconnection of two groups of operand digits in 1 bit, which is now completed optically. Finally, the 3-bit experimental model of a fully parallel MSD adder and subtractor was built using the simple optoelectronic switch technologies in conjunction with fiber interconnection technologies. At the same time, the simulation and the experimental results of MSD addition and subtraction are given.

In fact, not only can the 3-bit parallel MSD adder and subtractor be built using four optoelectronic switch modules and three stages of simple butterfly interconnects, as described in this paper, but any multibit parallel MSD adder and subtractor can also be built using four switch modules and three stages of butterfly interconnects. Note that the simultaneous increases of operand data width and operation hardware, exactly like the analysis and comparison we did in Sec. 6, will take more time in the future research. The better trade-off between the operand data width and hardware is an important task to develop for the optoelectronic parallel MSD adder and subtractor discussed herein. After all, we have really implemented the effective combination of a parallel carry-free algorithm (MSD) and a parallel implementing architecture (optical multilayer butterfly interconnection), which is a new approach of high-speed digital optical computing. At the same time, we have also researched the optoelectronic multiplier and divider and communication of this optoelectronic MSD computing system with binary electronic computers, which will be published in other papers. In our future work, we will use the micro-optoelectronic integration technology and microstructure interconnect technology to replace the current simple optoelectronic and fiber interconnect technologies to research and make the practical multibit optoelectronic parallel computing units.

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References

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