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Study on the instability of organic field-effect transistors based on fluorinated copper phthalocyanine

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Abstract

The effects of positive and negative gate-bias stress on organic field-effect transistors (OFET) based on tantalum (Ta)/tantalum pentoxide (Ta_2O_5)/fluorinated copper phthalocyanine ($F_{16}CuPc$) structure are investigated as a function of stress time and stress temperature. It is shown that gate-bias stress induces a parallel threshold voltage shift (ΔV_T) of OFETs without changes of field-effect mobility μ_{EF} and sub-threshold slope (ΔS). The ΔV_T is observed to be logarithmically dependent on time at high gate-bias appropriate to OFET operation. More importantly, the shift is directional, namely, be large shift under positive stress and almost do not move under negative stress. The threshold voltage shift is temperature dependent with activation energy of 0.51 eV. We concluded that threshold voltage shift of the OFET with $F_{16}CuPc$ as active layer is due to charge trapping in the insulator in which trapped carriers have redistribution.

Keywords: Threshold voltage shift; Organic field-effect transistor; Activation energy

1. Introduction

Recently, organic field-effect transistor (OFET) has attracted tremendous attention due to its potential application in low-cost large-area flexible displays and low-end data storage such as smart cards [1–4]. Although organic materials can offer many advantages for lower temperature manufacturing and lower-cost deposition processes such as spin coating, printing, evaporation, two kinds of instabilities of OFETs must be overcome before OEFT can be fully applied. Air stable is a well-known problem for organic semiconductor materials itself. Another instability comes from OFET device operation, which is characteristic of threshold voltage shift (ΔV_T) after gate-bias stress and is often observed in the case of hydrogenated amorphous silicon thin film transistor (a-Si:H TFT). Previous reports on a-Si:H TFT show that there are two distinct mechanisms responsible for the threshold voltage shift of a-Si:H TFT, namely, charge trapping in the insulator and creation of metastable states in the active layer [5–7]. However, several researches on stability of OFETs indicated that the exact nature of threshold voltage shift in the OFET is still a matter of debate [8–10].

In this paper, our OFET devices use $F_{16}CuPc$ as active layer and tantalum pentoxide (Ta_2O_5) as insulator. $F_{16}CuPc$ is a promising material for n-channel operation, which has proven high performance and stability in air. The structural formula of $F_{16}CuPc$ molecule is shown in Fig. 1a. We observed that threshold voltage shift is very large after gate-bias stress and it is logarithmically dependent on time. In addition, threshold voltage has obvious shift under positive bias stress and almost does not move under negative bias stress. Both threshold voltage shift (at 50 V) and field-effect mobility are temperature dependent with activation energy of 0.51 and 0.25 eV, respectively. The different activation energies of threshold voltage shift and field-effect mobility indicate that activation energies of threshold voltage shift may derive from redistribution of trapped charge in the insulator by hoping conduction rather than supply function of mobile carrier [11]. We conclude that the instability derive from charge trapping and then distributing in the insulator (at high field at least).

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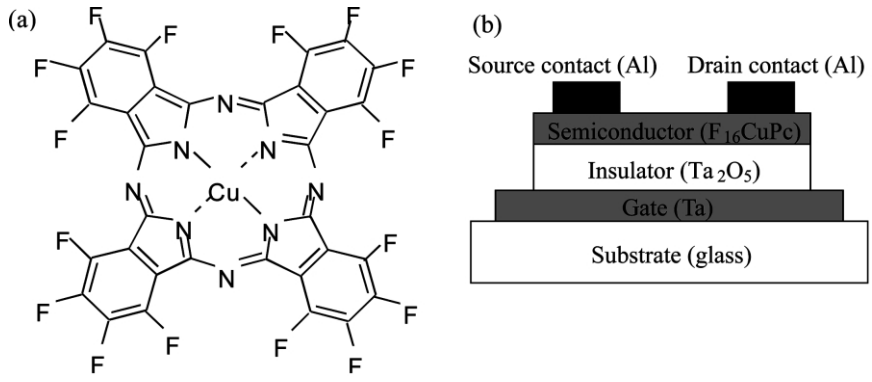

Fig. 1. Chemical structure of F_{16}CuPc (a) and schematic of F_{16}CuPc-based OFET (b).

2. Experimental details

F_{16}CuPc was purchased from the Aldrich Chemical Co. and further purified by sublimation at a pressure of 10^{-4} Pa. The OFET device structure was shown in Fig. 1b. Corning7059 glass is used as substrate and Ta metal thin film is used as gate electrode. The Ta_2O_5 film, which has a capacitance of 36 nF cm^{-2}, is deposited as gate insulator using magnetron reactive sputtering. F_{16}CuPc thin film was prepared by vacuum evaporation at a pressure of 10^{-5} Pa and substrate temperature is held at 150 °C. Thickness of prepared film was approximately 500 nm. Finally, gold source and drain contacts were evaporated on top of the organic semiconductor through a mask that defines channel width and length as 1200 and 80 μm, respectively. Samples are handled in air and measured in vacuum. Temperature dependent measurements were done by placing the device on the cold-finger of a close-cycle helium cryostat (made in China) equipped with electrical feedthroughs. The electrical measurements are carried out using tow KEITHLEY 236 unit voltage sources. After each measurement of gate-bias or temperature, the sample was unstressed for restoration (trapped charge release) at room temperature until its virgin characteristics are obtained and then next measurement is made.

3. Results and discussion

Fig. 2 shows the two-transfer curve of the same OFET device. After the first gate-sweep, gate contact was stressed at 50 V for 50 s and then second gate-sweep was taken. Fig. 2a and b is the same plot in different axis scale. Fig. 2c is the plot of the square root drain current vs. gate voltage, which, derived from Fig. 2a. Fig. 2a shows that two curves have same shapes with only a parallel shift along the gate voltage axis, denoting a different threshold voltage V_T. The similar sub-threshold slope ($\Delta S = 2.85$ V decade^{-1}) can be observed from Fig. 2b, which indicated that no extra electron states

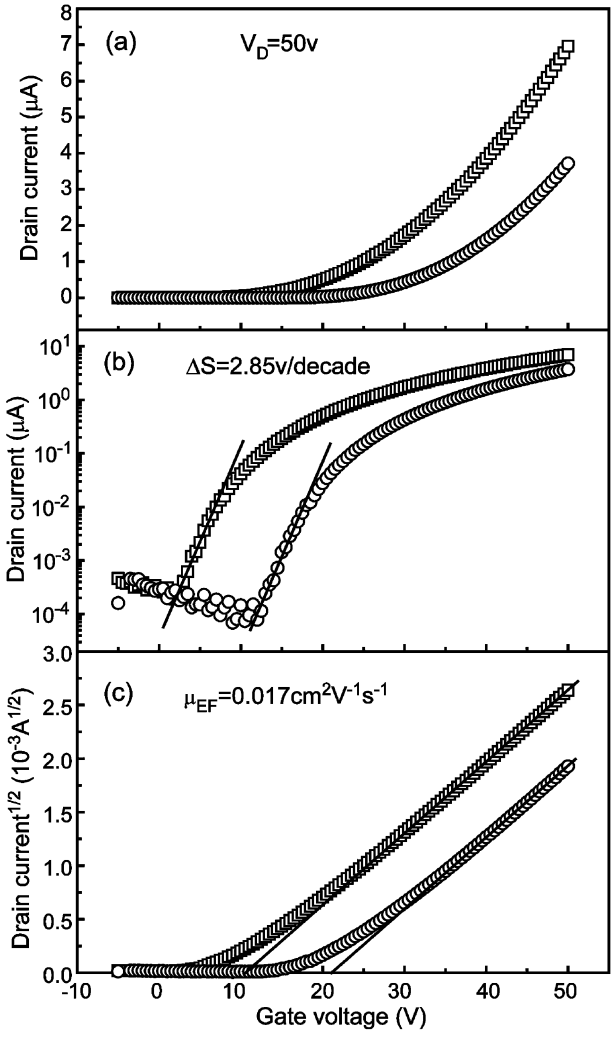

Fig. 2. Two plots of the drain current as a function of gate voltage with different histories at $V_d = 50$ V, in linear (a) and semi-logarithmic scale (b). And (c) two plots of square root of drain current vs. gate voltage at $V_d = 50$ V also. Data are plotted for transfer characteristics of virgin sample (open square) and after stressing at a gate-bias of 50 V for 50 s (open circle).

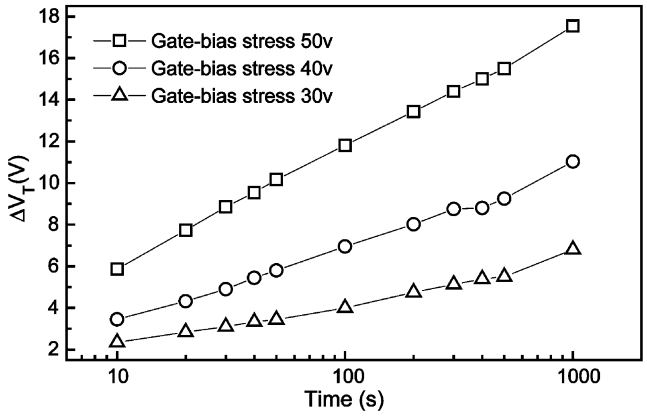

Fig. 3. The plot of threshold voltage shift (ΔV_T) as a function of stressing time at different gate-stressing voltage (50, 40, 30 V).

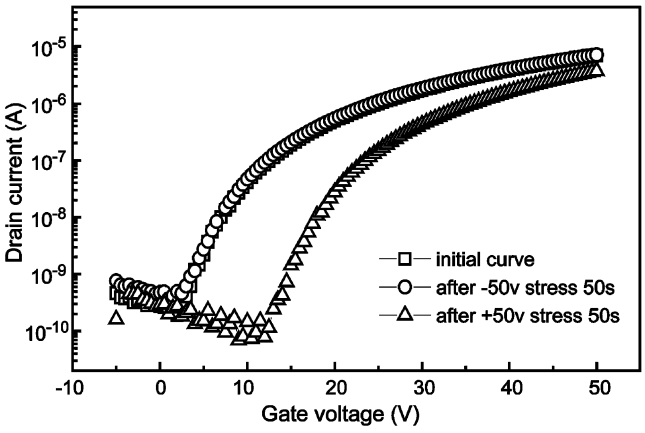

Fig. 4. An example of transfer characteristics before and after bias stress for a positive and a negative gate voltage.

created in the interface of active layer and dielectric layer after gate-bias stress. Fig. 2c also shows that two curves have almost same slope ($\mu_{EF}=0.017$ $cm^2\,V^{-1}\,s^{-1}$, which is similar to the value reported by Z. Bao for room temperature $F_{16}CuPc$ OFET device) [12]. This indicates that the field-effect mobility of the device does not change after gate-bias stress. This phenomenon quite consists with the mechanism of charge trapping in the gate insulator i.e. the applied gate potential is effectively screened by a buildup of space charge of trapped charges in the gate dielectric insulator.

The time dependences of threshold voltage shift ($\Delta V_T = V_T(t) - V_T(t=0)$) for a OFET at different gate stress voltages (50, 40, 30 V) are illustrated in Fig. 3. The threshold voltage shift is obtained by inserting a fast gate-sweep in a stress period at different time point. In addition, we set gate sweep from -5 to 50 V for 50 V gate-bias stress, from -5 to 40 V for 40 V gate-bias stress and from -5 to 30 V for 30 V gate-bias stress. A linear relation between ΔV_T and logarithmic time can be observed. The lines have different slopes, which represents different decay rate r_d (Eq. (1)). The relation is given by [13]

$$\Delta V_T = r_d \log(1 + t/t_0) \quad (1)$$

Where r_d is a constant, which related to the density of traps N_t (cm^{-3}) in the insulator and the tunneling constant λ (cm). This phenomenon has already been observed in the earlier research on OEFT with sexithiophene as active layer [8].

Fig. 4 shows that at positive gate-bias stress there is a big threshold voltage shift and at negative gate-bias stress the value of ΔV_T is almost zero. This phenomenon can rule out the mechanism of metastable state's creation. When positive gate voltage stress on gate contact, the OFET stay in a depletion state and a depleted layer form at the interface of organic semiconductor and insulator. So very little mobile carriers can be offered for the tunneling charge trapping process. Combined

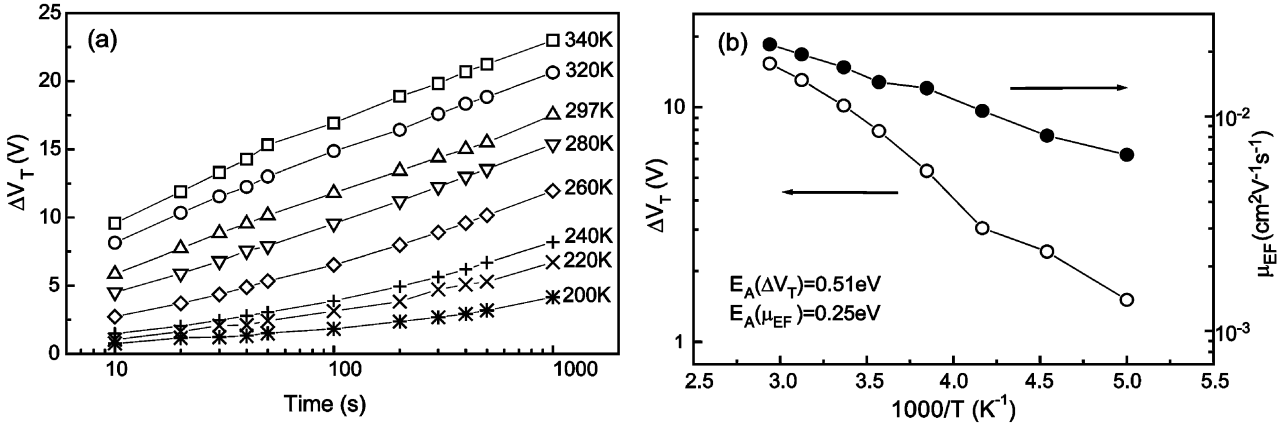

Fig. 5. Time dependence of ΔV_T for various temperatures (a) and the temperature dependence of the threshold voltage shift ($V_{G,bias}=50$ V, $t=50$ s) and the field-effect mobility (b).

with logarithmic relation of ΔV_T and time, we hypothesize that electron from conduct band of $F_{16}CuPc$ inject into trap site distributed in the band gap of the insulator by tunneling mode and then conduct in the insulator by hopping mode.

Fig. 5a shows time dependence of ΔV_T for gate-bias stress of 50 V at different temperature. Although ΔV_T somewhat deviated from the linear relation to logarithmic time at lower temperature, most of the curves show good linear fit. From the data measured for Fig. 5a, we can obtain the temperature dependence of ΔV_T and μ_{EF} as plot in Fig. 5b. The activation energy of ΔV_T is 0.51 eV, while that of μ_{EF} is 0.25 eV. The different activation energy of ΔV_T and μ_{EF} shows that supply function of mobile electron does not account for our case [11]. We hypothesize that the activation energy of ΔV_T may come from temperature dependent of hopping conduction in the insulator.

In conclusion, we have investigated the effects of positive and negative gate-bias stress on $F_{16}CuPc$ OFET with Ta_2O_5 as the insulator at various stress time, stress voltage and temperature. We find that the process of charge trapping in the insulator dominates the threshold voltage shift instability at high field is that often used in OFET device operation. This implies that changing deposition method or optimizing deposition condition could be beneficial in reducing gap trap site concentration and hence improving the OEFT device stability.

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