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Research on high-speed TDICCD remote sensing camera video signal processing

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Abstract

Video signal processing needs high signal-to-noise ratio (SNR) in high-speed time delay and integration charge coupled devices (TDICCD). To solve this problem, this article first analyzes the characteristics of the output video signal of a new type of high-speed TDICCD and its operation principle. Then it studies the correlation double sample (CDS) method of reducing noise. Following that a synthesized processing method is proposed, including correlation double sample, programmable gain control, line calibration and digital offset control, etc. Among the methods, XRD98L59 is a video signal processor for the charge coupled device (CCD). Application of this processor to one kind of high-speed TDICCD with eight output ports achieves perfect video images. The experiment result indicates that the SNR of the images reaches about 50 dB. The video signal processing for high-speed multi-channel TDICCD is implemented, which meets the required project index.

Keywords charge coupled device, correlated double sample, programmable gain control, digital offset control

1 Introduction

A CCD is a kind of large scale integrated semiconductor photoelectric device developed in the 1920's [1]. Because of its characteristics in photographing and recording of image information, it has extensive applications. Now, CCD is an important detector in imaging. It has numerous advantages such as large dynamic range, low noise outputs, high quantum efficiency and charge shifts efficiency, wide spectrum responding range, and good dependability [2].

A TDICCD is a new photoelectric sensor developed in recent years. Particularly, it is employed under low-intensity illumination and has higher sensitivity to goal than ordinary line CCDs [3]. TDICCD prolongs the total integration time by multistage integration, thus improving the sensitivity and SNR of the device. Therefore, it is widely used in the fields of aerospace, remote sensing, etc. With the above-mentioned characteristics, this device can not only improve detection ability, but also reduce the relative aperture of the remote sensing camera. Hence, the volume, weight and cost of the camera system are considerably reduced. Therefore, using TDICCD as a detector can make remote sensing camera lighter and smaller. With the advancement of the pixel resolution and manufacturing technique of CCD, the operating frequency of CCD is higher than before and readout speed of single-port has already reached above 12 MHz in applications. However, despite the development, noises still exist in the output video signal of high-speed TDICCD, and if not properly dealt with, they will affect the image quality and SNR of TDICCD signal seriously.

2 Structure of TDICCD and operation principle

Time delay and integration (TDI) is a scanning technique that can increase the sensitivity of the line-scanning sensor. TDICCD is a new type of CCD with area structure and line output. Compared with the ordinary line CCD, it has the function of multistage time delay and integration. In terms of structure, its lines are generally arranged in parallel and the pixels arranged in rectangular shape in line and progression directions. The number of the columns, denoted by N, is the number of pixels of its row, and the number of rows is the progression, denoted by M, of time delay and integration.

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The principle block diagram of TDICCD sensor is illustrated in Fig. 1.

TDICCD accumulates charge in the direction in which columns go, push and sweep progression from level 1 to level 96, as shown in the diagram. In the course of imaging, with the moving of the camera (or of the scenery), TDICCD sensitizes from level 96 to level 1 sequentially, and the charge is accumulated correspondingly. Finally, the charge package accumulated via multistage time delay and integration is transformed into the horizontal readout register of CCD, and is read out in the way charge is output from the ordinary line CCD. Therefore, the range of TDICCD output signal are M accumulated pieces of pixels, that is, M times of signal charge accumulated in one integration period of a pixel. Hence, when the output range is M times larger, the corresponding noise only increases by $\sqrt{M}$ times. Therefore, SNR is $\sqrt{M}$ times bigger [4]. Generally, M is at levels of 6, 12, 24, 48, 96, etc. in TDICCD. When the row periods are equal, TDICCD improves much more than the ordinary line CCD in degree of response.

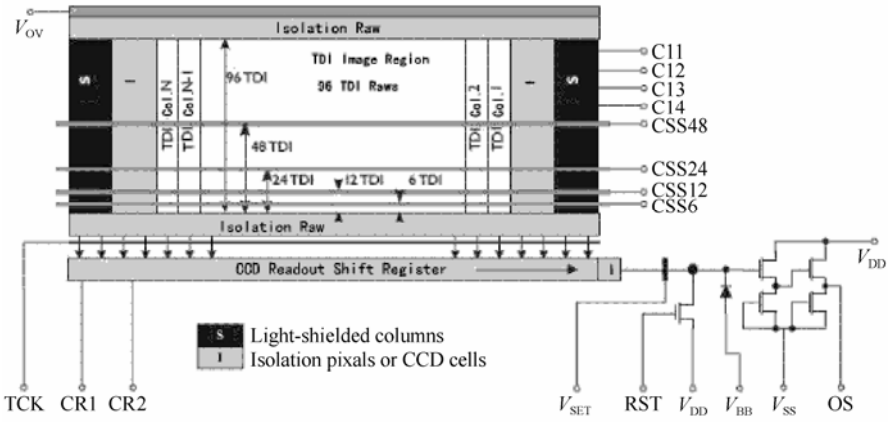


Fig. 1 TDICCD principle block diagram

The TDICCD sensor utilized in this article is manufactured by Canada DALSA Company. The sensor has high sensitivity and high differentiation and eight output channels. Its single port readout speed reaches over 25 MHz, with a maximum line frequency of 40 kHz, 4 096 photosensitive pixels of 8.75 μm by 8.75 μm, and a dynamic range of CCD pixel reaching over 1 600:1. The CCD with 96 levels time delay and integration has two periods in one work cycle: photo integration and charge transfer. Photo-charges are accumulated during the photo integration period. In the meantime, the shift-outputting charges, which are transformed into shift registers from the last frame, are transformed into output amplifiers, and invalid charges of pixel potential wells are cleaned. The photo-charges are transformed into shift register during the charge transfer period.

3 Characteristics of the output signal

To process TDICCD signals, its output signal characteristics must be analyzed first. There are two CCD output structures of a charge package: floating diffusion amplifier (FDA) and floating grid amplifier [5]. TDICCD adopts most frequently the FDA structure. For the FDA structure, the mainly produced noises during the detection of charges are reset noise, low frequency $1/f$ noise, and white broadband noise [6]. The reset noise emerges mainly because of the switch. The $1/f$ noise, also called glimmering noise and is mainly from the metal oxide semiconductor field effect transistor (MOSFET), is caused by the crystal defects of the semiconductor. The white noise, a resistance thermal noise, is primarily caused by the rising temperature of the resistance in the circuit which is related to the impedance R_L of the whole output level. Of the three kinds of noise, the reset noise is by far the major noise. The structure of the principle diagram of TDICCD floating diffusion amplifier is shown in Fig. 2. The TDICCD output structure is used to reduce the $1/f$ noise by the built-in two-level source emitter follower amplifier with bury channel. To reduce white broadband noise, the MOSFET ditch width has been optimized.

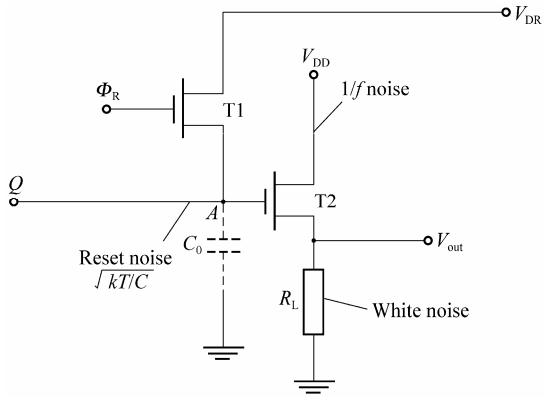


Fig. 2 Floating diffusion output principle diagram

T1 is a reset MOS transistor in the diagram, C_0 is a floating diffusion capacitance connected to the ground, and T2 is an outputting MOS transistor. When C_0 is recharged by reset noise, the extraction voltage value of the reset noise at point A is as follows [7]:

$$\overline{V^2(t)}=\frac{kT}{C_0}\left[1-\exp\left(-\frac{2t}{RC_0}\right)\right] \tag{1}$$

Here, R is the alternating current (AC) resistance connected to the ground, and t is the reset pulse cycle. Because of the extremely high input impedance of T2, and the floating diffusion region and base region reverse, it can be assumed that R is the ditch resistance of reset tube T(R_{ON} is the connected resistance of T1, R_{OFF} is the cut-off ditch resistance of T1). When reset, i.e., T1 is on because Φ_R is added to positive pulse. Then $V_A \approx V_{DR}$, $R=R_{ON}=10^4\ \Omega$. In general, C_0 is at 0.1 pF level. The time constant is $R_{ON}C_0=1$ ns, and is of nanosecond grade. Generally, the reset pulse frequency is less than tens of MHz, and the corresponding pulse cycle is of microsecond grade. It is obvious that $t>>R_{ON}C_0$. Hence, one has the following equation:

$$\overline{V^2(t)}=\frac{kT}{C_0}\left[1-\exp\left(-\frac{2t}{R_{ON}C_0}\right)\right]=\frac{kT}{C_0} \tag{2}$$

That is, at the interval between resets, reset noise charges will quickly saturate C_0 and stabilize the system. When Φ_R is zero-potential, the reset tube T1 is cut off. Then point A is in the state of high resistance, and $R_{OFF}>>10^4\ \Omega$, which may reach above $10^{10}\ \Omega$. The time constant now is $R_{OFF}C_0=1$ ms. It can then be known that $t>>R_{OFF}C_0$. If T1 is not got through, that is C_0 is empty without any reset noise charge, then the reset noise voltage at point A is

$$\overline{V^2(t)}=\frac{kT}{C_0}\left[1-\exp\left(-\frac{2t}{R_{OFF}C_0}\right)\right]=0 \tag{3}$$

If T1 has already been through, it must be kept in mind that the reset noise charges C_0 as the time constant $R_{OFF}C_0$ requires, and that C_0 is discharged slowly. As mentioned above, the effect of charging approximately amounts to zero. Therefore, it can be assumed that the extraction the voltage value of the reset noise at point A is:

$$\overline{V^2(t)}=\frac{kT}{C_0}\exp\left(-\frac{2t}{R_{OFF}C_0}\right)=\frac{kT}{C_0} \tag{4}$$

That is, because the RC time constant in the return circuit of discharge is very big, during the interval that T1 closes, the reset noise can be considered to be still kept in C_0 when 'resetting'. The output voltage wave of the reset MOSFET of TDICCD is displayed in Fig. 3.

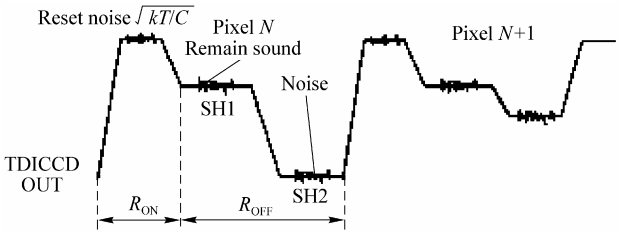


Fig. 3 Output voltage wave of the reset MOSFET of TDICCD

To reduce the readout noise, the correlation double sample (CDS) technology is used for reducing noise of high-speed CCD signals. This method can not only filter reset noise, but also can filter to a certain degree white broadband noise and $1/f$ noise [7].

4 Correlation double sample

Among the ways of reducing CCD output noise, the CDS method is often employed in applications that require high-speed operations [8]. The operation principle of the CDS and sample time sequence are illustrated in Figs. 4 and 5. In Fig. 4, the dotted line on the left side denotes TDICCD readout circuit and on the right side is the CDS circuit. In Fig. 5, the sample points S_1 and S_2 are the positions of the CDS. The basic principle of the CDS is as follows. Because the noise voltage of the equivalent capacitance output from the reset tube is slow in rise and fall when the reference level and signal level are output, two samples are taken in the same pixel period. If the interval between the two samples is far less than the time constant $R_{OFF}C_0$, the requirements are met in practical applications. Thus, because the difference between the noise voltages of the samples is quite small, the noises of the two samples are related in time. With the two

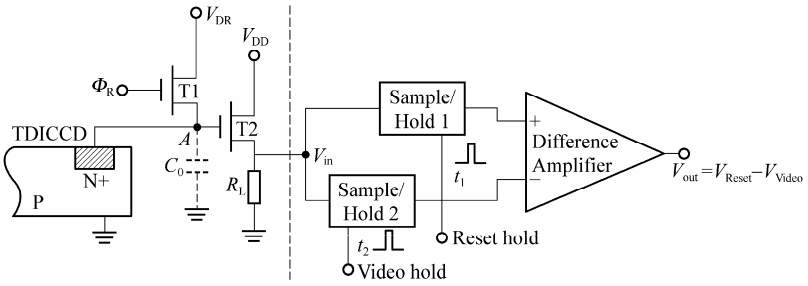


Fig. 4 TDICCD CDS technology basic principle block diagram

sample values subtracted, the reset noise is suppressed from the input signal. When the two samples are subtracted, real video signal level is obtained.

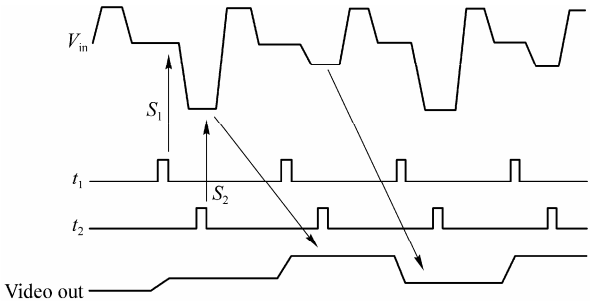


Fig. 5 Time sequence of the CDS sample of TDICCD signal and output video waveform

The choice of the position of sample and hold is critical to the CDS technique. The strict phase relation between the two sample and hold pulses and CCD readout signals, and the sample and hold device have precise symmetry.

Before the real CDS circuit is placed beforehand one level amplifier, which adapts CCD output to the forthcoming circuit, and adjusts amplitude, matches impedance, and suppresses white broadband noise. While reducing the transmission loss of signals and exterior disturbance, the preamplifier is placed as close as possible to the CCD output end. LMH6722 operation amplifier by NS Company is employed to adapt to the characteristics of the TDICCD readout signals.

5 Special-purpose video signal process circuit

The purpose of CCD output signal process is to reduce noises and interference as much as possible, instead of decreasing high definitions of images or guaranteeing the image signals to change linearly with the luminance of the goal in the dynamic range of CCD. Meanwhile, CCD readout signals must be processed digitally to be processed by a computer and stored in large memory. To achieve the above-mentioned ends, the process circuit must prossess the CDS, programmable gain amplification, digital dark level calibration, and analog to digital conversion, etc. In the past, independent integrated circuit was usually used to perform each individual function, which inevitably caused circuit complication, larger power consumption, and debug difficulty. With the development of the microelectronic technique, the special-purpose videos process chip that has integrated the above-mentioned functions is available at present. EXAR Company is one of the first companies to produce such chips in the world. Based on the practical needs the XRD98L59 video processor that EXAR Company developed was adopted here.

The XRD98L59 has 20 MHz sampling rate and contains a high bandwidth differential CDS, 8-bit digitally programmable gain amplifier (PGA), 10-bit analog-to-digital converter (ADC) and improved digitally controlled black level auto-calibration circuitry with pixel averager, hot pixel clipper, and a DNS filter [9]. Its has powerful function, superior performanceand low price. The function module will be analyzed in detail, and several practical engineering problems in CCD signal processing applications are briefly explained.

5.1 CDS and PGA

The circuit of CDS principle block diagram in XRD98L59 is shown in Fig. 6.

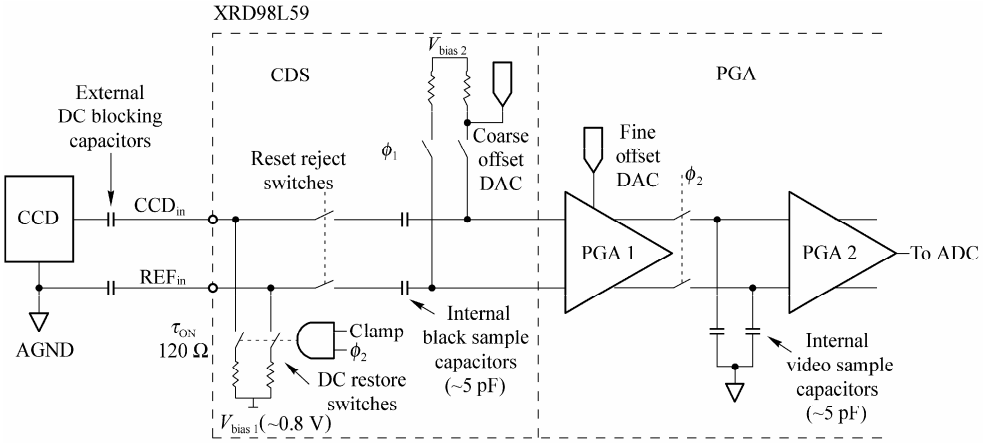


Fig. 6 CDS and PGAs within XRD98L59 principle block diagram

Through the preamplifier, the CCD output signal level has been adjusted, the output impedance matched and the system noise has been suppressed. The buffered difference signal of the CCD becomes the input signal of the CDS through the

direct current (DC) interrupting capacitors C_1 and C_2. The input difference of the CDS can effectively suppress the switch disturbance. Meanwhile, adopting smaller capacitors can obtain a longer period of hold time. The CCD_{in} end in Fig. 6 is a real video signal input end, and the REF_{in} end is the video signal ground. The right control of time sequence is the key to image quality. To analyze the working process of the CDS of the video processor, the CDS time sequence diagram (as shown in Fig. 7) and a CDS time sequence diagram that includes internal control signal (as shown in Fig. 8) will be combined.

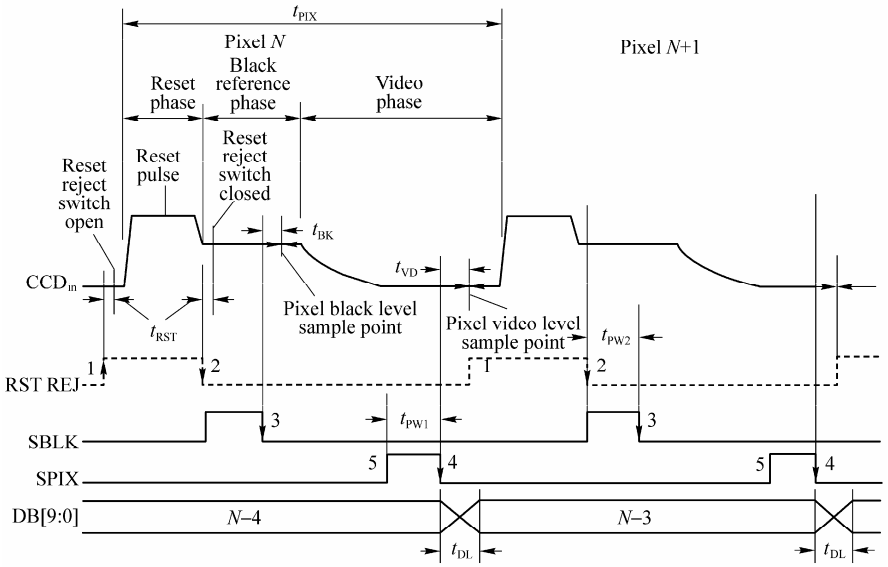


Fig. 7 CDS time sequence diagram

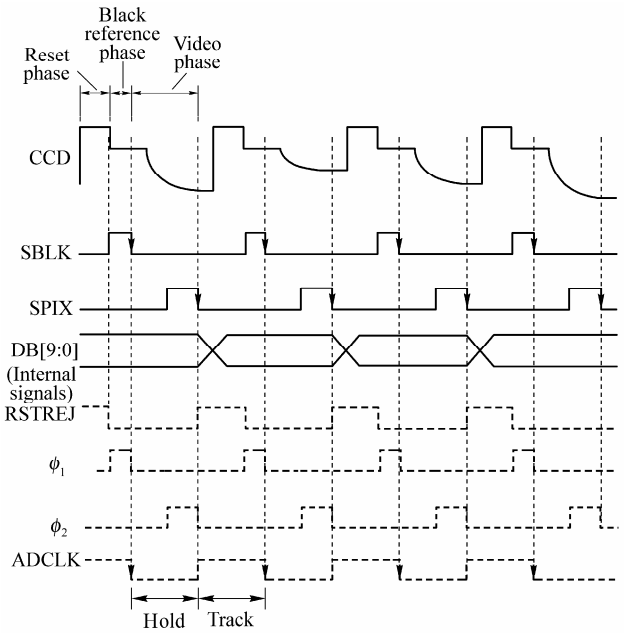


Fig. 8 CDS including internal control signal time sequence diagram

The pixel period of the video signal of the CCD is t_{PIX}. RSTREJ is an internally generated signal with certain phase relation to ϕ_1 and ϕ_2. RSTREJ disconnects the input to reject CCD reset noise after the SPIX and before the SBLK sampling events. When the RSTREJ is high-level, the CDS is isolated from the CCD input signal. When RSTREJ is low-level, the internal capacitor samples the reference level. The activation of RSTREJ can be controlled by internal clock register. To avoid the influence of the serial interference produced by reset pulse, the RSTREJ pulse should be activated, and the phases of the high level of RSTREJ and the interference level of reset pulse of the CCD video signal should be matched. The external sample control pulses SBLK and SPIX produce the internal electronic switch control pulses ϕ_1, ϕ_2 and ADCLK through the inside clock network. In the default state, the pulses ϕ_1 and ϕ_2 are delayed by 3.5 ns and 2.7 ns, respectively, compared with the external control pulse. The conversed data by the AD is valid after t_{DL} plus the change in ϕ_2 aperture delay. The pipeline delay of the entire XRD98L59 is four clock cycles. Whereas the aperture delay time t_{BK} between ϕ_1 and SBLK and t_{VD} between ϕ_2 and SPIX can be changed by varying the value of the internal delay register. By adjusting the falling edge position of ϕ_1 and ϕ_2, the precision can reach 2 ns/sb, hence the CDS sample position can be accurately controlled for achieving the optimal reducing noise effect, which is the unique programmable aperture delay function of the sample pulse of the XRD98L59 chip series.

At the beginning (or end) of every video line, the DC

restore switch is controlled by the combination of the CLAMP signal and the ϕ_2 clock. When the switch is on, it forces one side of the external capacitors to be an internal $V_{\text{bias 1}}$ level (approximately 0.8 V). During the black reference phase of each CCD pixel ϕ_1 (sample black reference) switches are turned on, shortening the PGA 1 inputs to a second bias level $V_{\text{bias 2}}$. The coarse offset digital to analog convertor (DAC) adjusts the $V_{\text{bias 2}}$ level for canceling offset in the CCD signal. When ϕ_2 switches are turned off, the pixel black reference (V_{BLACK}) is sampled on the internal reference sample capacitors, and the PGA is ready to gain up the CCD video signal. During the video phase of each CCD pixel, the difference between the pixel black reference level and video level is transmitted through the internal reference sample capacitors and converted to a fully differential signal by the PGA 1 amplifier. When ϕ_2 pixel signal value sample switches are turned off, the internal video signal sample capacitors follow the differential signal amplified by PGA 1 and the fine offset DAC adds excursion adjustment compensation to the positive output end.

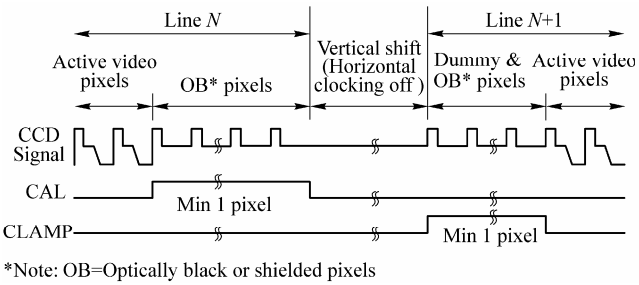
5.2 Programmable gain control

The voltage of CCD output signal and the system gain and offset of the signal processing determines the voltage of the video signal input to ADC. Because the amplitude of CCD output signal changes with the power of the intensity of illumination of the incidence, only through the signal processing system, regulating dynamically gain and offset can make luminance of the output digital image and contrast ratio meet the demands. Programmable gain control can adjust video signal dynamically. Based on correspondence relationship between input and output signals, it can be known that the value of output signal and luminosity of detected signals need to have a certain correspondence relationship. As the PGA part in Fig. 6 shows, because the product of gain bandwidth is restricted, the PGA of XRD98L59 is realized in two stages, PGA 1 realizes 0 dB, 8 dB, 16 dB rough gain control, and PGA 2 realizes adjustable fine control from 6 dB to 22 dB and the step is 0.125 dB. According to the 8 bit control code of gain register (range is from 0 to 255), the overall system gain can be adjusted from 6 dB to 37.875 dB. The formula is:

$$\text{Gain} = 6 + 32 \times \frac{\text{code}}{256} \quad \text{(dB)} \tag{5}$$

5.3 Line calibration mode

The process of line calibration is to calibrate dark reference level of optical black (OB) pixel of each line output of CCD. DC interrupting capacitors are usually needed at the input end of XRD98L59 for inputting the AC video signals into CDS. Because the fluctuation of luminosity, temperature, and power voltage make the dark level of video output signal fluctuate. In reality, whereas, the dark level needs to remain stable and the process of dark calibration is DC level restoration. Fig. 9 shows one kind of time sequence of line calibration. Generally, there are black pixels at the beginning or end of the video signal of CCD output (also called the dark level reference pixel). The position and number of the black pixels in different CCDs vary. When calibrating, the CAL and CLAMP signals are needed to define the number and position of calibrating black pixels. Meanwhile, the beginning and the end of each line image are determined. The CAL and CLAMP are two control signals of the line clock, which can be operated in two modes.



*Note: OB=Optically black or shielded pixels

Fig. 9 CLAMP&CAL line calibration mode time sequence diagram

In the CAL&CLAMP mode, the CAL is used to define OB pixel of the line end and to calibrate dark level. The CLAMP makes the input end of CDS restore the direct current clamp. Usually, the CLAMP defines OB pixel at the beginning of the line. If the number of those OB pixels is bigger than that at the line end, the CAL can be used to define the OB pixel at the line beginning, and the CLAMP can define the line end. In this mode, the CAL and CLAMP signals must not be activated simultaneously. In the CAL ONLY mode, CAL signal is used to activate the direct current clamp restoration and define OB pixels for calibrating dark level. In this mode, the CAL signal should have at least 5 pixel periods, and may as well be defined where it has the most black pixels at the line beginning or end. Because the line calibration takes place at the beginning or end of each line, it is also called line rate clamp [10].

5.4 Digital dark level offset calibration control

To obtain the biggest resolution ratio and dynamic range, XRD98L59 adopts calibration to correct the digital controlled circuit to adjust the dark level offset. Fig. 10 shows the correcting principle of feedback and compensation.

The function unit contains multiple function modes. As the CAL and CLAMP have already defined the DB pixel, to prevent the hot pixels in the black pixel area from affecting

the dark reference level, the hot pixel clipper clips the black pixels with response data value of over 127(7 fh) to prevent these pixels from being included in the calibration network or affecting the whole systematic performance. The pixel averager filters on average black pixels defined by the CAL signals. During the calibration of the dark level, the output signal of ADC is the value of dark reference voltage, which will be compared with the memory value of target and offset register. The offset control value will be increased or decreased accordingly. The coarse & fine accumulators and offset difference feedback adjust the signal in the CDS and PGA signal flow according to the output value through two DACs, thus correcting the systematic offset. The digital noise suppressing filter (DNS filter) is used to eliminate the changes on the dark level offset, in case the calibration loop is oversensitive to measured offset. The calibration value of dark level offset can be set up through the serial register, and can be remeasured automatically by system after each calibration process ends. The setup value of the target-offset register is 20 h after the power is on, and the typical value is from 02 h to 3 fh.

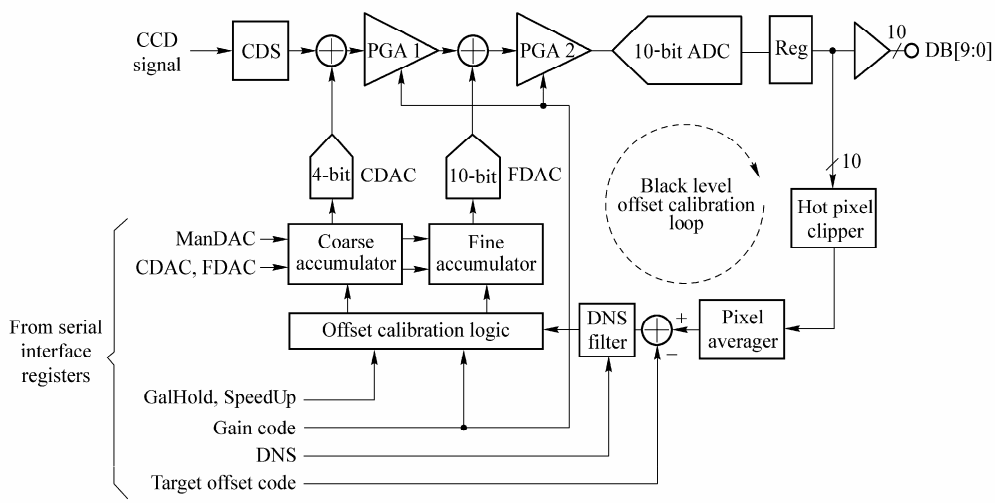


Fig. 10 The dark level offset calibration principle block diagram

5.5 A/D analog to digital conversion

XRD98L59 integrates the ADC of 10-bit resolution ratios and 20 MSPS. The sample moment of the ADC is determined by the ADCLK signal produced internally, which reduces the external signal kinds. It takes pipeline delay of four pixel periods for the video signal to be input and for such signal to be output as the correspondent digital signal. Therefore, the pipeline delay must be taken into consideration while available line signal is sent into memory, otherwise, all the pixels will move horizontally, and the image data may be wrong at the beginning and end of each line.

6 System construction and process analysis

To process the 8 Ports high-speed TDICCD videos signals used, the system construction is shown in Fig. 11.

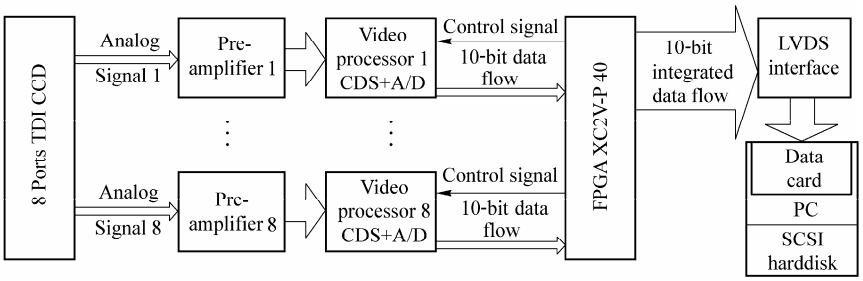


Fig. 11 System block diagram

Adjusted by the preamplifier, eight analog video signals output by TDICCD meet the requirement of the input and are sent to video processors. Under the control of FPGA, the video processors fulfill processing the input video signals and convert them to parallel data flows. These parallel data flows are transformed from parallel flows to serial ones (dataflow synthesis) by configured double ports RAM in the FPGA and then form a single channel data flow with line

synchronization, data clock and image data. The data then undergo uninterrupted buffering and processing. The output data flows are sent into image acquisition card of computer through LVDS interface with LVDS format camera form for finishing the display and storage of image data in real time. The system adopts FPGA as the control-core to make the design all-purpose and flexible. XC2VP40 produced by Xilinx Company is selected to carry out tasks such as time sequence producing, communication controlling and eight channels image data merging.

7 Conclusions

This article presents in detail the procedures in processing high-speed TDICCD output video signals together with special-purpose video signal processor XRD98L59. By analysing each functional unit circuit and special chips, eight pieces of XRD98L59 have been successfully used in processing parallel the eight-channel high-speed pan TDICCD output video signal. The readout frequency of single port is 16 MHz, and the contrast and luminance can be adjusted according to the amplitude of the signals. Simultaneously, the line rate and time of exposure can also be adapted. The design meets the systematic function requirement. The actual panchromatic test image obtained is shown in Fig. 12.

Fig. 12 Test image of eight-channel TDICCD output

The video image data demonstrate that the image is of high quality, and no disturbed phenomenon exists among the channels.

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